Design Procedure for System in Package (SIP) Business

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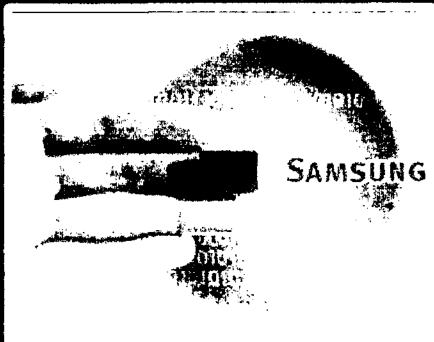
SIP Design Flow



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IPT Development
System LSI Business
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SAMSUNG ELECTRONICS Co.

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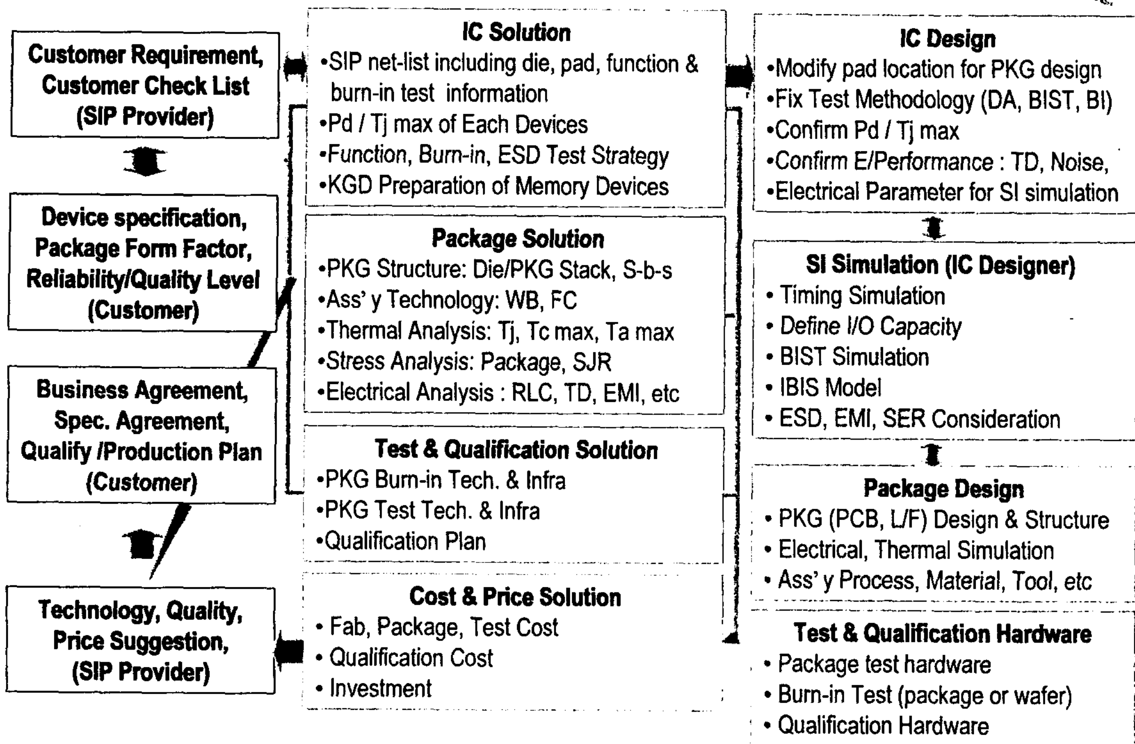
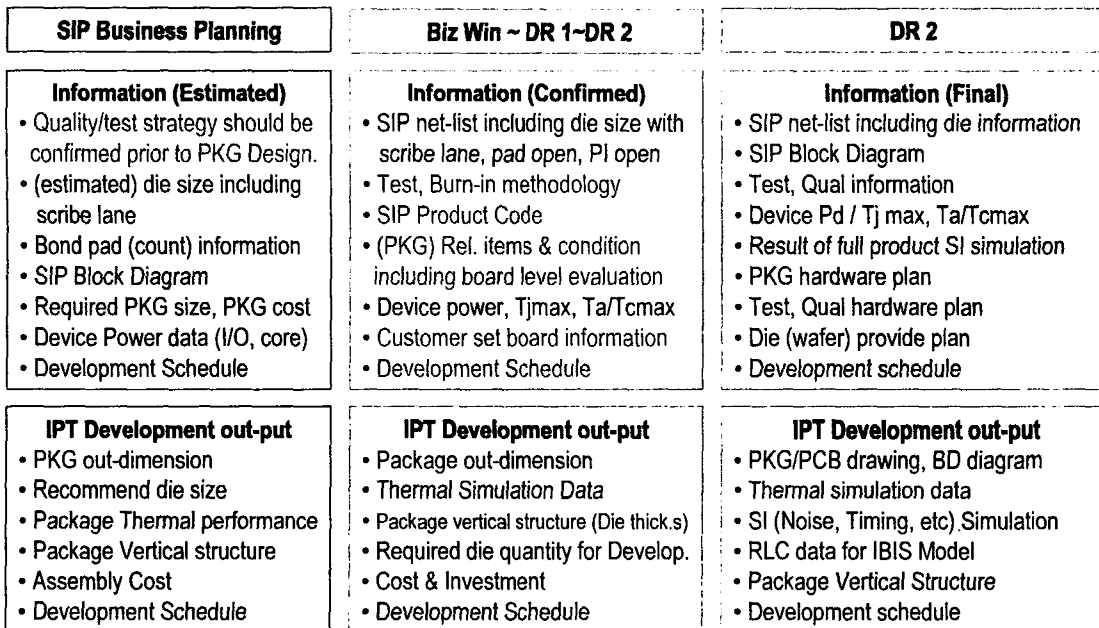
I. SIP Product Design Flow



II. SIP Design Flow



Test & Burn-in

SIP Thermal

SIP SI

SIP Block diagram & Net-list

2-1. SIP Design (Summary)

❑ In order to start SIP Project

- Marketing (& ASIC team) should present biz planning, schedule, device/SIP specs., in SIP TFT prior to request SIP development for package development project.
- In order to prevent (PCB) revision, test, burn-in, & quality strategy should be fixed by SIP TFT (PE/Test, QA) prior to request for PKG development.
- Target product price/cost, package/ test cost should be delivered and reviewed.

❑ Minimum Information for PCB Design, Package Size, and Cost

- (Required) package form factor : size, height, type (BGA, QFP), Pin count/pitch
- (Estimated) each die size including scribe lane
- (Estimated) pad inform. : count, pitch, configuration(in-line/staggered), (open) size
- (Estimated) each device (I/O & Core) power (especially for DRAM embedded SIP)
- SIP Block diagram, and net-list using excel sheet format

❑ Why is the initial evaluation important ?

- The higher logic power resulted in spec. over of DRAM Tjmax. This caused business drop → Thermal simulation of some SIP product is essential in the beginning stage of SIP business planning (or design) stage. (i.e., DRAM embedded SIP)
- When SIP is developed using discrete packages, the I/O driver Capa. of each device may be so high for SIP. Since I/O driver capa. was optimized to discrete package and set board environment, this resulted in severe noise problem in SIP.

→ In this case, the electrical performance of product (including PKG) should have been considered (simulated) in the beginning stage of business planning (or design).

2-2. SIP Design Guide I

❑ Technical availability

- SIP quality level and test method should be decided prior to consider PKG solution.
- SIP net list is the most important for providing fast and exact solution.
- Confirm of product (device) function, PKG form form factor, reliability & quality level
- Supplying plan of memory including version change should be confirmed.

❑ **Cost & price availability**

- Price (cost) is also the most important factor for SIP business.
- SIP cost is strongly dependent on the required quality level and its test strategy.
- In general, SIP has manufacturing cost merit compared with SOC, and also, comparing with discrete packages, SIP has set cost merit in spite of its higher manufacturing cost.

❑ **Close co-work between customer, marketing, IC & Package engineer**

- To overcome technical limit, close relationship between each parts is required.
- In case of memory embedded SIP, KGD is essential to get high quality level and low cost. Customer (application) specific test program is essential for getting low cost test program.

2-3. SIP Design Guide II

❑ Key information for SIP design

- In general, SIP net list including memory device IP may be fixed.
- Logic device including interface with other dies should be optimized with SIP design.
- Test capability including function, burn-in, & ESD should be applied to the SIP net list.
- Aspect ratio and bond pad location of each dies must be adjusted with package design.
- Pdmax of each device should be re-confirmed (refer to thermal engineering plan file)

❑ SIP design using EDA (CAE tool) system

- Signal integrity including timing delay should verified with ASIA and Cubicware.
- SIP performance should be verified based on package (substrate) design with EDA.
- The verification categories are Timing skew, Power Noise, X-talk, EMI, etc.
- SI verification of product level should be carried out by logic designer.
- Product thermal performance & product quality should be proven.

❑ Close co-work between customer, IC & Package engineer

- In case of SIP limitation, customer spec. should be revised to get solution.
- It is required for customer to provide exact and detail set information to estimate thermal and mechanical simulation data. This provides the most cost effective SIP solution and win-win profit for each other. (refer to SIP questionnaires and others)

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2-4. SIP Design Guide III

❑ Customer evaluation & qualification sample

- In-time CES (customer engineering sample) delivery
- Strong internal qualification system
- Fast corrective action and feed-back

❑ SIP quality & reliability

- Quality procedure, level, system agreement with customer
- Prepare test program including interface vector, and reliability test infra.
- Prepare production control (trace) system : SIP code, SIP process code.

❑ Close co-work between customer, IC & Package engineer

- Agree qualification plan and schedule for each other.
- Share test results and seek best solution.
- Deliver power measure data on the application set board (refer to thermal file).

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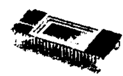

2-5.SIP Design Guide Ⅳ

❑ Stable product delivery

- In-time volume delivery
- Strong quality control system
- Fast corrective action and feed-back

❑ Low cost solution

- Pursuit low cost solution endlessly.
- Require close re-work.
- Simplification of test procedure is the best solution for low cost SIP.

❑ Close co-work between customer and SIP maker

- Co-work with customer is essential for test simplification including BI skip.
- Share the profit of cost saving with customer.

APPENDIX Ⅰ : Information for SIP Design

❑ Package Form Factor

- Package Dimension, Height, Pin pitch/count, and Package pin net list (Customer)
- SIP net list including test (BI, DA / BIST, ESD) information (SEC: IC Designer)
- Block diagram including pin-out of each devices should be delivered.
- Mechanical information of each devices (die size, pad, scribe lane, PI open/thickness)

❑ Package Thermal Performance

- Devices power : I/O & Core (Device designer) respectively
    - ✓ Device operating frequency in application set
    - ✓ Loading capacitance for I/O, Read band width for I/O (Customer)
- Tj max of devices (Device designer), Ta max of application set (Customer)
- Measure the actual deice power (I/O & Core) in the application set (Customer)
- Refresh time spec. of DRAM in application set (Customer)

❑ Package Electrical Performance

- Data link speed
- Required timing skew margin, Required Vdd variation
- I/O Model (IBIS or Net-list)
- Set board information, if possible (Customer)

❑ Package Reliability & Quality Level

- Product quality level (Customer)
- Product (Package) reliability level, Item, and conditions (Customer)
- Board level reliability items, condition, and test hardware
- Green package requirement (lead-free, halogen-free, etc)

APPENDIX Ⅰ : Information for SIP design

Ⅰ. Package Form Factor

Item	Description	Data (Unit)	Remark
Package Type	BGA, QFP, or Other		
Package Body Size (BGA Type)	Area Dimension	X*Y (mm)	
Package Body Size (Lead Frame Type)	Mold Body Area	X*Y (mm)	
	Area with Output Pin	X*Y (mm)	
Package Height (BGA Type)	Total Height including Ball	(mm)	
Package Height (L/F Type, i.e., QFP)	Mold Thickness	(mm)	
	Height Including Output Pin Stand-off	(mm)	
Output Pin Count		(ea)	
Output Pin Pitch		(mm)	

Ⅱ. Package Thermal Characteristics

Item	Description	Data (Unit)	Remark
SIP Thermal Performance	Tj	(℃/W)	In the steady ambient tem.
	Tj	(℃/W)	In the steady ambient tem.
Maximum Junction Temperature of Each Devices	Tjmax	(℃)	
Maximum Ambient Temperature of Thermal Test	Tamax	(℃)	
Pdmax of ICs, Operating Voltage	Each Core IPs	(mV)	
	Each I/Os	(mV)	
Max. Operating Frequency of ICs in Application	Frequency	(MHz)	

- Package design stage : requires estimated power of each cores and I/Os.
- Thermal characterization stage : requires measured power of each cores and I/Os.
- *Each dimensions of I/Os & cores on die should be delivered in the design stage.*
- In the case of power data, details of calculation procedure should be delivered.

Ⅲ. IC Information (Logic)

Item	Description	Data (Unit)	Remark/Example
Each Core IP	Clock Speed		Description of Function
	Power	(mV)	
	Tjmax of each core IP	℃	
	Each Dimension(X*Y)	(㎛)	Drawing on die
(Each) I/O information	Power, Dimension	(mV), (㎛)	
Die Size	X * Y axis	(㎛)	
Scribe Lane Width	X * Y axis	(㎛)	
Bond Pad count	Pad # of each device	ea	
Bond Pad Pitch	In-line or Staggered	(㎛)	70㎛, 35/70㎛
Bond Pad Size	X × Y	(㎛)	
Space between pad open and scribe lane		(㎛)	
Bond Pad Size	X × Y	(㎛)	

- **SIP net - list including interface with other devices and considering package test should be delivered using excel format. The pad coordinates of each devices also should be included.**

Ⅳ. SIP Net-list (Including SIP Block Diagram)

❑ To provide device information (excel format)

- Die stepping size including scribe lane.
- Bond pad coordinates including its function
- Bond pad size, Space between bond pad and scribe lane

❑ To provide interface information between devices in SIP

- Interface information of pads of devices should be expressed by block diagram.
- Interface information should be expressed in SIP net list using excel format also.
- According to the PCB lay-out, PCB designer can request change of the pad location of device (logic) and modification of die aspect ratio.

❑ To provide package pin-out information for function test, burn-in test, reliability test

- According to the test strategy, SIP designer should deliver the net-list information including the function, burn-in, reliability (ESD, EMI, etc) level tests to package team.
- In case of memory devices in SIP, KGD is essential to get high quality level and low cost. Customer (application) specific test program is essential for getting KGD and low cost test program.

Ⅴ. IC Information (Memory : SDRAM/ Flash/ SRAM/ UtRAM)

Item	Description	Data (Unit)	Example / Remark
Memory Spec.	Density	Mb	64Mb, 128Mb, 256Mb
	Bit Organization	×	×8, ×16, ×32
Die Size	X * Y axis	(㎛)	
(Each) I/O Information	Power, Dimension	(mV), (㎛)	
Each Core Information	Power, Dimension	(mV), (㎛)	
Tjmax of each core		℃	
Scribe Line Width	X * Y axis	(㎛)	
Distance between pad and scribe lane		(㎛)	
Pad count	Pad # of each device	ea	
Pad Pitch	In-line or Staggered	(㎛)	70㎛ In-line, 35/70㎛ staggered
Pad Size	X × Y	(㎛)	

• **Memory net list should be delivered using excel format.**

Ⅵ. Quality (Reliability) Requirement

Item	Description	Requirement	Example/Remark
Precondition Test	**Bake**		**125℃, 24hrs**
	TC 5 cycle		**-65 ~ 150℃, Dwell: 10 min/ transition: < 5 min**
	Soak Level		**Level Ⅰ(85℃/ 85RH, 168hrs)**
	Peak IR Temp.		**220(leaded), 240, 260(leadfree)℃**
Temperature Cycling Test	**Temp. range, cycle, Temp. change**		**-65 ~ 150℃, 500 cycles, Dwell 13 min/ Transition 2 min**
Pressure Cooker Test	**Temp., Duration R- Humidity**		**121℃, 2 atm, 100% RH, 192 hrs, un-saturation**
High Temperature Storage Test	**Temperature, Duration**		**150℃, 0.5K hrs (1K hrs Monitor)**
Highly Accelerated Temperature and Humidity Stress Test	**Temperature, R- Humidity, Duration**		**130℃, 85% RH, 192 hrs, unbiased**
Temperature Humidity Bias	**Temperature, Humidity**		**85 ℃/ 85 %RH, Static**
CDM/MM/HBM Level	**ESD Test**		**2,000 V**
Alpha Particle	**SRAM (core)**		**0.5 Particle /㎠ hr**

I . (Mobile Product) Board Level Evaluation Items

Item	Objective	Application	Remark
Board Level Solder Joint Reliability Test	• Estimate solder joint lifetime • Board Design Guide	• All application • PDA, HHP, Potable PC	• Customer need • Need Application set board information
Thermal Performance	• Package type selection (Tj define) • Measure Θ ja, Θ jc (Tj): qualification → define (hot) test temperature • Measure Tc in the application set → Reference data for each other	• All application • PDA, HHP Portable PC	• Simulation (Design) • Measure (Verification) • In the steady state ambient condition
Drop Test	• Endurance when set drops • Hand held / Portable product	• PDA, HHP, Portable PC	• Customer need • Different test condition for customer & set
Bending Test	• Endurance for repeated button in-put • Button type data input product	• HHP	• Customer need • Different test condition for customer & set
Twist Test	• Endurance for twist deformation when memory card/module is inserted into application set. • Slot insert application with connector	• Card application • Case by case	• Customer need • Different test condition for customer & set