3D LSI Technology and Wafer-level Stack

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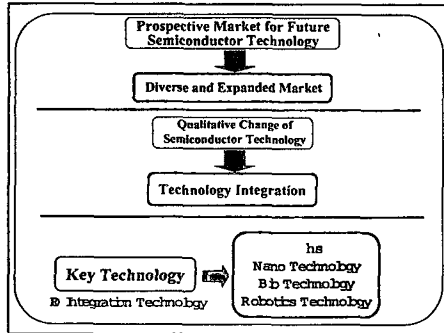
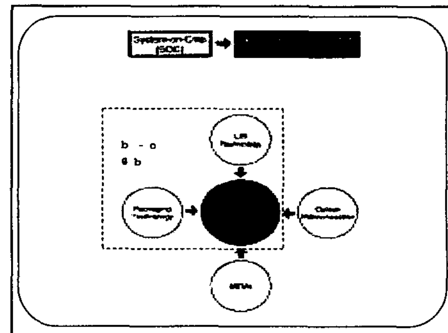
Tohoku Univ.

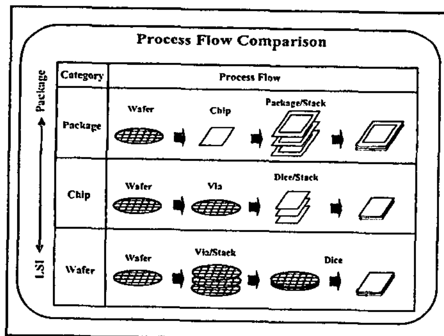
Outline

1. Introduction
2. Wafer Level 3D Integration Technology
3. New Integrated Systems Using 3D Integration Technology
4. Summary

Tohoku Univ.







Wafer Level 3D Integration Technology

Monolithic 3D LSI

- Stacking of passive element
- Stacking of a-Si/ poly-Si devices
- Re-crystallization and seed epitaxy

Wafer Stacking 3D LSI

- Bulk wafer stacking
- SOI wafer stacking

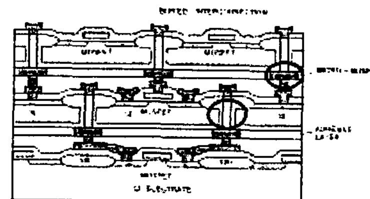
Previous 3D-LSI Technology

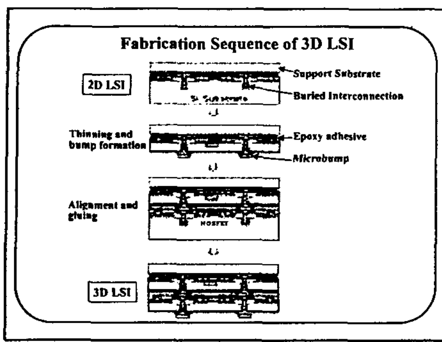
- Stacking of devices fabricated by beam annealing and re-crystallization method
- Transferring and bonding of thinned SOI device wafers

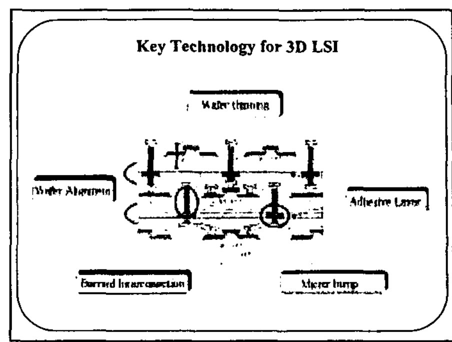
New 3D-LSI Technology proposed by Tohoku University

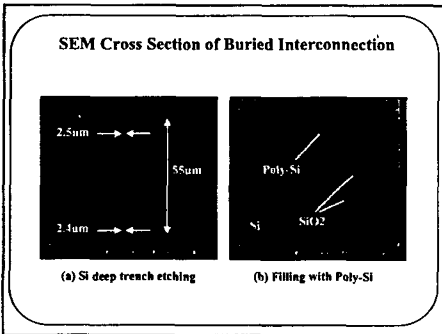
- Bonding of LSI wafers with buried interconnection
  - Silicon substrate thickness 10 – 70 µm
  - Buried interconnection (Micro-bumps
  - Wafer bonding with liquid adhesive injection
    No wafer transfer
  - Wafer level 3D CSP
- Merge of LSI technology and package Technology

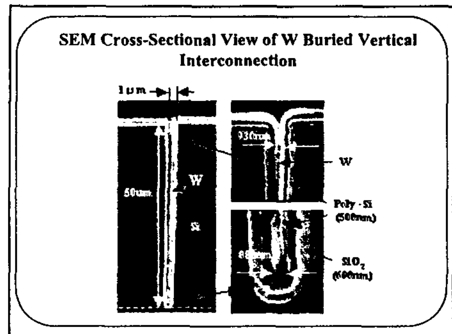
Cross-Sectional View of Three-Dimensional LSI

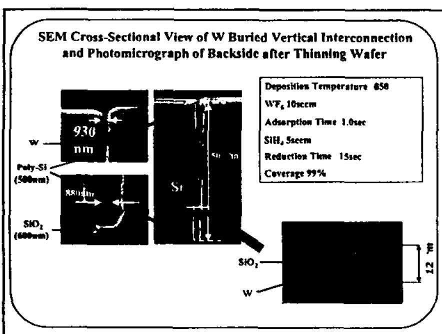


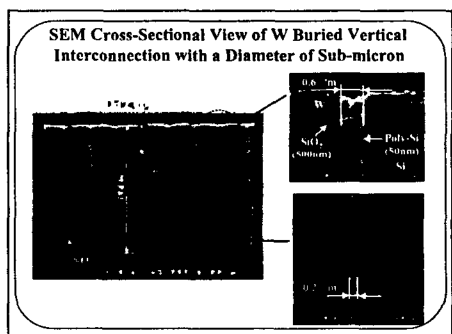

Fabrication Sequence of 3D LSI
2D LSI
Support Substrate
Buried Interconnection
Thinning and bump formation
Epoxy adhesive
Microbump
Alignment and gluing
3D LSI

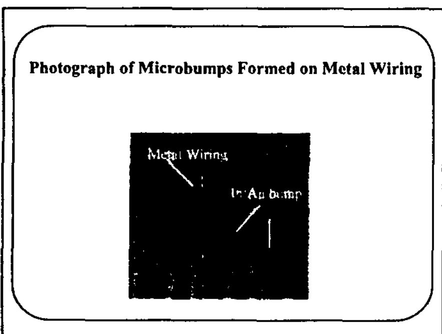

Key Technology for 3D LSI

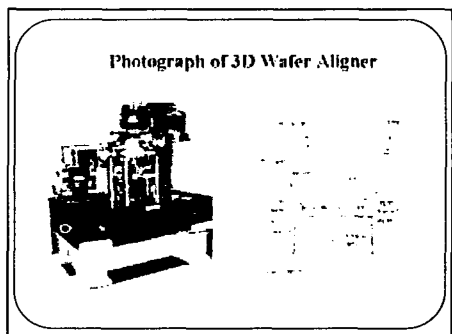

SEM Cross Section of Buried Interconnection
2.5um
55um
2.4um
Poly-Si
Si
SiO2
(a) Si deep trench etching
(b) Filling with Poly-Si


SEM Cross-Sectional View of W Buried Vertical Interconnection
1um
50um
W
Si
W
Poly-Si (500nm)
SiO2 (600nm)

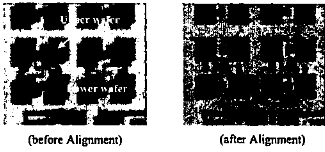

SEM Cross-Sectional View of W Buried Vertical Interconnection and Photomicrograph of Backside after Thinning Wafer
W
930 nm
Poly-Si (500nm)
SiO2 (600nm)
Si
Deposition Temperature 850
Adsorption Time 1.0sec
Reduction Time 15sec
Coverage 99%
SiO2
W


SEM Cross-Sectional View of W Buried Vertical Interconnection with a Diameter of Sub-micron
W
Si


Photograph of Microbumps Formed on Metal Wiring
Metal Wiring
In/Au bump

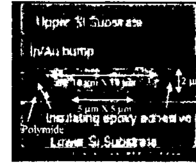

Photograph of 3D Wafer Aligner

Infrared Images Before and After Wafer Alignment

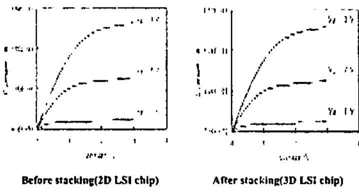


(before Alignment) (after Alignment)

SEM Cross Section After Injecting Adhesive Epoxy

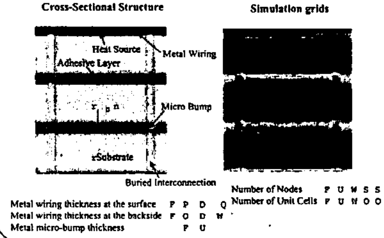


I_d-V_d Characteristics of NMOSFET(L_g=1.5mm) Before and After Stacking

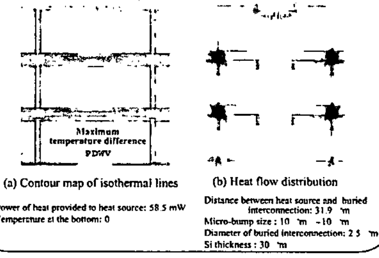


Before stacking(2D LSI chip) After stacking(3D LSI chip)

3D Structure for Heat Flow Simulation



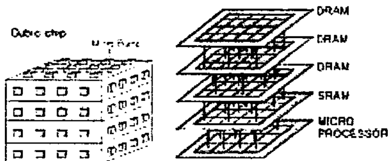
Simulated Heat Flow in 3D Structure



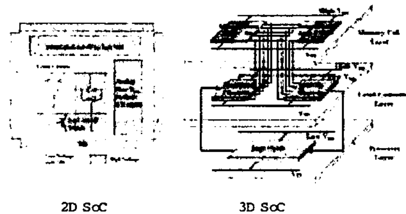
3D Chips and 3D Integrated Systems

- Memory /logic merged 3D LSI
- 3D parallel processor (cubic computer)
- 3D real-time image processing system
- 3D artificial retina chip
- 3D neuron chip
- E
- E

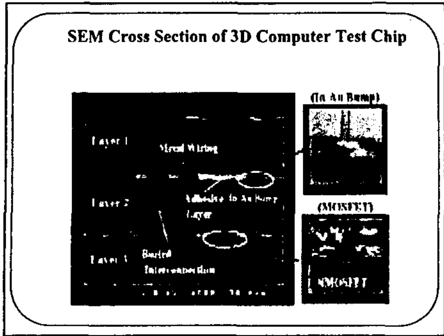
Configuration of Cubic Computer Chip

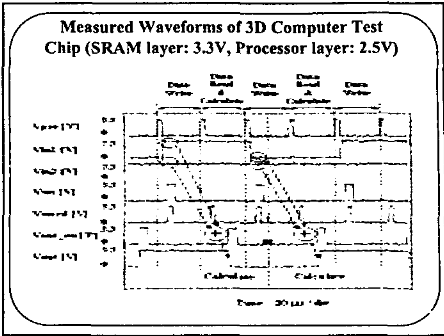


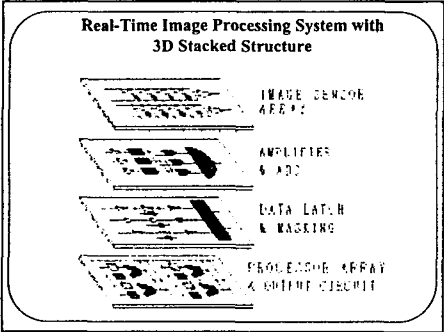
Configuration of 3D Computer Test Chip

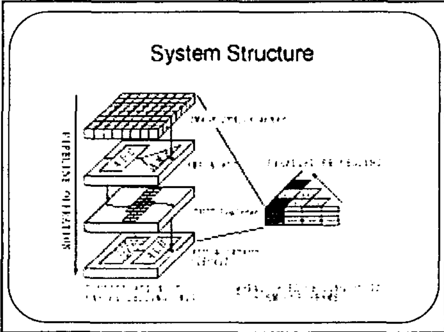


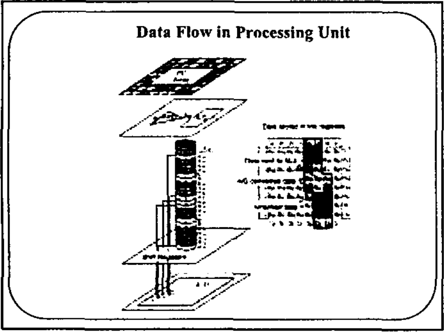
2D SoC 3D SoC

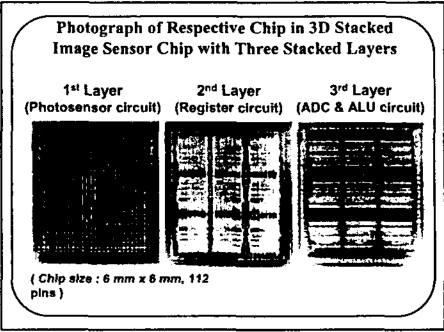

SEM Cross Section of 3D Computer Test Chip
(In Au Bump)
(MOSFET)

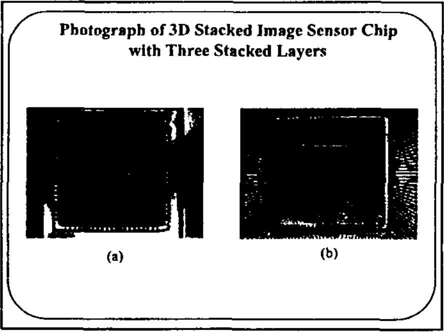

Measured Waveforms of 3D Computer Test Chip (SRAM layer: 3.3V, Processor layer: 2.5V)

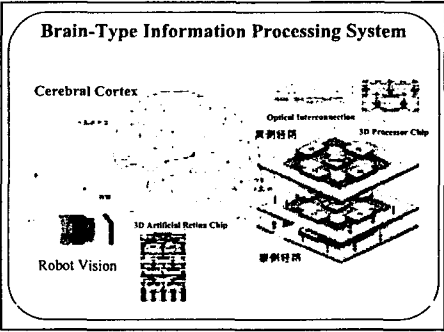

Real-Time Image Processing System with 3D Stacked Structure
IMAGE SENSOR ARRAY
AMPLIFIER & ADC
DATA LATCH & MASKING
PROCESSOR ARRAY & OUTPUT CIRCUIT

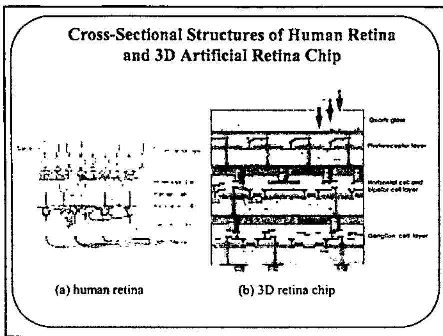

System Structure

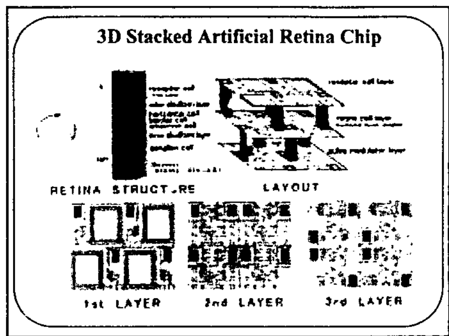

Data Flow in Processing Unit

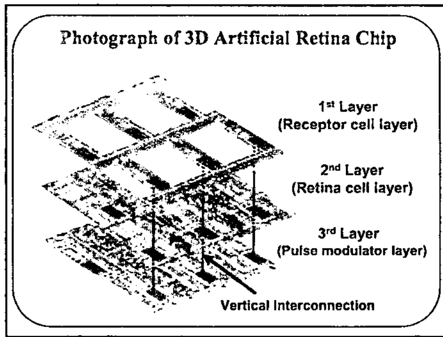

Photograph of Respective Chip in 3D Stacked Image Sensor Chip with Three Stacked Layers
1st Layer
(Photosensor circuit)
2nd Layer
(Register circuit)
3rd Layer
(ADC & ALU circuit)
(Chip size : 6 mm x 6 mm, 112 pins)

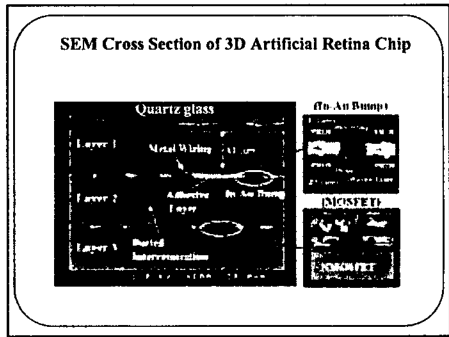

Photograph of 3D Stacked Image Sensor Chip with Three Stacked Layers
(a)
(b)

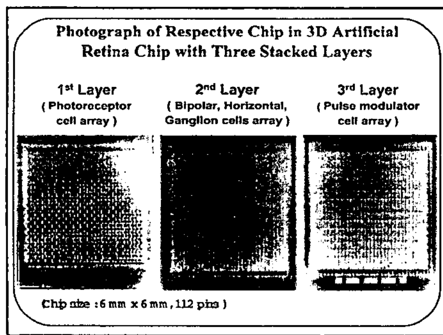

Brain-Type Information Processing System
Cerebral Cortex
Optical Interconnection
3D Processor Chip
3D Artificial Retina Chip
Robot Vision

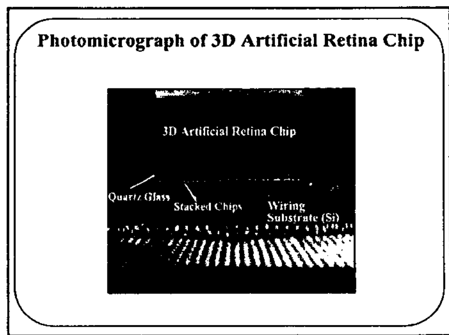

Cross-Sectional Structures of Human Retina and 3D Artificial Retina Chip
(a) human retina
(b) 3D retina chip

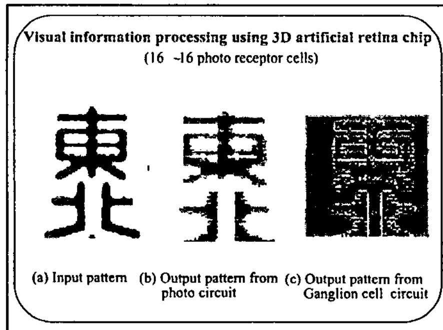

3D Stacked Artificial Retina Chip
RETINA STRUCT.RE
LAYOUT
1st LAYER
2nd LAYER
3rd LAYER

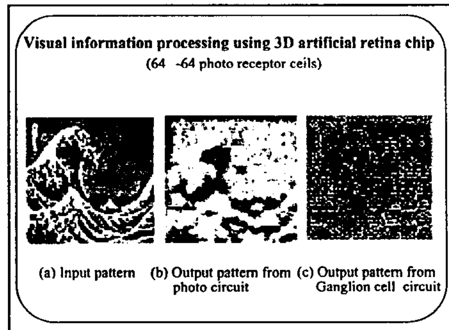

Photograph of 3D Artificial Retina Chip
1st Layer
(Receptor cell layer)
2nd Layer
(Retina cell layer)
3rd Layer
(Pulse modulator layer)
Vertical Interconnection


SEM Cross Section of 3D Artificial Retina Chip
Quartz glass
Metal Wiring
Layer 1
Layer 2
Layer 3
Buried Interconnection


Photograph of Respective Chip in 3D Artificial Retina Chip with Three Stacked Layers
1st Layer
(Photoreceptor cell array)
2nd Layer
(Bipolar, Horizontal, Ganglion cells array)
3rd Layer
(Pulse modulator cell array)
Chip size : 6 mm x 6 mm , 112 pins)


Photomicrograph of 3D Artificial Retina Chip
3D Artificial Retina Chip
Quartz Glass
Stacked Chips
Wiring Substrate (Si)


Visual information processing using 3D artificial retina chip
(16 ×16 photo receptor cells)
(a) Input pattern
(b) Output pattern from photo circuit
(c) Output pattern from Ganglion cell circuit


Visual information processing using 3D artificial retina chip
(64 ×64 photo receptor cells)
(a) Input pattern
(b) Output pattern from photo circuit
(c) Output pattern from Ganglion cell circuit