IC Interposer Technology Trends

Byoung-Youl Min

Sep. 24. 2003

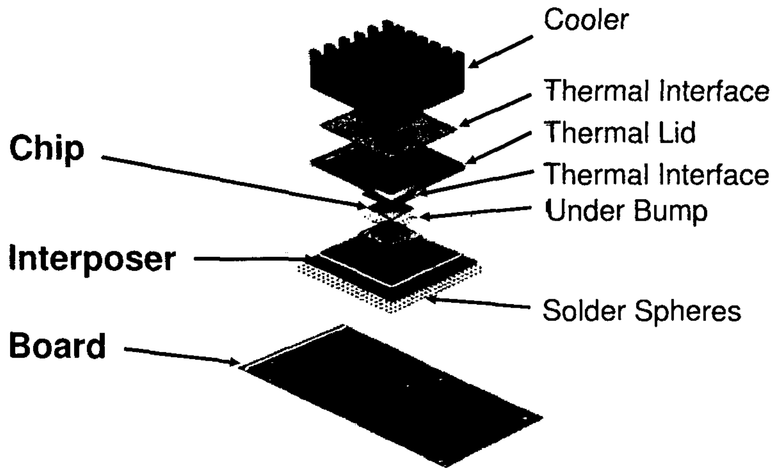
ACI R&D Center
Samsung Electro-Mechanics Co., LTD.

Outline

- Introduction
  - Role of Interposer
  - IC Requirement
- Package Technology Trend
  - SiP
  - 3D Stack
  - FCBGA
- Interposer Technology Trend
  - Via Structure
  - All-layer Build-up Processes
  - Interposer Materials
- New Technology Concept
  - Imprint / MLTS / BBUL
- Summary

Introduction

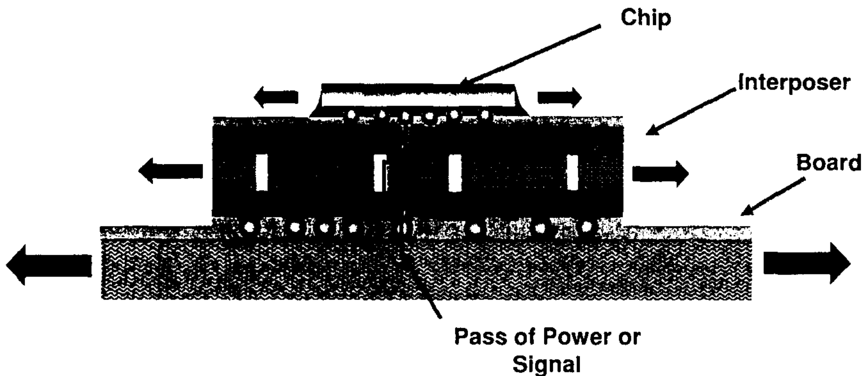
- Interposer Position



SAMSUNG ELECTRO-MECHANICS

Introduction (cont.)

- Interposer Role
  - Scale & CTE matching between IC chip and board
  - Physical & Chemical protection of IC Chip
  - Power distribution & signal I/O
  - Yield & reliability improvement

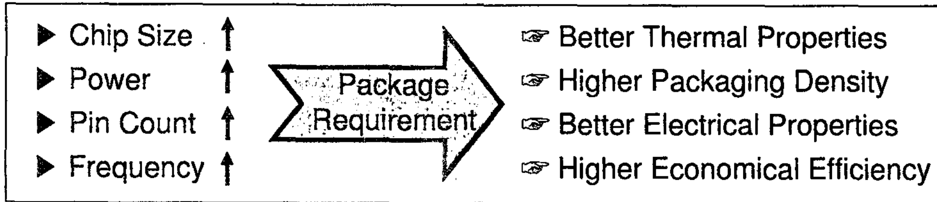


SAMSUNG ELECTRO-MECHANICS

IC Requirement

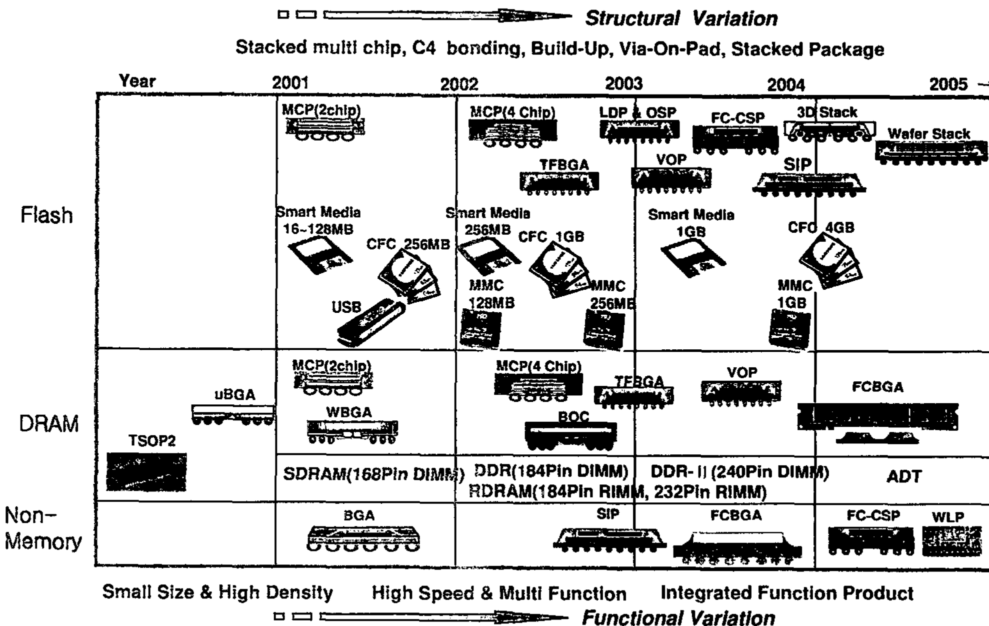
- MPU vs. Memory Requirement

Year		2001	2003	2005	2007
Chip Size [㎟]	MPU	170	186	204	204
	Memory	127	157	175	175
Power [W]	MPU	61	81	92	104
	Memory	1.2	1.6	2	2
Package Pin Counts	MPU	480-1200	500-1452	550-1760	600-2140
	Memory	44-128	44-144	48-160	48-160
Frequency [㎒]	MPU	1,700	3,090	5,170	6,740
	Memory	400	495	612	740



SAMSUNG ELECTRO-MECHANICS

Package Trend



SAMSUNG ELECTRO-MECHANICS

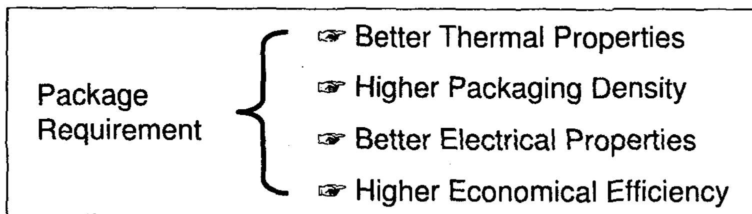
Outline

- Introduction
  - Role of Interposer
  - IC Requirement
- **Package Technology Trend**
  - SiP
  - 3D Stack
  - FCBGA
- Interposer Technology Trend
  - Via Structure
  - All-layer Build-up Processes
  - Interposer Materials
- New Technology Concept
  - Imprint / MLTS / BBUL
- Summary

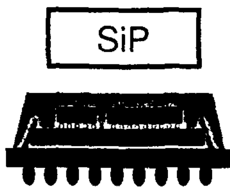
ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

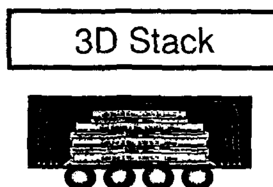
Package Technology Trend



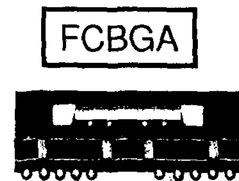
SiP



3D Stack



FCBGA

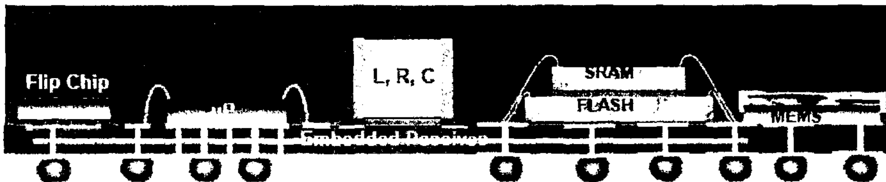


ACI R&D CENTER

SiP (System in Package)

SAMSUNG ELECTRO-MECHANICS

- High & Multi Functional Package
  - ➢ Multiple components on a high density interconnect substrate, realizing a (sub)-system function
  - ➢ Merge of
    - ➢ Logic ICs + memory ICs + Passive components
    - ➢ Different semiconductor substrate (Si, GaAs, SiGe etc..)
    - ➢ Different technology (Electronic, Optical, MEMS etc..)
  - ➢ Modular design approach
  - ➢ Reduced development time, cost

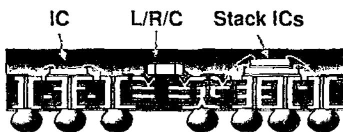


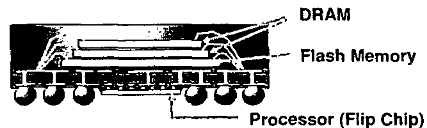
SiP Interposer Requirement

SAMSUNG ELECTRO-MECHANICS

Interposer Total Thickness / Layer Count	0.25 ~ 0.6 mm / 2~4L
Ball Pitch/ Bond Pad Pitch	0.2 mm (Flip Chip) / 0.15 mm (W/B)
Core Thickness	60um
Line/Space	40um / 40um
Via Size (Mechanical / Laser)	150um / 100um
SR Tolerance	35um
Material	BT, High Tg FR 4

(Based on CSP substrate technology)



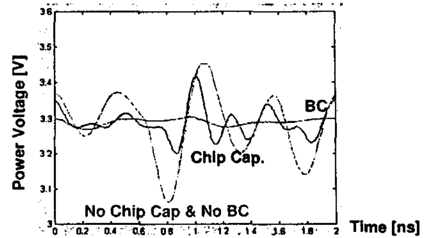


SAMSUNG ELECTRO-MECHANICS

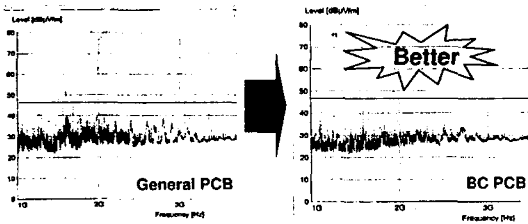
SiP with Embedded Passives

- Embedded Passives

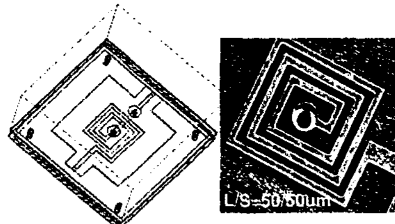
43% Size Reduction by BR&BC (Motorola)



34% Lower Volt. Fluctuation by BC



10dB Lower EMI Noise by BC



Better RF Performance by BL

SAMSUNG ELECTRO-MECHANICS

SiP with Embedded Passives

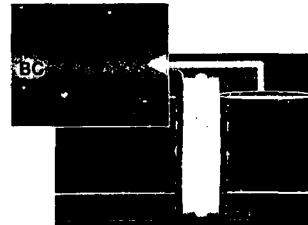
- Embedded Passive Requirement

✓ ***Embedded Resistor PCB***

- ***Better reliability required (Low TCR<200 ppm)***
- ***Laser trimming required (If ΔR<5%)***
- ***Cost & size competition with chip resistor***

✓ ***Embedded Capacitor PCB***

- ***Better reliability required (Low TCC<X7R)***
- ***High speed application (Low parasitic inductance)***
- ***Higher capacitance value required (Cap.>400nF/in^2)***

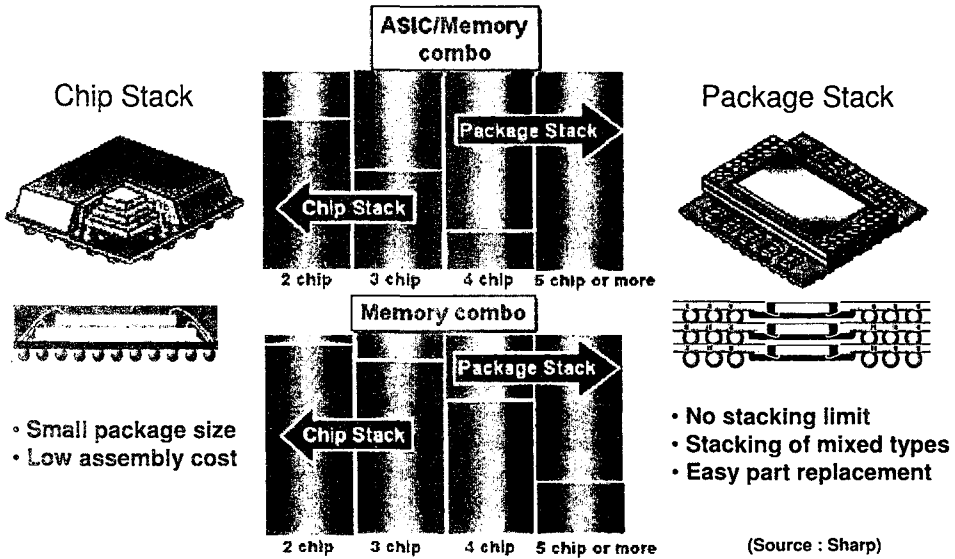


✓ ***Embedded Inductor PCB***

- ***Better RF properties***
  → Q factor>47, SRF: 4.2GHz at 6.8nH
- ***Low dielectric loss required for higher Q factor***

SAMSUNG ELECTRO-MECHANICS

3D Stack Package



- Small package size
- Low assembly cost

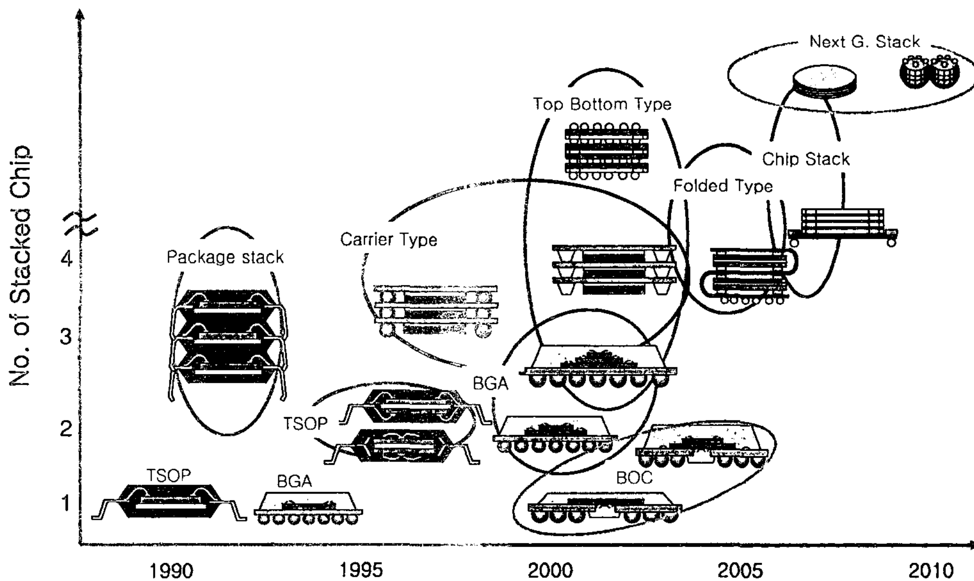
- No stacking limit
- Stacking of mixed types
- Easy part replacement

(Source : Sharp)

ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

3D Stack Package Type



ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

Interposer for 3D Stack Package

Lower Package Profile
- More ICs in same(or thinner) PKG
- Various types of die combination (Flip chip + W/B + Au bump)

	2003	2005
PKG height (4 Chip CSP)	1.2 mm	0.8 mm
Stack-PKGs	3 PKGs	5 PKGs
Ball Pitch	0.5 mm	0.3 mm

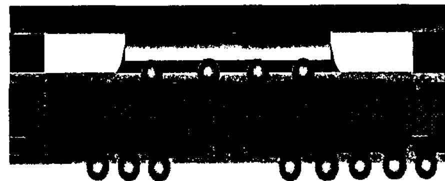
Thinner Interposer
- Thin core material (⇨ 50um)
- Stiff base for flexible & fragile thin die
- Multi layers for complex IC combination

	2003	2005
Core	100 um	50 um
Line/Space	50/50 um	30/30 um
Via Size	100 um	60 um
Solder Resist Tolerance	50 um	35 um
I/O Counts / Layer	100~200/2L	200~300/4L

SAMSUNG ELECTRO-MECHANICS

FCBGA

- Advantage of Flip Chip BGA
  - ➢ High electrical performance
  - ➢ High I/O counts
  - ➢ High packaging density
  - ➢ High thermal performance



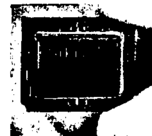
- Applications

PC Chipset

Graphic Chip

Camera Card

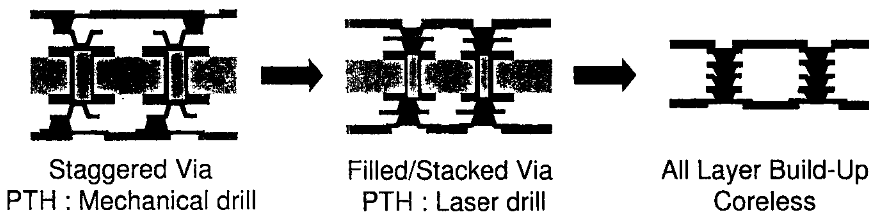
Fast SRAM



SAMSUNG ELECTRO-MECHANICS

FCBGA Interposer Requirement

Year	2003	2005	2007
Line/Space (μm)	25/25	20/20	15/15
μVia diameter (μm)	65	55	45
μVia land diameter (μm)	130	95	70
FC bump pitch (μm)	180	150	130
Dielectric constant	3.4	3.4	3
Dielectric dissipation factor	0.025	0.025	0.01
Stacked via	No	Yes	Yes
Core thickness (mm)	0.8	0.4	Coreless
Embedded components	No	No	Passive



Staggered Via
PTH : Mechanical drill

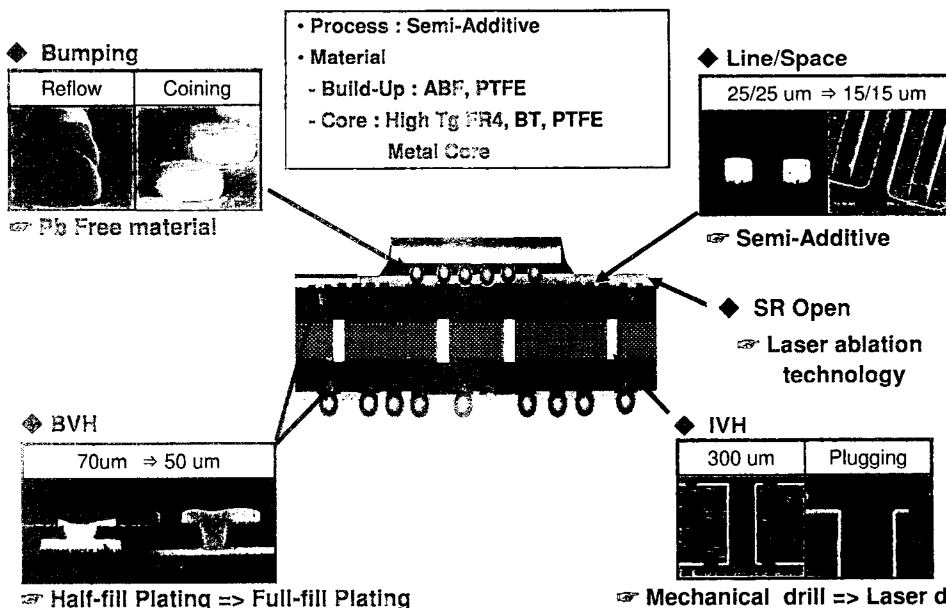
Filled/Stacked Via
PTH : Laser drill

All Layer Build-Up
Coreless

ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

Interposer Tech. for FCBGA



ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

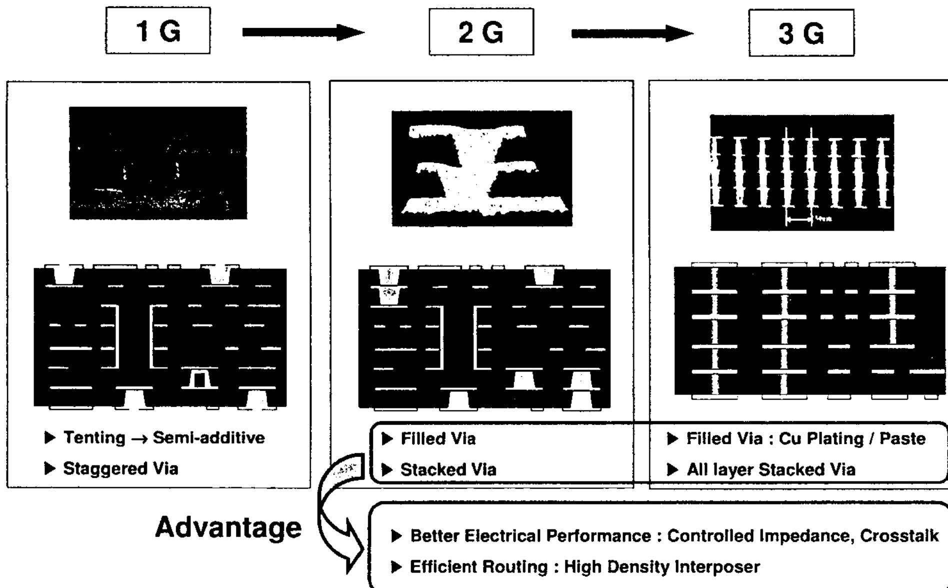
Outline

- Introduction
  - Role of Interposer
  - IC Requirement
- Package Technology Trend
  - SiP
  - 3D Stack
  - FCBGA
- **Interposer Technology Trend**
  - **Via Structure**
  - **All-layer Build-up Processes**
  - **Interposer Materials**
- New Technology Concept
  - Imprint / MLTS / BBUL
- Summary

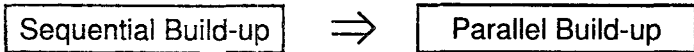
ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

Via Structure



ACI R&D CENTER



All-layer Build-up Processes

Sequential Build-up ⇒ Parallel Build-up

✓ Short delivery
✓ Potentially lower cost (large volume)
✓ High density interposer

- Candidates

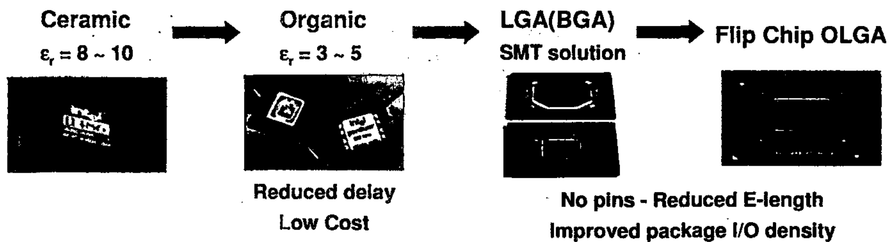
Process	B²it	NMBI	ALIVH	SSP	PALUP	SAVIA
Maker	DTCT	North	Matsushita	Ibiden	Denso	Samsung
Structure	Ag Bump Cu Foil	Cu Bump Cu Foil Prepreg	Cu Paste Cu Foil Prepreg	Cu Plating Cu Foil Bump Plating Adhesive	Ag Paste Cu Foil Cover Lay Thermoplastic	Cu Plating CCL
Key Factor	▶ Ag Paste Printing	▶ Cu BumpEtching : Cu-Ni-Cufoil	▶ Cu Paste Printing	▶ Cu Fill Plaing ▶ BumpPlating : Sn Plating	▶ Ag Paste Printing ▶ Thermoplastic : PEEK,PSS	▶ Cu Fill Plating

ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

Interposer Materials

- Interposer Material Trend for MPU



Reduced delay
Low Cost

No pins - Reduced E-length
Improved package I/O density

(Source : Intel)

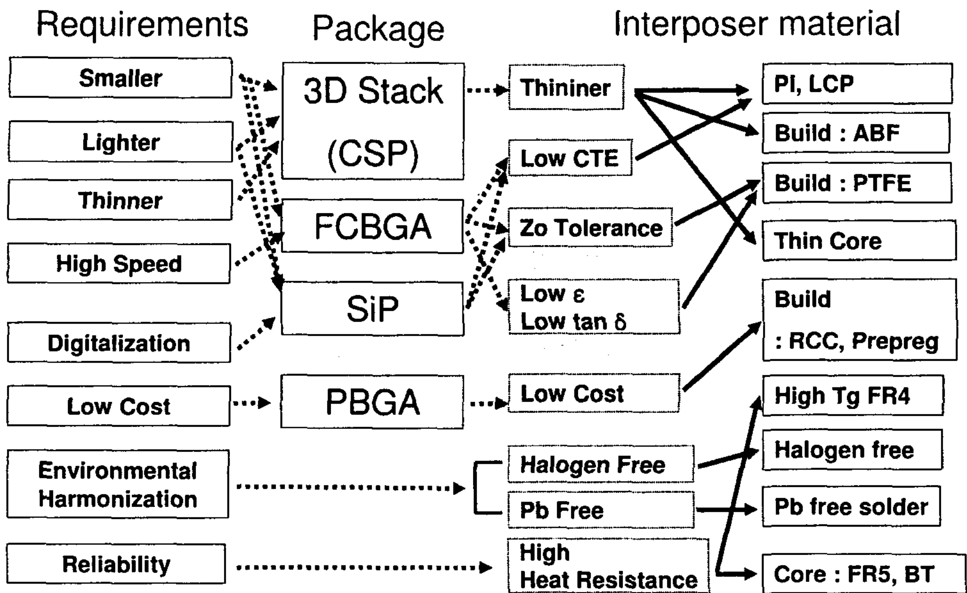
- Organic Material Properties

Item	High Tg FR 4	BT	PTFE	ABF	PI (Flex)	LCP (Flex)
Dielectric Constant @1MHz	4.7	4.6	3.2	3.8	3.4	2.8
Dissipation Factor @1MHz	0.014	0.006	0.003	0.027	0.008	0.001
Tg @ TMA	173℃	180℃	220℃	170℃	320℃	280℃
CTE [ppm/℃]	15	15	19	70	19	4

ACI R&D CENTER

SAMSUNG ELECTRO-MECHANICS

Interposer Materials (cont.)



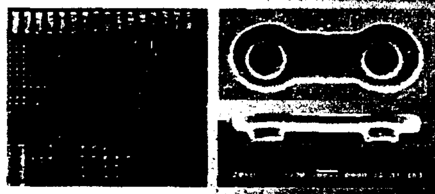
SAMSUNG ELECTRO-MECHANICS

Outline

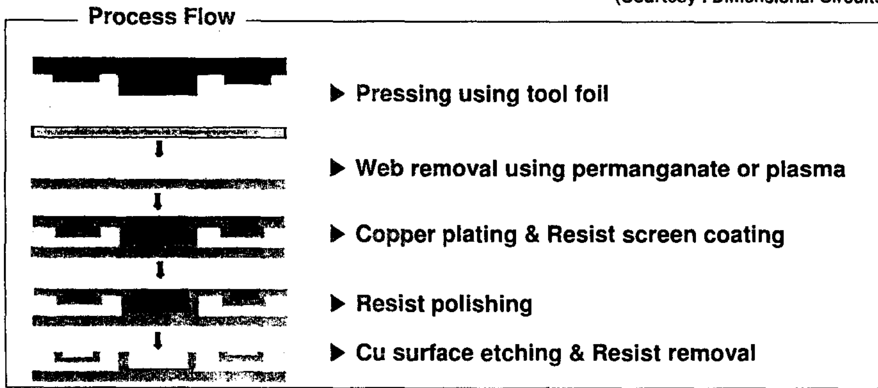
- Introduction
  - Role of Interposer
  - IC Requirement
- Package Technology Trend
  - SiP
  - 3D Stack
  - FCBGA
- Interposer Technology Trend
  - Via Structure
  - All-layer Build-up Processes
  - Interposer Materials
- **New Technology Concept**
  - **Imprint / MLTS / BBUL**
- Summary

Imprint Technology

- Advantage
  - Fine & plat pattern
  - Cheap & fast process
  - 10um line/space possible

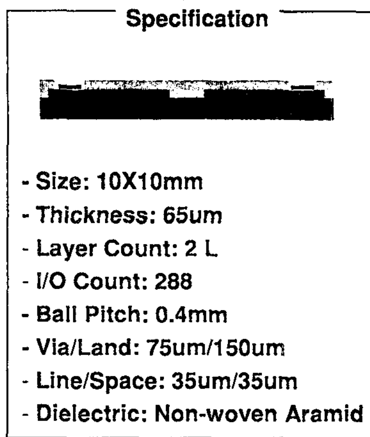


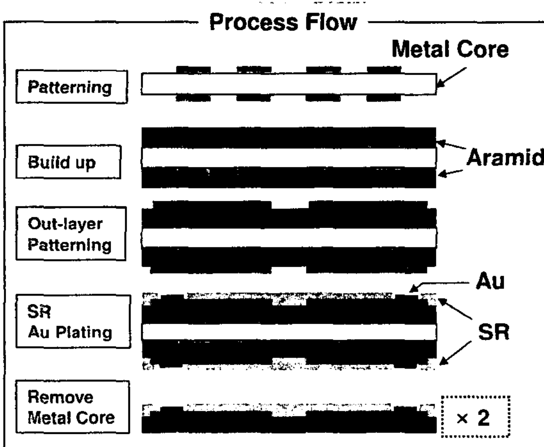
(Courtesy : Dimensional Circuits)



MLTS Technology

- NEC's MLTS Tech.
  - Multi-Layer Thin Substrate
  - Cheap & fast process

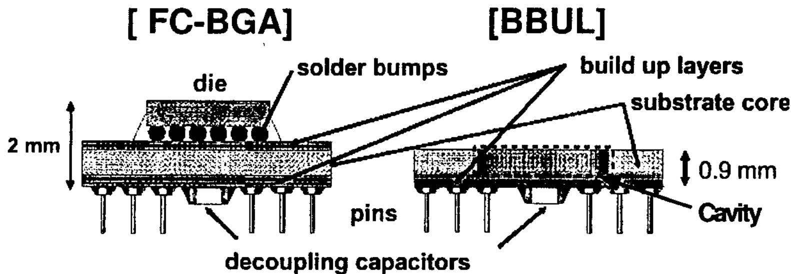




BBUL Technology

SAMSUNG ELECTRO-MECHANICS

- Advantage of BBUL (Bumpless Build Up Layer)
  - ➢ No solder bumps
  - ➢ Smaller pad area
  - ➢ High performance
  - ➢ Thinner / Lighter



Summary

SAMSUNG ELECTRO-MECHANICS

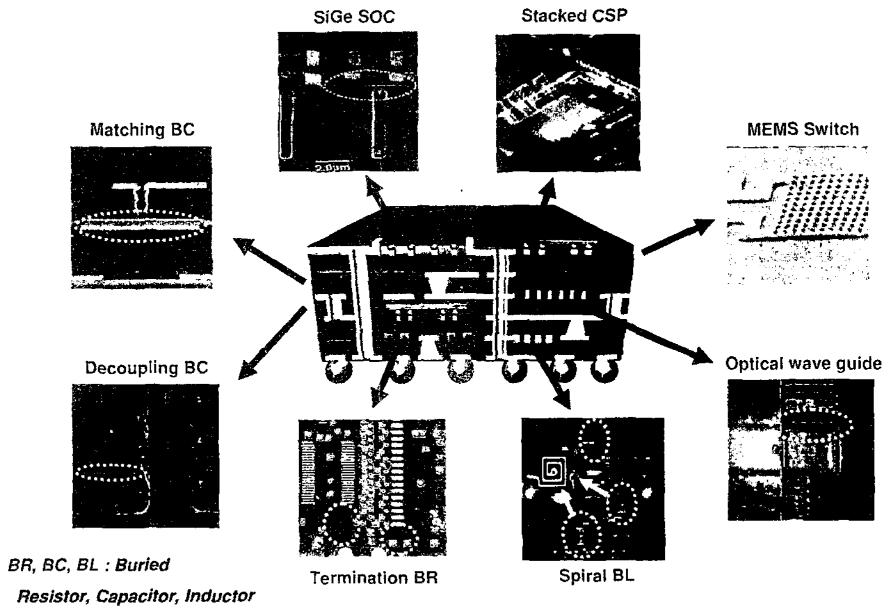
- Package Trend
  - ➢ Memory : Lighter, Thinner, Smaller & High Density
    ⇒ SiP, 3D Stack
  - ➢ MPU : High Pin Counts & Multi-functional
    ⇒ FCBGA

- Interposer Trend
  - ➢ Via
    - Unfilled Via ⇒ Filled Via
    - Staggered Via ⇒ Stacked Via
  - ➢ Emergence of All-layer Build-up Processes
  - ➢ Interposer Material Requirement
    ⇒ Low CTE, Low D_k, Low D_f, Halogen-free

- New Technology Concept
  - ➢ Embedded Passives, Imprint, MLTS, BBUL etc.

Smart Functional Interposer

SAMSUNG ELECTRO-MECHANICS



BR, BC, BL : Buried Resistor, Capacitor, Inductor