

Ceramics Interconnection Initiative Technology Roadmap 2002 & Challenges for Future Growth

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(MIDAS Vision System, Inc.)



IMAPS-CII 2002 Roadmap & Challenges For Future Growth

**Nepcon Korea 2003
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**Howard Imhof – Vice President Marketing
MIDAS Vision Systems, Inc.
Chairman of IMAPS-CII Technology Roadmap Committee**

**Frank Marangell – Vice President Sales
MIDAS Vision Systems, Inc.**

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Overview



Sections:

1. IMAPS – NEMI 2002 Technology Roadmap
2. The Multi Layer Ceramic Markets
3. Yield Management in Multi Layered Co-Fired Ceramics Production

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IMAPS – NEMI 2002 Technology Roadmap

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IMAPS - NEMI ROADMAP - History



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- **First Roadmap from IMAPS was released in 2000**
 - Help from IPC and NEMI
 - Strategy for this edition will be up-dated sections by collective expertise of Ceramic Interconnect Initiative committee.

 - We can only do this with your input!
 - Thank You!

Now released!!

***The IMAPS 2002 Ceramic Interconnect
Technology Roadmap.***

Visit www.midasvision.com to download the IMAPS 2002 Ceramic Technology Roadmap

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IMAPS-CII Roadmap Committee



- Chair: Howard Imhof, MIDAS Vision Systems, Inc.
- Co-chair: Wayne Johnson, Auburn University
- Contributors:

Dan Amey	Dupont
Peter Barnwell	Hereaus Circuit Materials Division
Ted Datri	ADL Corp
Mike Ehler	National Semiconductor
Sam Horowitz	Dupont
Ton Schless	MIDAS Vision Systems
Rick Sigliano	Kyocera
Vern Stygar	Ferro
Jim Lawson	C-MAC/SOLETRON

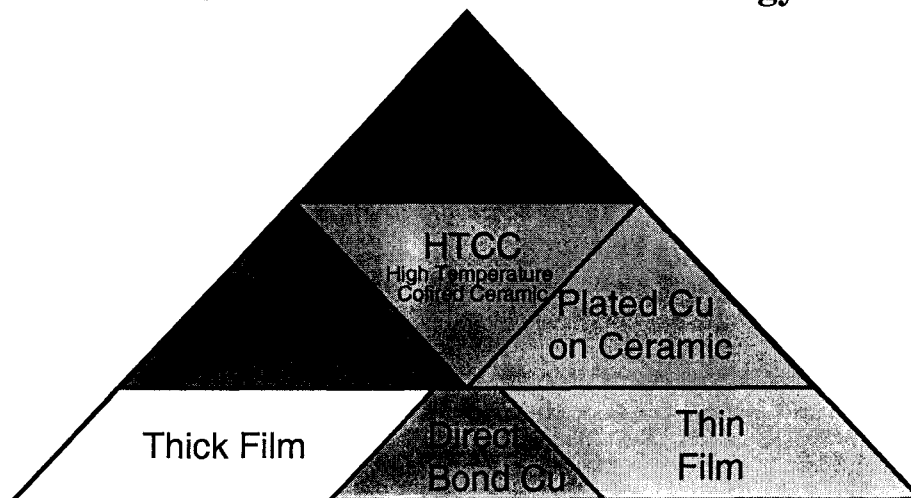
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Ceramic Interconnect Technology



Ceramic Interconnect Technology



Courtesy: DUPONT

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What's Changed in Last 2 Years??



- Ceramic production sheet size has increased
 - from 6.5 x 8.5" to 12 x16"
- "0" shrink green tape
 - Available to 18.0X18.0 inches and larger
- Advances in Photo Processed Materials
 - Reduce dimensions and layer count
 - Line definition to 25 microns.
- Renewed interest in Aluminum Nitride ceramic
 - With compatible material set.
- National Institute for Standards and Technology and University involvement
 - Standard Measurements for Loss Tan data at high frequency.
- Low Temperature Co-Fired Ceramic has demonstrated capability for MEMS architecture.

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CMAC
MicroTechnology

Tying together MCM's, SoC, SoP, and SiP

System-IN-Package

MCM + SoC + 3D package

Substrate is interconnect, has multi-I/O, is passively integrated & is the package

Packaging provides high value-add, becoming part of the system

Electrical, optical, environmental, mechanical

Cost effective rather than value-added

SYSTEM IN A PACKAGE

SOLETRON

Attributes for Enabled Packaging



Packaging must address requirements beyond structural ...

<ul style="list-style-type: none"> • Provide interconnect • Support multiple assembly formats <ul style="list-style-type: none"> – Solder (SMD & Flip Chip) – Resin/Epoxy – Brazing / Welding – Eutectic – Wire bond – Optical Alignment • Integrate circuit elements 	<ul style="list-style-type: none"> • Support Multiple I/O <ul style="list-style-type: none"> – Electrical – Mechanical – Optical – Fluidic – Gaseous – Waveguide – Thermal • Provide Protection <ul style="list-style-type: none"> – Mechanical – Environmental
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Courtesy: C-MAC MicroTechnology – a Solectron Company

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'Z' is not Imaginary in Packaging



Density Measurements in mm² or mm³....

<ul style="list-style-type: none"> • PWB & IC industries: density = XY use of real estate XY measurements reflect interconnect only • Efficient packaging utilizes real estate in the 'Z' direction • PWB vs. Ceramic debate(s) <ul style="list-style-type: none"> – Same arguments, different decade – Dispute is over interconnect <ul style="list-style-type: none"> • PWB is interconnect • LTCC is packaging 	<ul style="list-style-type: none"> • LTCC – cubic packaging <ul style="list-style-type: none"> – MHz & GHz friendly – Hi-density interconnect – High layer counts – Embedded capacity – Unique 3D Features – Cavities & Shelves – Blind, buried and thermal vias – Dimensionally stable – Hermeticity – Becomes the package
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Courtesy: C-MAC MicroTechnology – a Solectron Company

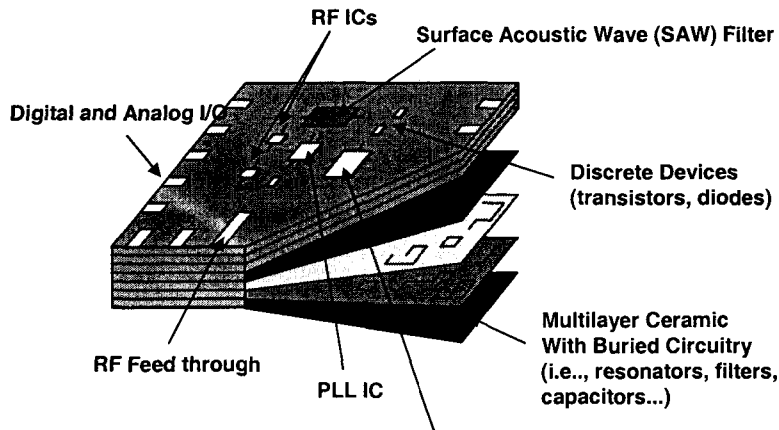
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LTCC Adaptable & Scaleable Features



1. Embedded GHz Friendly Elements
2. High Density 3-D Interconnect
3. Advanced Assembly & Packaging

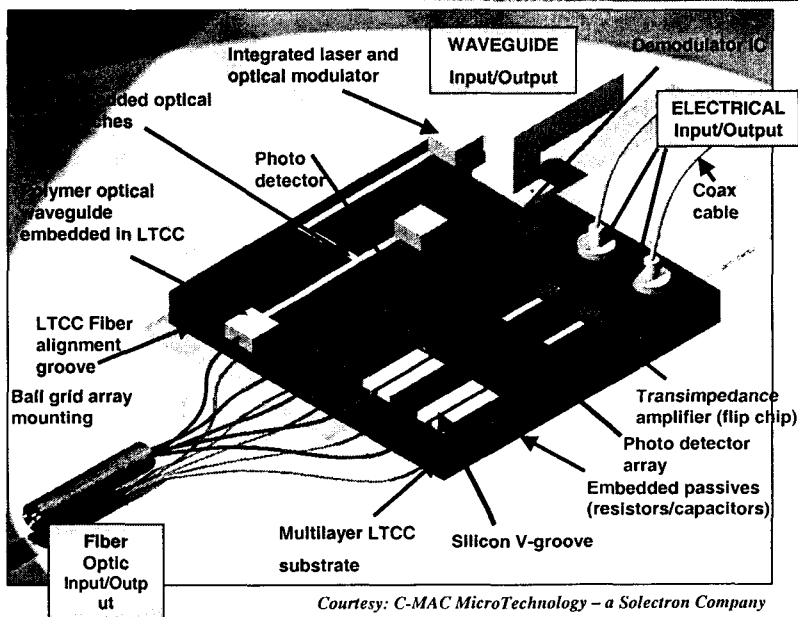


Courtesy: C-MAC MicroTechnology – a Solectron Company **Baseband Processor IC**

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LTCC Module Capabilities



Courtesy: C-MAC MicroTechnology – a Solectron Company

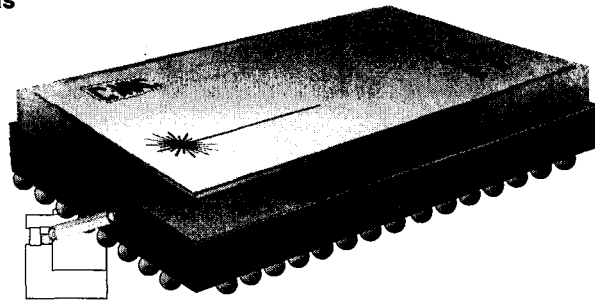
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Opto-Electronic System in Package, SiP



- LTCC tape layer
- Tape layer interconnect w/vias
- Next tape layer
- Tape layer interconnect w/vias
- Embedded resistors
- Tape layer with cavities
- Tape layer interconnect w/vias
- Surface resistors
- BGA I/O
- Embedded fiber ferrules
- Passive add-on elements
- Active electrical & optoelectronic devices
- Wire bonding
- Brazed sidewall
- Hermetic package



Courtesy: C-MAC MicroTechnology – a Solectron Company

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Photo Processes

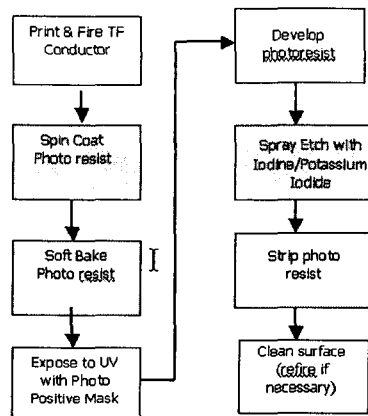
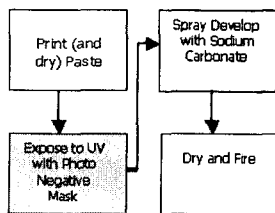


- Processes that reduce dimensions
 - result in denser circuits and reduced circuit layer count

•2 Processes:

•Photo defined or etched

•Photosensitive

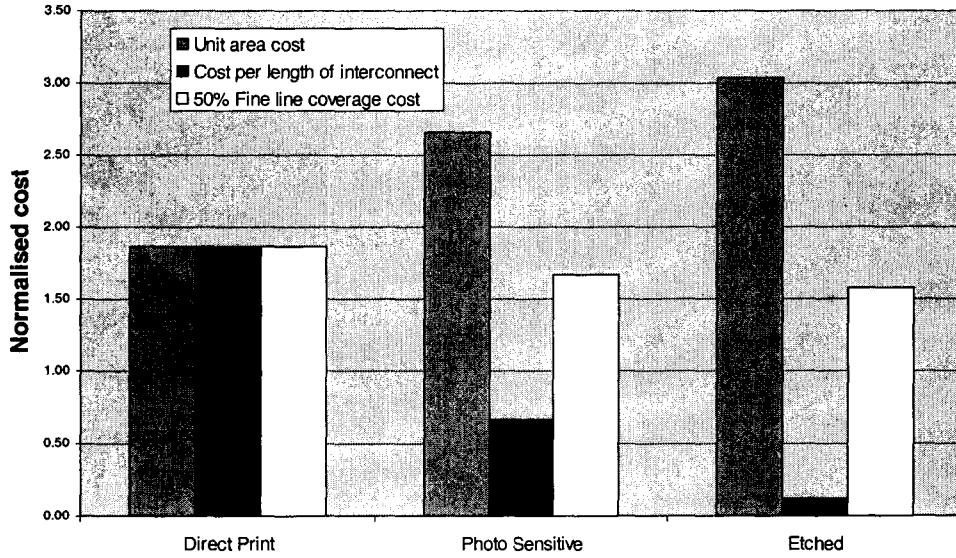


Courtesy of Heraeus CMD

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Substrate cost

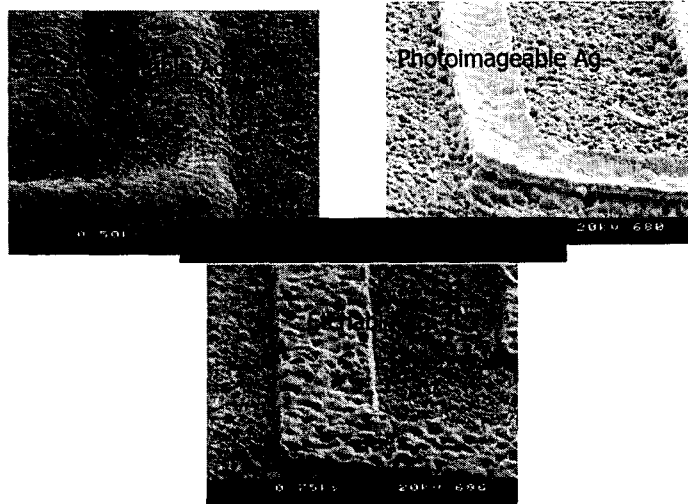


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Comparison of 50 micron Line



Courtesy of Heraeus CMD

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Advanced and Packaging Challenges Short Term – 5 years



- Improved Organic Substrates
 - T_g compatible with Pb free soldering processing
 - Increased wire ability at low cost
 - Improved dimensional control and lower dielectric loss to support
 - Low-cost embedded passive
 - Improved planarity and low warpage at higher process temperatures
 - Low moisture absorption



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Challenges for Ceramics



- Design and Simulation software
 - Embedded Passive “Library”
 - Faster design iteration turn-around
- North American Infrastructure Investment to capitalize on “Killer Apps”
- Reduce cost with Yield Management Solutions
- Equipment set capable of handling large format tape.
- Migration of manufacturing will take capital investment and R&D out of NA
- Education and retention of engineering and technical resources

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Key Educational Programs



- IMAPS Educational Foundation
- Auburn University
 - Wireless Engineering Degree Program
- University of Arkansas, Georgia Institute of Technology
 - Packaging Program
- Florida International University and Penn State University
 - Material Science

.....to name a few.

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Business Issues



- Current downturn has seen significant prototype activity
 - When successful designs reach production volumes it will fuel recovery.
- Significant investment of production fab in China and Taiwan
- Paradigm shift in price of laminates from FR4 to high performance PTFE type for high frequency application make ceramic more competitive in these applications
- Time to Market issues increase with out-sourcing
 - Need to establish supplier relationships at design level
- EMS companies pressure passive component suppliers.
- Discounting by major distributors has stopped, volumes are returning at lower unit pricing
- CII Education Initiative
 - ATWs, Trade Shows, etc.
- .

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Summary



- MLC is no longer a SCIENCE PROJECT
- MLC is a mature technology with global infrastructure
- Ceramic will continue growth in niche markets
 - Demanding performance requirements such as thermal conductivity and uniform electrical properties over a broad frequency range (applications proven to 77 GHz) are required in analogue, digital, RF and Optical applications.

WE HAVE THE TECHNOLOGY

ADOPT IT!!

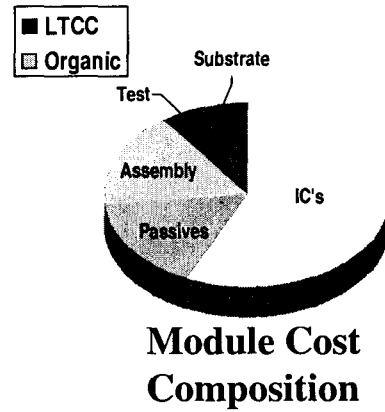
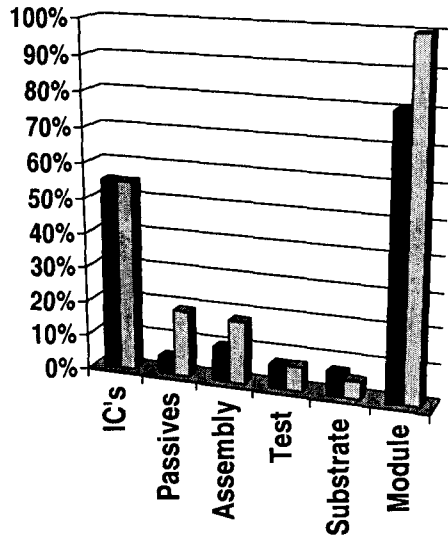


The Multi Layer Ceramic Markets

Cost Comparison: LTCC v. Organic



LTCC is HALF the size, 80% the COST



Source: Ray Brown. IEEE/MTTS2000

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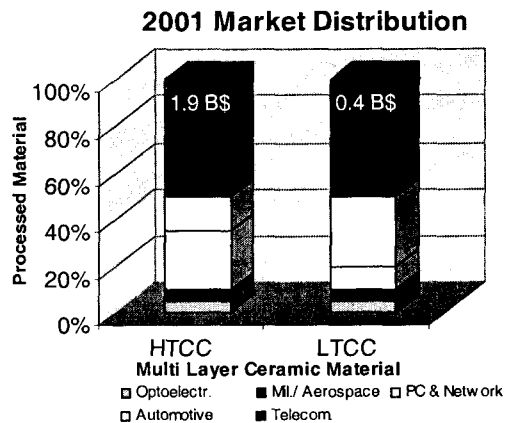
Total Available Market, TAM



- Chip Carriers, MCM and Semiconductor Multi Layer Ceramic Packages

MLC Material Processed in Billion Inch ²						
	2002	2003	2004	2005	2006	2007
Asia	18.30	21.05	24.20	30.25	39.33	53.09
USA	0.30	0.51	0.68	0.81	1.20	1.30
ROW	1.30	1.63	2.20	2.86	4.32	5.53
	19.90	23.18	27.08	33.92	44.85	59.92

Source: Prismark Partners LLC, Japanese MITI, IMAPS, Industry Sources, Paumanok Group, Semiconductor Industry Association



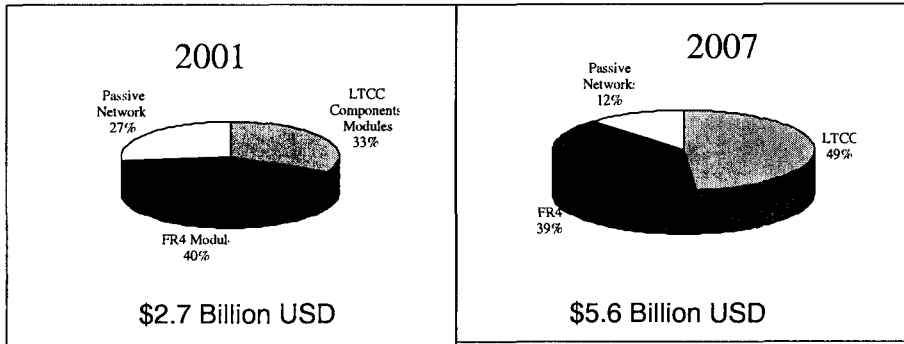
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Global Market Forecasts



- Passive Integration Components & Modules: 2001-2007



Average Annual Growth = 13%

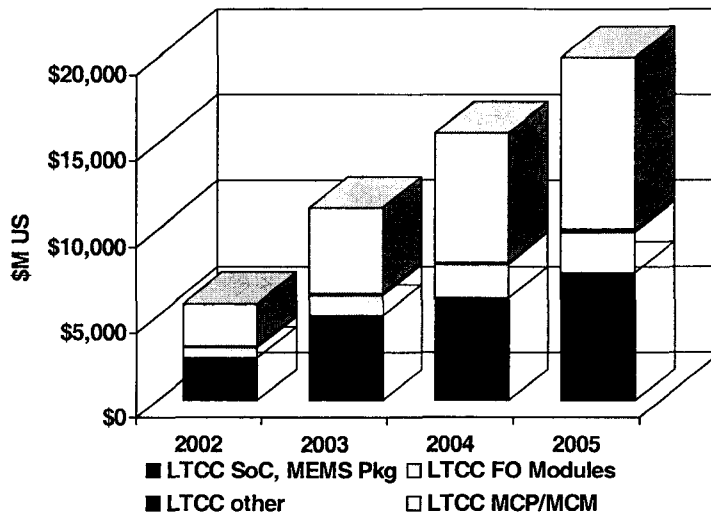
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Market Drivers



LTCC-based SiP Market



Courtesy: C-MAC MicroTechnology - a Solectron Company

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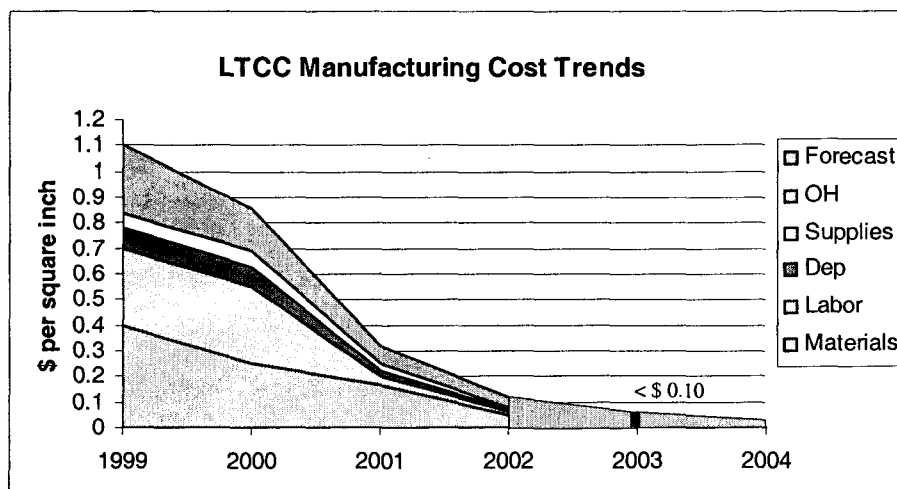
Yield Management in Multi Layer Ceramic Production

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Managing Production Cost

- **Dramatic drop in manufacturing costs is needed to achieve and maintain A competitive position in the world.**



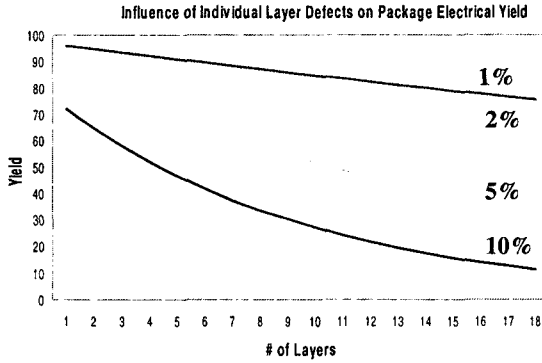
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The Need for Yield Management



Yield Deterioration Due to Layers



% OF DEFECTS AT LAMINATION IN EACH LAYER

Example: 10 Layers
95% yield/layer

Sheet/Layer	Component	Sheet Yield	Total Yield
1		95%	95%
2		95%	90%
3		95%	86%
4		95%	81%
5		95%	77%
6		95%	74%
7		95%	70%
8		95%	66%
9		95%	63%
10		95%	60%

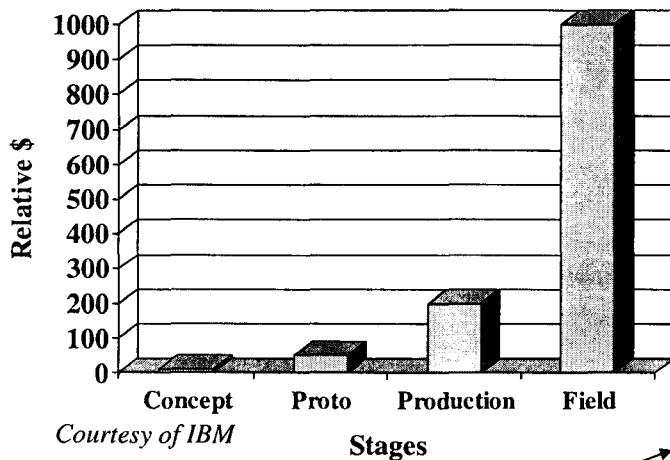
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Prevention of Field Failures



Relative Costs of Catching Mistakes



Courtesy of IBM

Stages

Conductor
Flex Substrate or 'Green Tape' Sheet

MIDAS Finds "Dirty" Opens/Shorts

Conductor Partially Printed or Etched



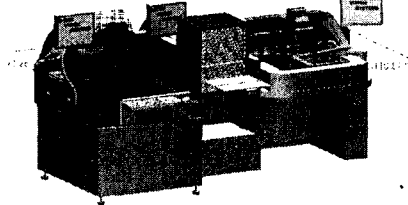
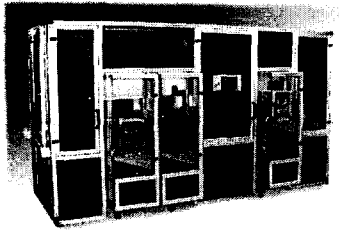
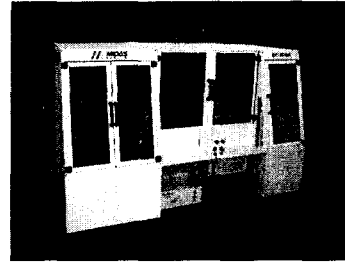
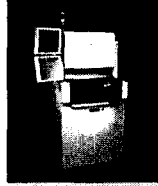
Residual Conductor - Can Pass Electrical Test. "High Field Failure Probability"

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MIDAS inspection and repair modules



- Stand-alone Process Modules
- Islands of Automation
 - w/loaders and un-loaders
- Complete In-line Solutions



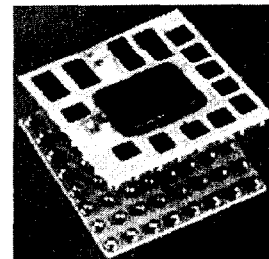
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In-Production Yield Management



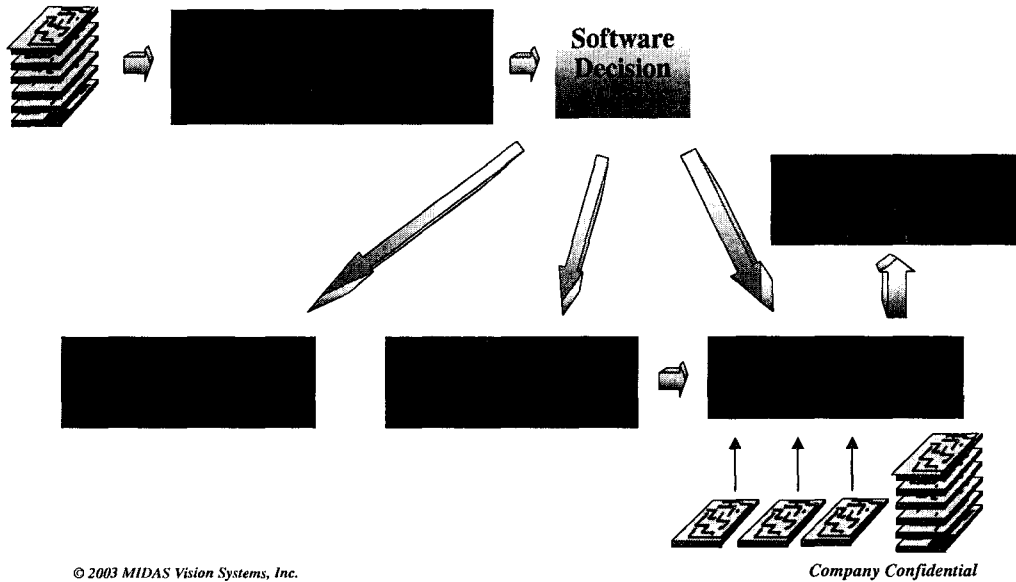
- **Identify Defects and Trends Immediately**
 - Reject or Repair Defects
 - Fix the Problems Before Laminating
 - Eliminate Added Value to Scrap
 - With Known Good Circuit Map Reduce Cost of Electrical Test
 - Guaranteed Increase Electrical Yields
- **Statistical Process Control (SPC)**
 - Characterize Process Capabilities
 - Unbiased Feedback to the Operator
 - Automated Data Collection



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Ideal Production Control Scrap - Repair - Smart Stack



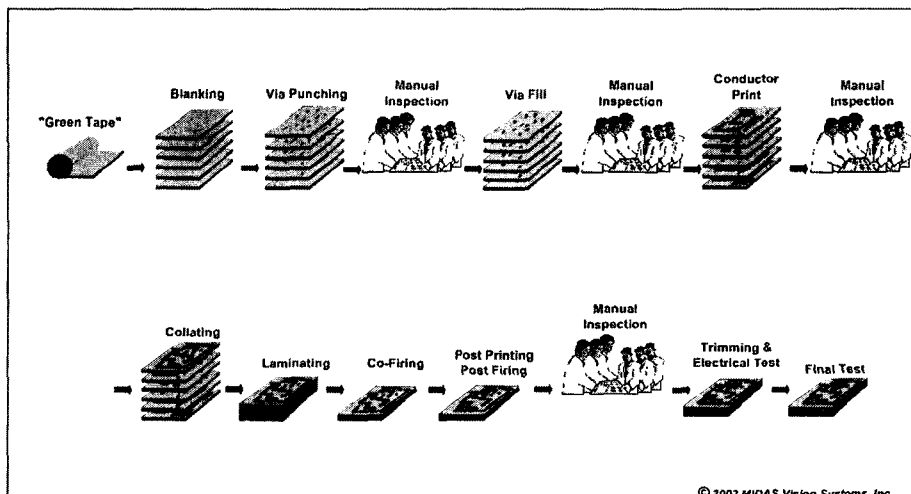
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Process w/Manual Inspection



•Manual Inspection w/o Process Feedback

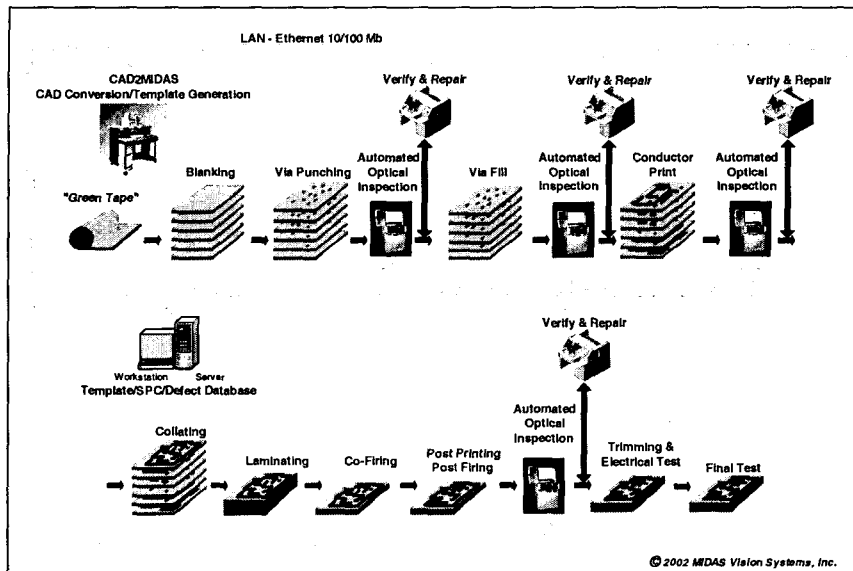


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Yield Management w/AOI



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Data Collection & Report Generation



- **Data Collection**
 - **Defects**
 - Excesses
 - Voids
 - **Material Shrinkage/Stretch**
 - **Screen Stretch**
 - Registration Verification
 - **Feature Measurements**
- **Report Generation**
 - Known Good Circuit Map, KGC
 - Defect Data - Type, Location, Size
 - Measurement - Registration, Line Width, etc

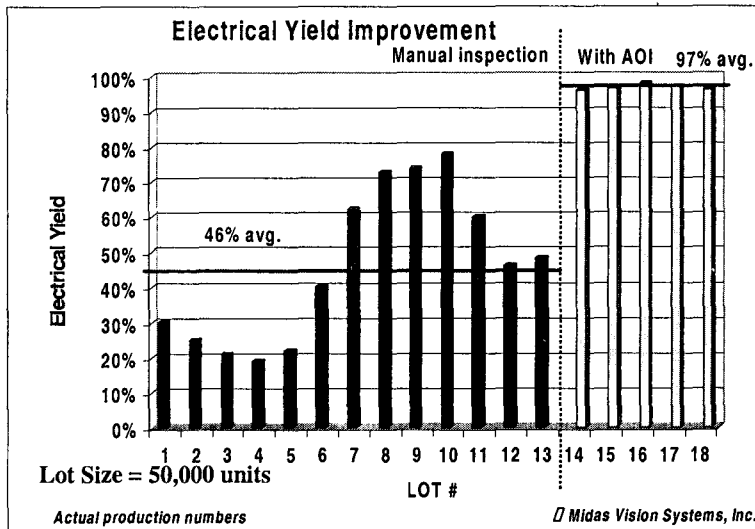
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Maximized Yields



- MIDAS Automated Optical Inspection, AOI, Drives Yield Increase



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Yield Management Results



Incorporating 100% Inspection and Verify & Repair Provides

1. Reduced Cost of Inspection & Supervision
2. Reduced Scrap Material
3. Higher Productivity
4. Lowers Cost of Test
5. Efficient Production Planning
6. On-time Delivery to Customers
7. Increased Quality (Less Field Failures)

**AOI will make you more competitive
in today's global market!**

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Thank You

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The 63 companies of the
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