

Electrical properties of the Porous polycrystalline silicon Nano-Structure as a cold cathode field emitter

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Abstract

The electrical properties of Porous polycrystalline silicon Nano-Structure (PNS) as a cold cathode were investigated as a function of anodizing condition, the thickness of Au film as a top electrode and the substrate temperature. Non-doped 2 μ m-polycrystalline silicon was electrochemically anodized in HF: ethanol (=1:1) mixture as a function of the anodizing condition including a current density and anodizing time. After anodizing, the PNS was thermally oxidized for 1 hr at 900 °C. Then, 20nm, 30nm, 45nm thickness of Au films as a top electrode were deposited by E-beam evaporator. Among the PNSs fabricated under the various kinds of anodizing conditions, the PNS anodized at a current density of 10mA/cm² for 20 sec has the lowest turn-on voltage and the highest emission current than those of others. Also, the electron emission properties were investigated as functions of measuring temperature and the different thickness of Au film as a top-electrode.

1. Introduction

Flat panel display (FPD) is one of the key devices in an information technology (IT) area. There are many different technique to realize flat panel displays such as liquid crystal display (LCD), plasma display panel (PDP), organic light emitting device (OLED), and field emission displays (FED). Among those techniques, it becomes general opinion that FED is most promising technology [1]. FED has been developed for a long time and the electron emission mechanism of FED is based on cathode-luminescence like cathode lay tube (CRT). Therefore, it is said that FED can realize the most natural and clear picture, because one is used to viewing picture on CRT screen.

Main development activities were started on the spindt-type FED [2] but that has still several points to overcome. The spindt-type FED is based on tunneling emission from the sharp tip of the metal under the high vacuum pressure and it is crucial problem to hold high vacuum level in the panel. Also focus electrode may be necessary to gather emitted electrons on the phosphor screen, which also leads to a complex device design higher manufacturing cost.

Various fabrication methods were proposed to overcome previous problems [3][4]. Nowadays, new type of cold cathode, such as Porous poly-silicon Nano-Structure(PNS) was proposed to candidates for field emission cold cathode [5][6] and it is expected that PNS is the newest and the most promising cold cathode because it can emit electron almost vertically to the cathode surface and operate under low vacuum pressure. In addition, PNS can inherit basic FED advantage such as high performance field emitter.

In this paper, we estimated the detail fabrication process and electron emission characteristics of PNS and discuss the potentiality of the application to a cold cathode device for future FPD.

2. Experiment

The PNS was formed on heavily doped N-type <100> Si wafer. Non-doped poly-silicon layer was grown by low-pressure chemical vapor deposition (LPCVD) to a thickness of 2 μ m. Subsequently, poly-silicon layer was anodized in mixed solution {HF (50wt %): ethanol (99.8wt %) = 1:1} as a function of anodizing condition. The various kinds of anodizing condition were summarized in Table I. After anodizing, the PNS was thermally oxidized for 1 hr at 900 °C. And then, the 20nm, 30nm, 45nm thickness of Au films was deposited

Table I. Anodizing conditions used in this experimental

Sample No.	Anodizing Condition	
	J(mA/cm ²)	Time(sec)
#1	5	50
#2	5	60
#3	5	70
#4	10	10
#5	10	20
#6	10	30
#7	20	20
#8	20	30

using E-beam evaporator. In order to ohmic contact, thermally evaporated Al was formed on the backside of Si-substrate. The prepared PNSs were placed into ultra high vacuum (UHV) chamber for measurement of the emission properties. The applied voltage of top Au electrode was varied from 0 to +20V, the anode electrode set above the top electrode and kept at a positive voltage of 300V. The fabricated PNS were analyzed as a function of anodizing condition, measuring temperature and the properties of top-electrode. The distance between top electrode of PNS and the anode glass coated phosphor on ITO (Indium Thin Oxide) was set to 1mm. The diode current and the emission current were measured using the Keithley 237 Source Measure Unit. Figure1 shows the

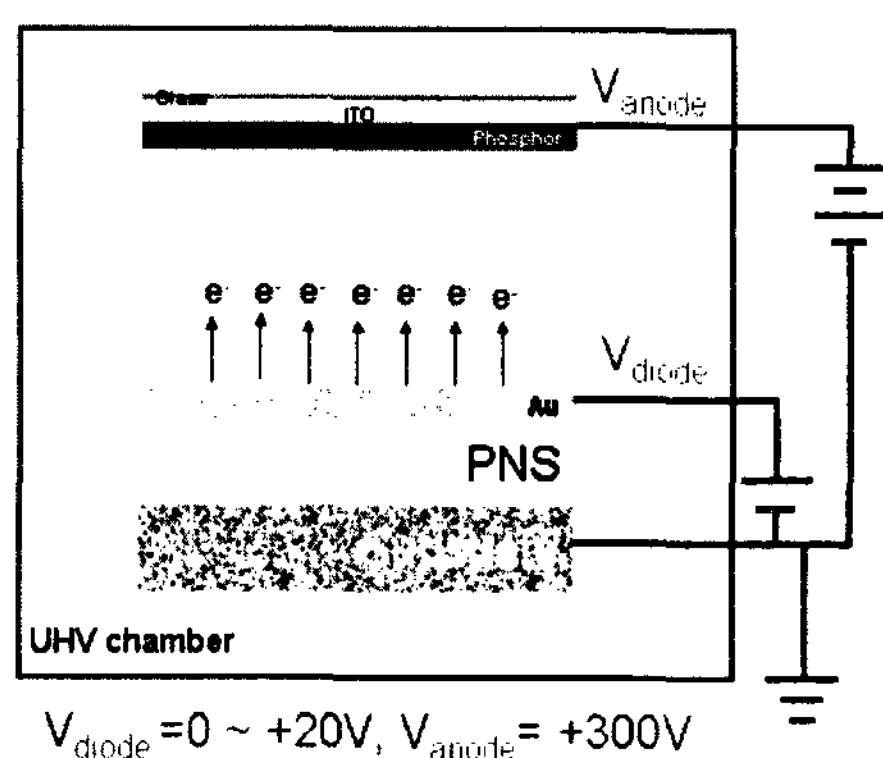


Fig. 1. Schematic diagram of the measurement system.

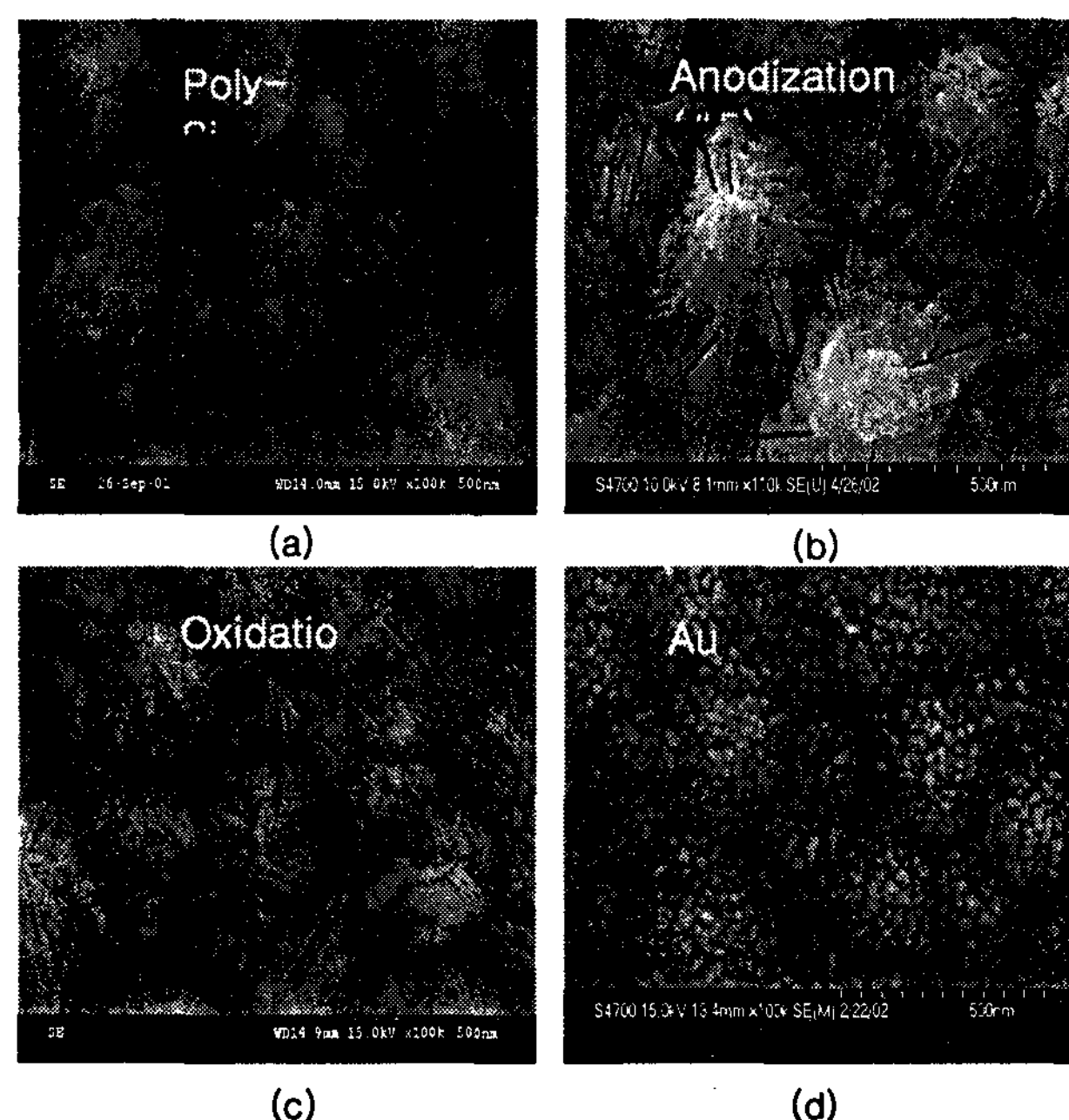


Fig. 2. Surface morphologies of (a) non-doped poly-silicon,, (b) porous poly-silicon nano-structure, (c)oxidized porous poly-silicon nano-structure and (d) fabricated Au porous poly-silicon nano-structure with Au top electrode.

schematic diagram of measurement system.

3 Result and Discussion

In order to examine the surface morphology as a fabrication process step, Scanning electron microscopy (SEM) measurement was performed. As shown in figure 2, SEM is used to analyze the surface morphologies as a function of the fabrication step. The PNS layer formed at a current density of 10mA/cm² for 20sec shows a large number of pores with an average width of several nm. And after oxidation step, we can inspect that the pores width of PNS were decreased by increasing thickness of the oxide.

Figure 3 shows the I-V characteristics of the PNS emitter, which was deposited the 20nm thickness of Au film, under the various kinds of anodizing conditions. Electron emission properties of the fabricated PNS emitters were characterized in an UHV chamber at a base pressure of 1×10⁻⁵ torr. Prior to the test, PNSs were not heated and maintained the same pressure. The anode plate was 1mm above the top electrode and biased to +300 V. The applied voltage to the top Au electrode varied from 0 to +20V. In this figure, we can see that the PNS electron

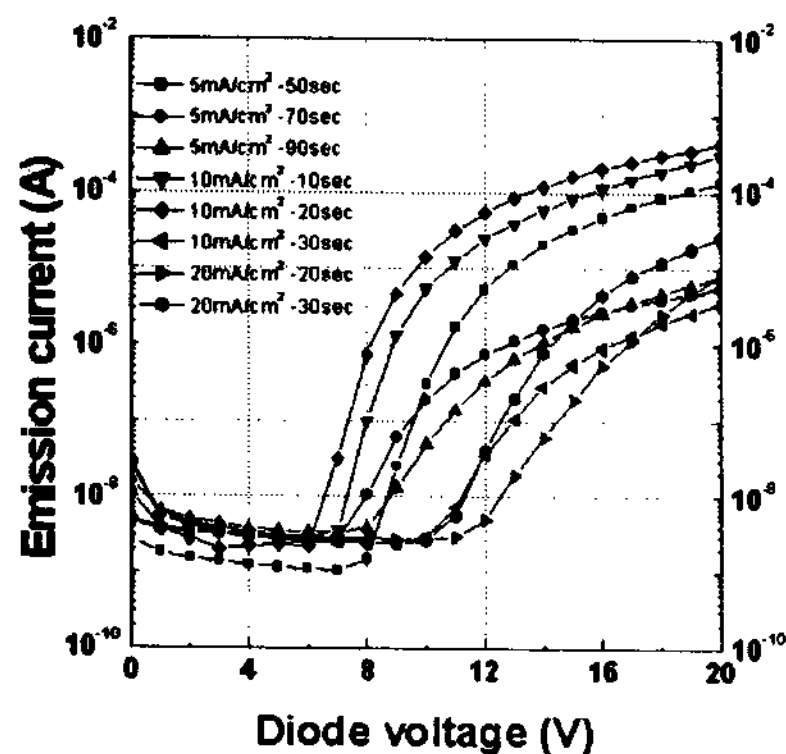


Fig. 3. Current-voltage characteristics of PNS as a function of anodizing condition.

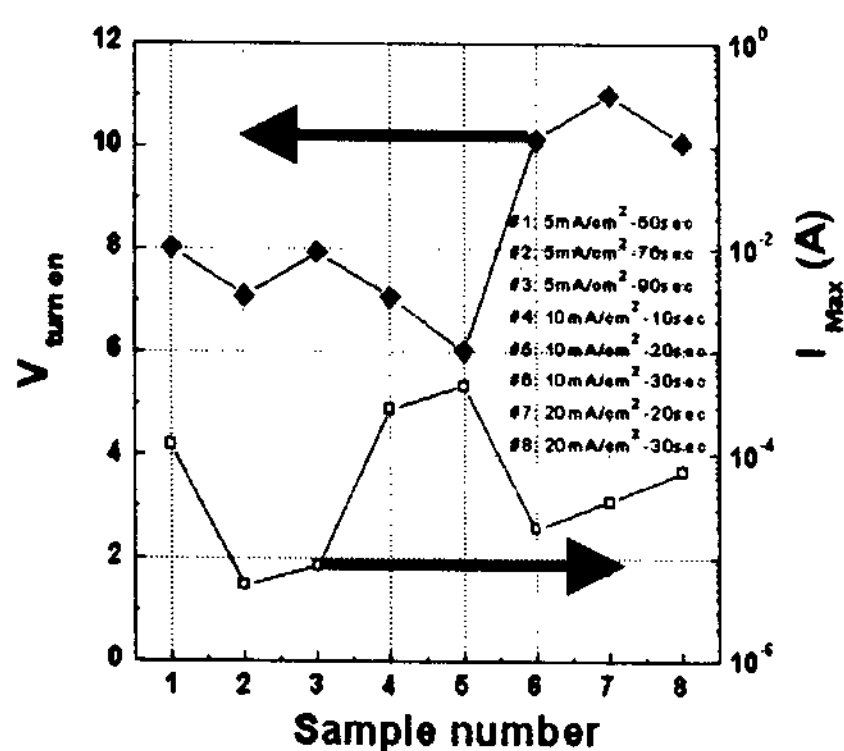


Fig. 4. Turn-on voltage and the maximum emission current of PNS as a function of anodizing condition. The Au thickness is 20nm.

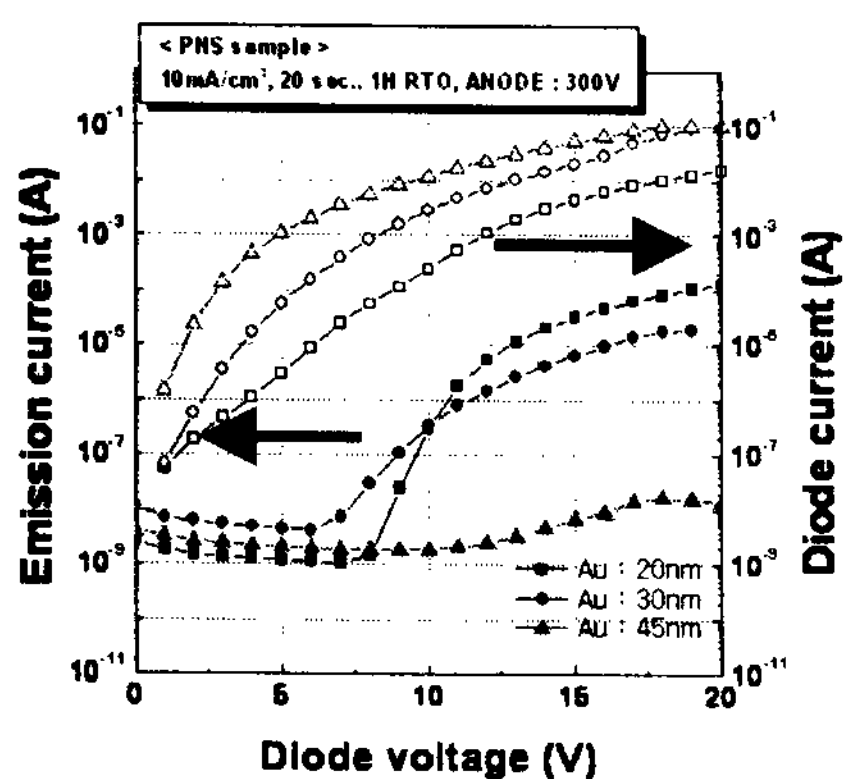


Fig. 5. Current-voltage characteristics as a function of Au film thickness.

emitters fabricated at a current density of $10\text{mA}/\text{cm}^2$ has a lower turn-on voltage and a higher emission current compared to that of others. So, we can

consider that electron emission properties of PNS strongly depend on the anodizing condition.

Figure 4 summarized the turn-on voltage and the maximum emission current of PNS emitter as a function of anodizing condition. We can find that the PNS emitter of #1 and #4 has a higher electron emission current but turn-on voltage is much higher. The PNS emitter of #7 and #8 also has a highest turn-on voltage than that of others. In case of #5, the PNS has the lowest turn-on voltage and the highest maximum emission current compared to that of others. Thus we can confirm that the anodizing condition of #5 is the most effective condition for field induced electron emission.

Figure 5 shows the I-V characteristics of the PNS emitter under the various kinds of Au film thickness. In this figure, we can see that the emission current decreased by increasing of Au film thickness. So, we can consider that the thick-Au film as a top electrode causes a reduction for the emission current.

Figure 6 shows that the I-V characteristics of PNS emitter were measured as a function of the substrate temperature ($<450^\circ\text{C}$). As increase the substrate temperature, the emission current was decreased by the thermally-induced effect. And, we could not measure the emission current at the substrate temperature over 300°C . After measurement, we can see that the emission current was reduced compared to that of initial case.

In general, when two different materials make intimate contact with each other, the diffusion occurs across the interface. The diffusion in semiconductor-related applications precedes the intermetallic formation, grain growth and solid solution formation. And, the diffusion of one species into another strongly depends on the temperature since the phenomenon is a thermally activated process [7]. Thus, from this phenomenon, we can consider the diffusion probability of Au film. And, we can estimate that the top-electrode of thin Au film (20nm) slightly diffused into the oxide. Since it is so, the thermally-induced phenomenon affected to the electron emission property.

Figure 7 shows the light emission pattern on anode phosphor. Au electrode was patterned into 10mm square and it was confirmed that the light emitting image show a good emission uniformity.

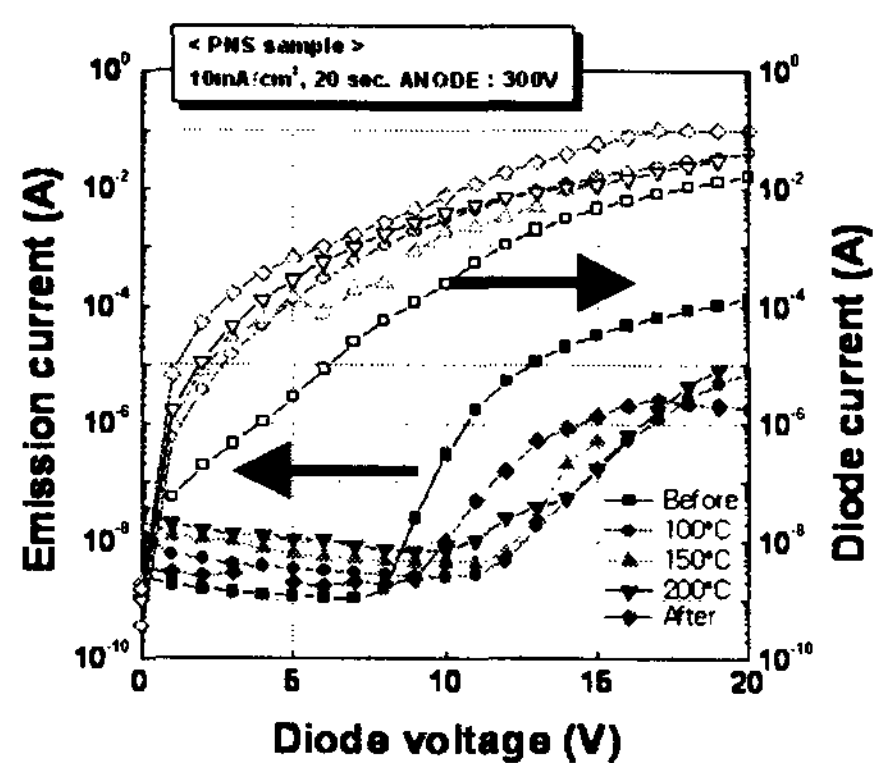


Fig. 6. Current-voltage characteristics of PNS diode as a function of substrate temperature.

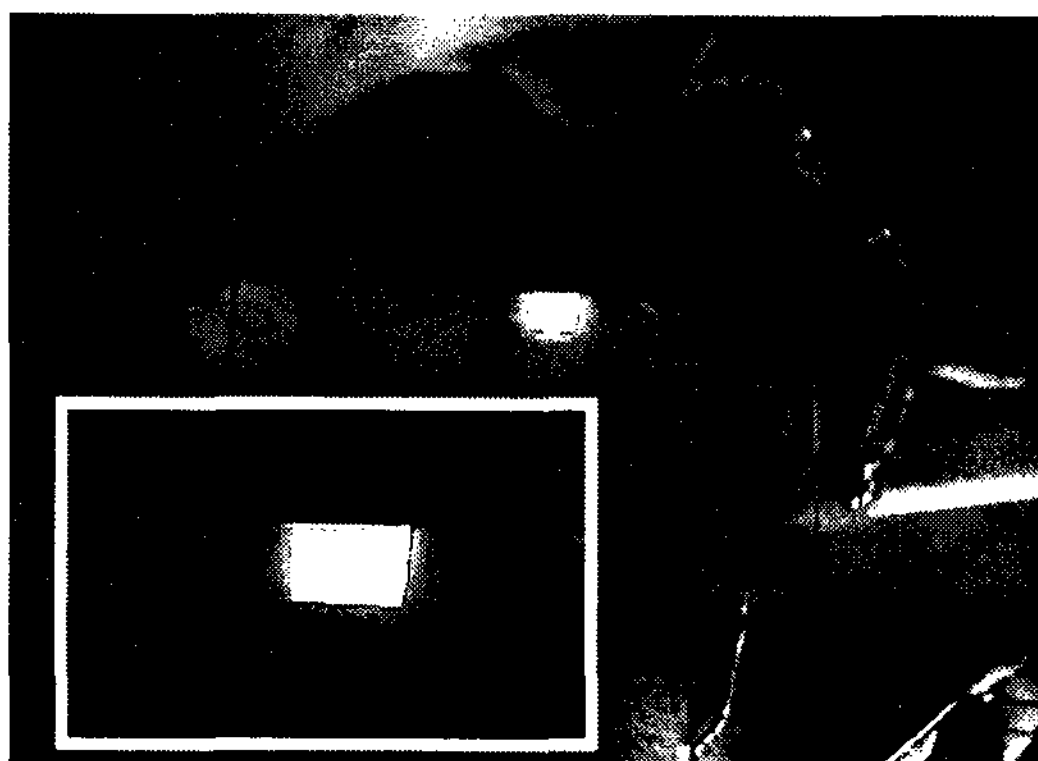


Fig. 7. Light emission pattern of PNS in UHV chamber.

4 Conclusion

The PNS emitter was fabricated on the Si-substrate by means of electrochemically anodizing technique and the electron emission properties were

analyzed as a function of both the measuring temperature and the thickness of Au film. As a result, we can see that the electron emission properties were strongly depended on the thickness of top Au film and the measuring temperature. Also, we can show that the PNS almost vertically emit electron to the anode plate (Fig. 7) and it is easy to fabricate and has low turn-on.

But, we can also obtain that the emission current was decreased by increasing the substrate temperature. From this result, we can estimate that the diffusion in thin films depends on the substrate temperature and may be expected to have a special property between the thin oxide and the thin Au film.

However, it is clear that the PNS shows the potentiality of the application to a cold cathode device for future FPD..

5. References

- [1] B.R Chalamala, Y wei, and B Grand, IEEE Spectrum, April (1998)
- [2] C.A Spint, J.Appl. Phys, 39, 3504(1968)
- [3] N. Koshida, T. Ozaki, X. Sheng and H. Koyama, Jpn.J. Appl.Phys., 34, L705(1995)
- [4] T. Komoda, X. Sheng, and N. Koshida, Mat. Res. Soc. Symp. Proc., 509,187 (1998)
- [5] H. Kim, J. W Lee, IDMC 2002, P273, 2002
- [6] H. Kim, J.W Lee, proceed. SID'02, 365, 2002
- [7] Shyam P.Murarka, "Metallization: theory and practice for VLSI and ULSI",P89, Butterworth-Heinemann(1993)