# LVDS I/O Cells with Rail-to-Rail Input Receiver

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## Abstract

*The LVDS (Low Voltage Differential Signaling) I/O cells, fully compatible with ANSI TIA/ EIA-644 LVDS standard, are designed using a 0.35μm standard CMOS technology. With a single 3V supply, the core cells operate at 1.34Gbps and power consumption of the output driver and the input receiver is 10.5mW and 4.2mW, respectively. In the output driver, we employ the DCMFB (Dynamic Common-Mode FeedBack) circuit which can control the DC offset voltage of differential output signals. The SPICE simulation result of the proposed output driver shows that the variation of the DC offset voltage is 15.6% within a permissible range. In the input receiver, the proposed dual input stage with a positive feedback latch covers rail-to-rail input common-mode range and enables a high-speed, low-power operation. 5-channels of the proposed LVDS I/O pair can handle display data up to 8-bit gray scale and UXGA resolution.*

## 1. Introduction

With increasing demand for higher data throughput in the host-to-flat panel display digital interface, several low-voltage signaling technologies such as LVDS(Low Voltage Differential Signaling), TMDS (Transition Minimized Differential Signaling) were introduced to overcome the bottleneck of conventional CMOS/TTL interface [1-3]. These new I/O schemes give higher signaling speed as well as lower power consumption.

Especially as shown figure 1, LVDS standardized by both TIA/EIA and IEEE gives many advantages [1]: Featuring a constant current-steering, low voltage swing with about 350mV single-ended maximum offers low off-chip power consumption as well as high-speed data transmission over 1Gbps. And differential scheme accomplishes low EMI, robustness of signal to noise sources.

With these advantages, LVDS requires stringent DC electrical specifications. The output signal swing of LVDS output driver is typically 350mV centered at around 1.2V and the receiver should accommodate the

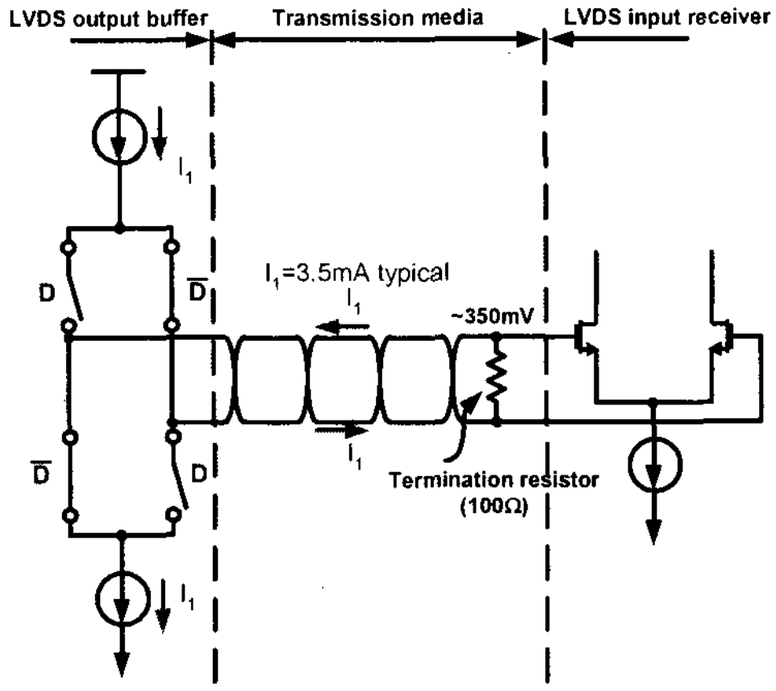


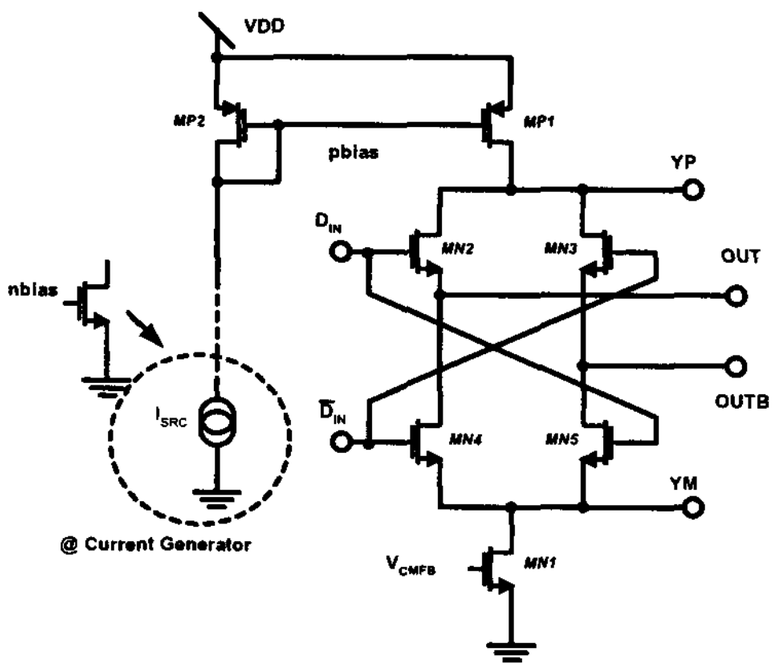

**Figure 1. Basic configuration of LVDS I/O pair via 100Ω differential impedance media.**

input common-mode voltage in the range of ±1V around 1.2V [1]. Since LVDS specification is technology independent, LVDS I/O cells should tolerate PVT variations without additional trimming processes to be compatible with conventional digital CMOS technologies.

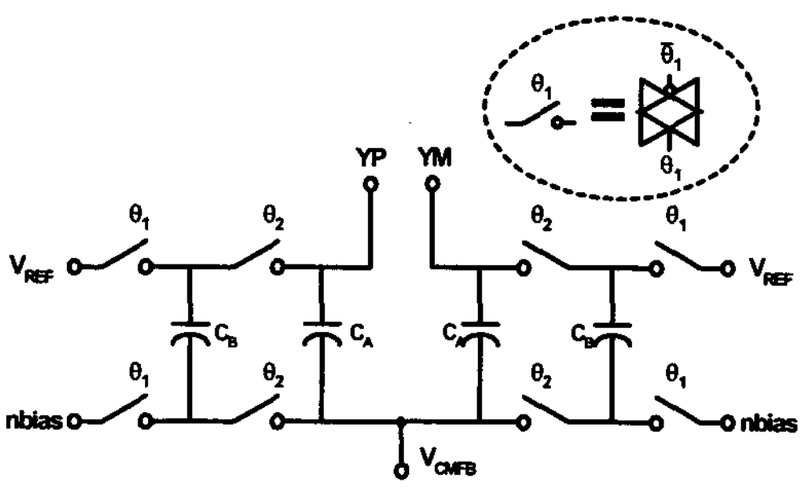
This paper presents newly proposed LVDS I/O cells using a 0.35μm standard CMOS process that satisfy the ANSI TIA/ EIA-644 LVDS electrical specification and have low power consumption.

## 2. Proposed LVDS I/O Cells

Figure 2 shows the proposed LVDS output driver and calibration circuitry. As shown figure 2(a), the LVDS output driver is a push-pull current driver. Constant current source and sink configured by MP1 and MN1 drives the externally terminated 100Ω resistor, which converts 3.5mA current signal into 350mV voltage signal. Binary polarity of differential signal pair is delimitated by set of switches, MN2 through MN5. But in this driver, two differential output node, OUT and OUTB, have high output impedance, which cannot determine the desired DC offset voltage of differential output signals. In [1], the DC offset voltage level and the differential output swing of the LVDS differential output signal should fall within specifications over PVT variations,




(a)




(b)

**Figure 2. The proposed LVDS output driver, (a) Push-pull LVDS output driver and (b) Calibration circuit of (a) to adjust differential DC offset voltage.**

$$1.125V \le |V_{OS}| \le 1.375V \quad (1)$$

$$250mV \le |V_{OD}| \le 450mV \quad (2)$$

where $V_{OS}$, $V_{OD}$ represent the DC offset voltage and the differential output swing at the driver's output, respectively.

One of the schemes to satisfy above requirements is to use common-mode feedback control with resistive divider [4], but it has a drawback of large chip area due to several hundreds kΩ resistors. So we apply a dynamic common-mode feedback to calibrate and control the DC offset voltage of differential output signals as shown in figure 2(b). The differential output swing is adjusted by controlling the gate bias of MP1 in figure 2(a). In calibration circuitry, the DC offset voltage of differential signal is compared with the reference voltage, $V_{REF}$@1.22V. The output signal of calibration circuitry, $V_{CMFB}$, is connected to the gate terminal of the MN1 in figure 2(a), and controls the effective resistance of MN1. In this manner, calibration circuitry forces $V_{OS}$ to $V_{REF}$. Total capacitance in calibration circuitry is less than 2pF, which occupies much smaller area than resistive-feedback. Although discrete-time processing nature of dynamic common-mode feedback requires calibration time, an order of hundreds of nsec, it doesn't matter in a flat panel display interface, a low latency system.

With a LVDS output driver, a LVDS input receiver that converts LVDS signal to CMOS/TTL signal is necessary. Besides high-speed signal conversion, a LVDS input receiver should have a wide input common-mode range specified by [1],

$$0.2V \le |V_{CM}| \le 2.2V \quad (3)$$

where $V_{CM}$ is input common-mode voltage of a LVDS input receiver. A typical receiver with only pMOS gate input pair could not perform satisfactorily with less than 3V supply voltage and typically 0.5V~0.7V threshold voltage of MOS devices. In these reason, an input receiver should have rail-to-rail input common-mode range and high gain-bandwidth product. Figure 3 presents the proposed LVDS input receiver. The proposed input receiver consists of input stage with rail-to-rail input common-mode range, gain-boost stage for high-speed operation and buffer stage. The detail design of the proposed input receiver is described below. Folded cascode input stage, nMOS MN1~MN3 and pMOS MP2~MP3, MP6~MP7, covers upper rail of the input common-mode range. Source coupled differential input stage, pMOS MP1,

MP4~5 and nMOS MN6~MN7, covers lower one. With dual input stage, the proposed input receiver can cover the rail-to-rail input common-mode range. The summing circuit, composed of nMOS MN4~MN5, put

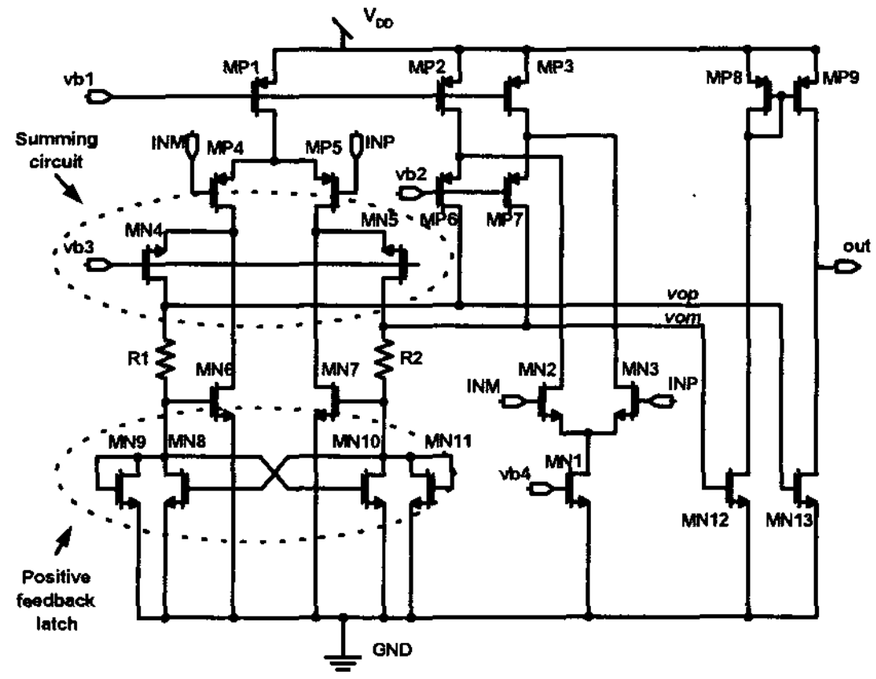
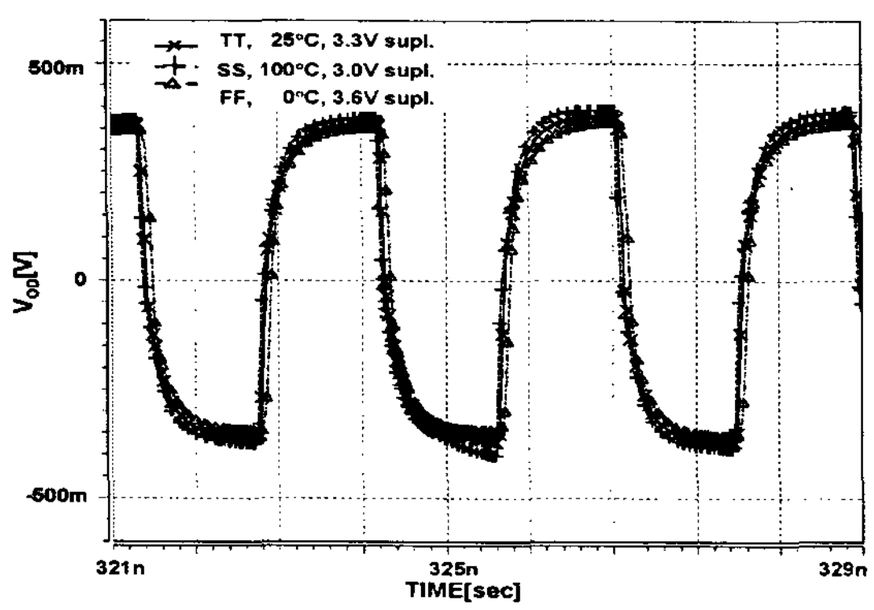



**Figure 3. The proposed LVDS input receiver.**

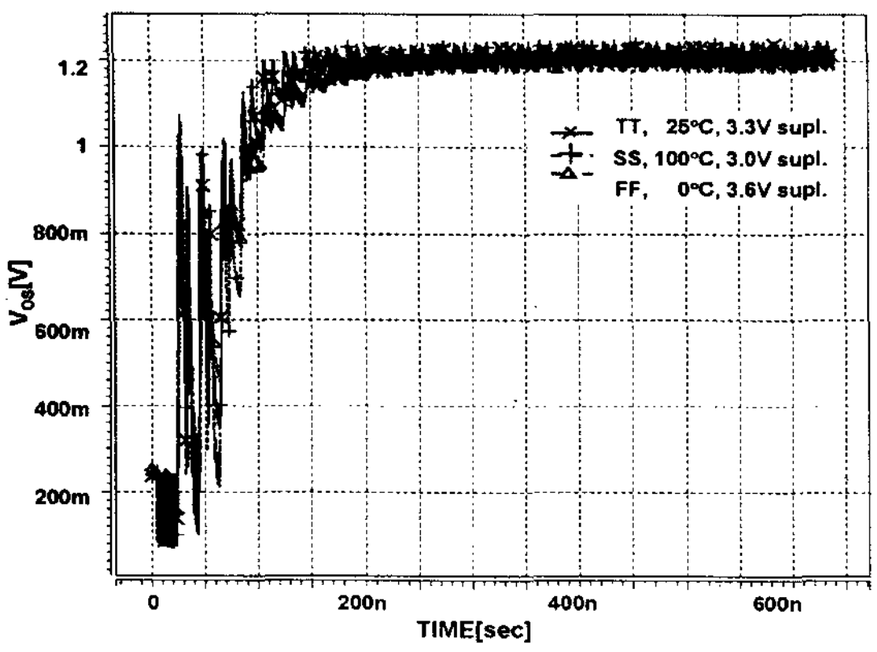
together signal paths from two input stages. Resistors, R1 and R2, with positive-feedback latch, nMOS MN8~MN11, increase gain-bandwidth of this circuit and then increases slew rate of intermediate output voltage, 'vop' and 'vom'. The differential output, 'vop' and 'vom', is converted to single-ended output by the output stage. The output stage, pMOS MP8~MP9 and nMOS MN12~MN13, is a conventional current-mirror type amplifier.

## 3. Simulation Results

The proposed LVDS I/O cells are verified using HSPICE circuit simulator. Spice model for circuit simulation is level 49 of 0.35μm standard CMOS process. The threshold voltages of the nMOS and pMOS are 0.58V and –0.81V, respectively. Power supply voltage is assumed to 3.0V~3.6V.




(a)




(b)

**Figure 4. Simulation waveform of the proposed LVDS output driver, (a) Differential output signal of the driver and (b) Calibration and settling behavior of DC offset voltage of differential output signal ($V_{DD}$=3.0V~3.6V, 0°C~100°C, TT/FF/SS corner model).**

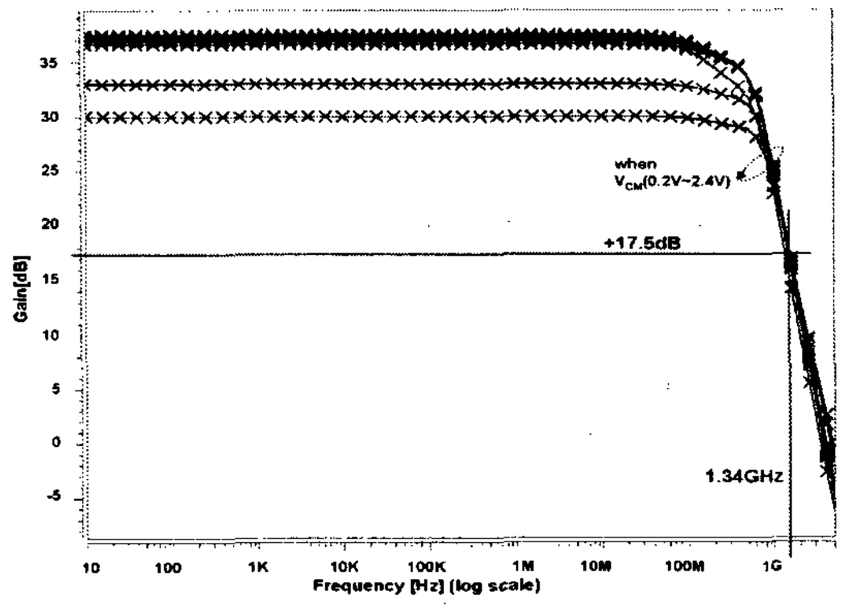



**Figure 5. Frequency response of the proposed LVDS input receiver ($V_{DD}$=3.0V, 100°C, SS model, $V_{CM}$=0.2~2.6V).**

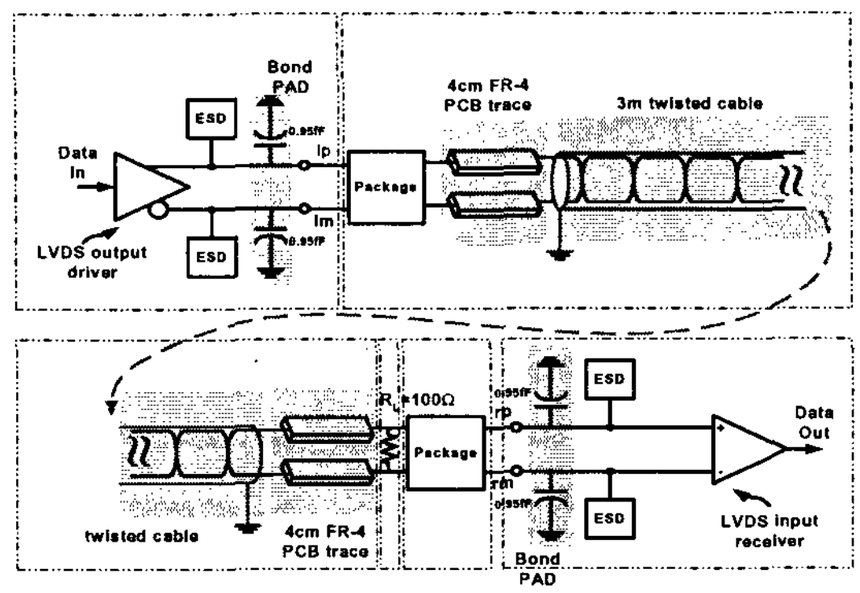



**Figure 6. Channel configuration to measure system performance of the proposed LVDS I/O cells.**

Figure 4 shows dynamic behavior of the proposed LVDS output. Typical value of $V_{OD}$ is about 350mV as shown in figure 4(a) and the $V_{OS}$ is varied 15.6% within permissible range, equation (1), after calibration in figure 4(b).

Figure 5 shows the frequency response of the proposed input receiver. Since minimum +17.5dB gain is required to boost 0.2V to mid-supply voltage, we set the maximum bandwidth of the circuit to above +17.5dB. So the maximum bandwidth of the proposed input receiver is 1.34GHz.

To measure the combined performance of the circuitry with physical signal line, the channel configuration as shown in figure 6 is assumed and modeled. The ESD pattern in [5] is incorporated and TSSOP(Thin Shrink Small Outline Package) is modeled. PCB trace with 4cm-long, FR-4, 50Ω characteristic impedance is designed and modeled with HSPICE *w*-element. 3-meter long, CAT 5 cable is also modeled by HSPICE *w*-element.

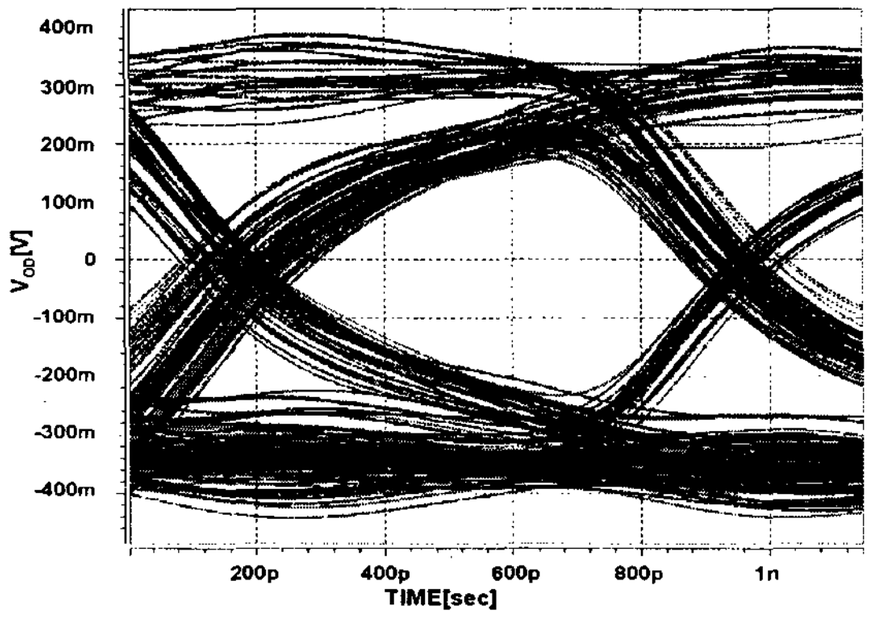
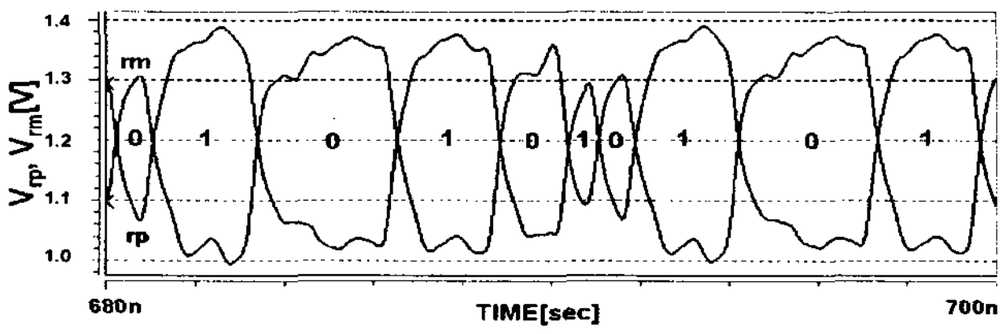
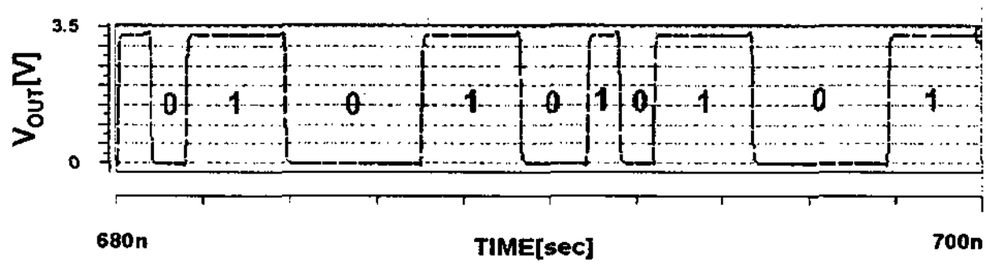



**Figure 7. Simulated eye-pattern at receiver-end (1.34Gbps maximum toggle rate, $V_{DD}$=3.0V, 100°C, SS model).**




**(a)**




**(b)**

**Figure 8. Simulated waveform of the proposed LVDS I/O cells, (a) single-ended waveform at receiver-end and (b) recovered waveform through the proposed LVDS input receiver (1.34Gbps maximum toggle rate, $V_{DD}$=3.0V, 100°C, SS model).**

Figure 7 shows the eye pattern at LVDS receiver-end. The maximum toggle rate of the data is 1.34Gbps.

Figure 8 shows transmitted and recovered signal pattern. Figure 8(a) shows single-ended data pattern at receiver-end. Figure 8(b) shows recovered data through the proposed input receiver.

Table I summarized overall performance of the proposed LVDS I/O cells. A typical LVDS interface for flat panel display consists of 1-clock channel and 4-data channel. So we can confirm that the proposed LVDS I/O cells cover UXGA resolution with 160.1MHz pixel clock frequency.

**Table I. Performance summary of the proposed LVDS I/O cells.**

| Parameter | | Description |
|---|---|---|
| Process | | 0.35μm standard CMOS |
| Minimum supply voltage | | 3.0V |
| Output driver | $V_{OD}$ | 350mV |
| | $V_{OS}$ | 1.2V |
| | $\Delta V_{OS}$ | ±40mV |
| | Power consumption | 10.5mW @ 1.34Gbps transmission with $V_{DD}$=3.0V |
| Input receiver | $V_{CM}$ | 0V~$V_{DD}$V |
| | Sensitivity | < 20mV |
| | Maximum data recovery rate | 1.34Gbps |
| | Power consumption | 4.2mW @ 1.34Gbps data recovery |

## 4. Conclusions

LVDS I/O cells, applicable to UXGA resolution display interface with 8-bit gray scale, have been proposed and verified. Two key circuit techniques, dynamic common-mode feedback and dual input stage, are applied to I/O cells, which guarantee reliable operation with low-power consumption. The proposed cells are designed as a macro-cell and can be combined to standard PAD cell.

## 5. References


[1] *Electrical characteristics of low-voltage differential-signaling(LVDS) interface circuits, TIA/EIA-644*, National Semiconductor Corp., ANSI/TIA/EIA, 1996.

[2] *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), 1596.3 SCI-LVDS Standard*, IEEE Std. 1596.3-1996, 1994.

[3] *Digital Visual Interface Rev. 1.0*, DDWG, Apr., 1999.

[4] A. Boni, *et al.*,"*LVDS I/O Inteface for Gb/s-per-Pin Operation in 0.35-μm CMOS*," *J. Solid-State Circuits*, vol. 36, pp. 706-711, Apr., 2001.

[5] J. H. Lee, *et al.*,"*Improvement in the Second Breakdown Voltage and Current of ESD Protection Devices in a 0.35μm CMOS Process*," *Proceeding of the 8th KCS*, pp. 685~686, Feb., 2001.