BUMPLESS FLIP CHIP PACKAGE FOR COST/PERFORMANCE DRIVEN DEVICES

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ABSTRACT

This paper presents a novel "bumpless flip chip package" for cost/ performance driven devices. Using the conventional electroplating and etching processes, this package enables the production of fine pitch BGA up to 256 I/O with single layer routing. An array of circuitry down to 25-50 μm line/space is fabricated to fan-in and fan-out of the bond pads without using bumps or substrate. Various types of joint methods can be applied to connect the fine trace and the bond pad directly. The resin-filled terminal provides excellent compliancy between package and the assembled board. More interestingly, the thin film routing is similar to wafer level packaging whereas the fan-out feature enables high lead count devices to be accommodated in the BGA format.

Details of the design concepts and processing technology for this novel package are discussed. Trade offs to meet various cost or performance goals for selected applications are suggested. Finally, the importance of design integration early in the technology development cycle with die-level and system-level design teams is highlighted as critical to an optimal design for performance and cost.

INTRODUCTION

The key factors driving semiconductor package development are electrical performance, size, cost, and reliability. In today's high-speed applications, high-end processors require logic devices for stable, clean signal output. This becomes increasingly difficult at higher clock speeds due to the inherent parasitics of packages. Both package and board designs are significant factors in noise generation. Thus, optimizing the design to minimize package parasitics allows system designers to optimize both PCB and system designs for fast clock speed, high bandwidth applications.

A major advantage of flip-chip packages is that they provide shorter connection paths between chip and the external circuitry. With careful design, flip-chip packages often demonstrate better electrical characteristics such as less inductive noise, signal cross-talk, propagation delay and waveform distortion. In addition, flip-chip bonding requires minimal mounting area and weight increase which results in a smaller packaging footprint and lighter package.

While flip-chip technology has tremendous advantages, its cost and technical limitations are significant. For instance, there is the manufacturing cost to form bumps on the chip. Additional adhesive material is normally under-filled between the die and substrate to reduce stress on the solder joints. Finally, the solder bumps are typically tin-lead alloys and lead-based materials are becoming less popular due to environmental concerns.

A wafer level re-distribution scheme provides similar or even higher routing density because it uses the full area of the die. However, wafer level packaging requires "fan-in" routing as opposed to "fan-out" routing. With fan-in routing, the edge of the chip itself defines the boundary of the package. Although current SMT-compatible pitches have come down from 0.8 mm to 0.5 mm along with the emergence of 0.4 mm, for practical reasons, it is not always possible to miniaturize the connection scheme concurrently with die-level and board level improvements. As a result, only a handful of

low I/O devices are able to take advantage of wafer level packaging technology.

DESIGN CONCEPT AND PACKAGING STRUCTURE

Thin Film Re-distribution. To date, most ICs are still designed with peripheral pads with notable exceptions in advanced microprocessors and some SOCs. The peripheral pad pitch is typically 150 μm and is decreasing to 70 μm due to the increasing number of I/Os. While wire bonders can handle this pitch, the high-density boards required to directly connect solder balls with this pitch are far too expensive for commodity products. Therefore, pad redistribution is often required for devices with pad pitch in the 200 μm to 70 μm ranges in order to adopt flip-chip packaging and meet the HDI substrate manufacturing capability with reasonable assembly yield.

Most re-distribution approaches use thin-film dielectrics, polyimide or benzocyclobutene (BCB) followed by vacuum sputtering and semi-additive plating to build the traces for re-routing. Since the plating bus is vacuum deposited and photolithography is processed at the wafer level, it is difficult to lower manufacturing cost effectively.

A more economical way of fabricating fine line traces is to avoid expensive vacuum processes altogether. In other words, the thin film process can be simplified from sputtering-plating-etching steps to plating-etching steps if a plating bus already exists. This can be easily achieved by using copper as the carrier material as it is electrically conductive. Copper plate is widely used in the lead-frame manufacturing. However, in lead-frame, copper is stamped or patterned-N-etched to form the leads. Due to the thickness of copper (e.g. 5, 6 and 8 mils) and isotropic wet chemical etching, achieving ultra-fine circuitry, which is compatible to the normal bonding pad pitch, is impractical. Wire bonding is therefore needed to bridge the "very last millimeter" between bond pads and the metal leads. However, using the additive process such as plating on the copper plate, 50 μm line/space resolution can be easily achieved with 25 μm dry film resist. This is a common practice in most of the lead frame makers. When thin dry film resist (e.g., 12.5 μm) or liquid resist is used, advanced lead-frame makers can provide line resolution in the range of 25 um or less. Of course, fine line circuitry can be achieved by etching thin copper foil with polymer tape support such as TAB. However, issues associated with next level interconnection and board level reliability, have greatly limited its design options.

Fig. 1 shows the fine line Ni/Cu traces plated on the copper carrier with 50μm line/space design rule.

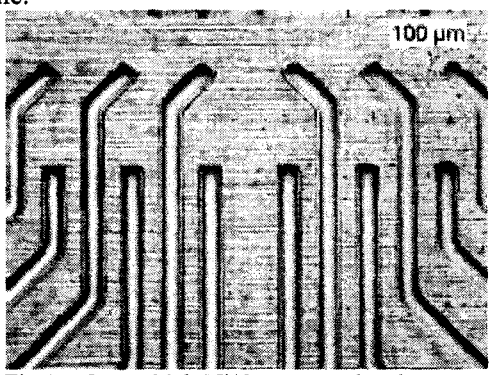

Fig.1. 15 um thick Ni/Cu traces plated on copper carrier

Flip Chip Attachment. Conventional flip-chip bonding involves flipping the chip and re-flow of pre-formed solder bumps located on the chip to wet the corresponding bond sites on the substrate. After the solder cools down, it solidifies to form a series of solder joints between the chip and the substrate. With the self-alignment properties of the solder bumps on the flipped chip, a bump can theoretically be off the pad by as much as 50% and during re-flow, the surface tension of the many solder bumps will pull the die to its proper location. However, for smaller bumps or no-flow under-fill approach, the self-alignment properties become less pronounced because of reduced surface tension effect.

High Density Interconnect Substrate Substrates for flip chip attachment typically require routing line/spaces in the range of 100 탆 (4 mils). Leading edge offers 50 탆 (2 mils) together with build-up-layer or blind and buried vias. BT resin laminate, high Tg FR4, FR5, polyimide-based tap have all been adopted in the various package structures. Although these approaches are relatively lower cost and easier to singulate than specialty substrates like thin film or ceramics ones, they are not as cost-effective as conventional metal-based lead-frames in general.

Handling substrates that come with a wide range of mechanical tolerances is another major obstacle in assembly operations. Metal lead-frames offer very tight tolerances whereas organic substrates have much lose control due to the heterogeneous nature of the multiple resin/glass laminates. Thermal coefficient of expansion (TCE) mismatch between copper, polymer and glass fibers as well as the difference in Young's modulus of these materials greatly induces deformations of the interposer during panel fabrication as well as assembly.

As a result, significant yield losses occur with direct flip chip attachment to the routing substrate with less than 50 um line/space and 150 μm bond pad pitch; even with smaller bump design or careful warpage and dislocation compensation. It is clear that with this large disparity in geometry registration between chip and substrate, a low cost interposer with very tight dimensional stability has to be developed to close the gap.

Electroplated copper re-routing traces on a thick copper plate provide excellent dimensional stability due to its homogeneous characteristics. Electroplating of 15 μm copper at 50 μm line/space circuitry densities onto a 150 μm thick copper experiences almost no global as well as local deformation. Thus, excellent placement accuracy can be achieved when attaching bare dies to this rigid, homogeneous interposer using conventional non-conductive die attach adhesives. However, as there is no bump, no self-aligning effect, the chip will stays where it is placed. Advanced vision systems are required to ensure the accuracy of die placement.

Since the nickel-copper pattern is formed on the copper base and attached to the chip with adhesive, it is necessary to dislodge them from the conductive base in order to form the circuitry. By selectively choosing an etching solution which differentiates base material from trace overcoat (e.g. an ammonia system), fine line circuitry with nickel overcoat will remain un-attacked while the bulk copper is completely removed. The result is that re-routing traces that are mechanically coupled to the chip re-exposed and physically aligned to the designated bond pads. At this stage, although the re-routing circuitry is transformed to the chip surface, they not electrically connected yet as a thin-layer of adhesive still in between. For fan-out design, molding compound is used to provide critical mechanical support for the fan-out circuitry. The chip is fully protected by the molding compound from the top, and adhesive protect it from the back during the entire etching process.

Fig. 2 shows the 50 μm copper traces precisely aligned to the pads after copper base removal.

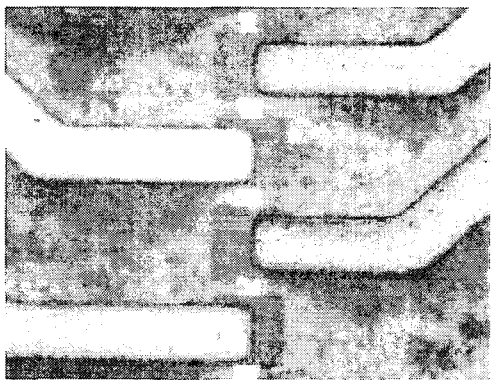

Fig.2. Fine Ni/Cu traces overlapped on the pads respectively

1st Level Interconnect. Only a few connection methods are widely used in the semiconductor packages. Wire bonding is by far the most popular 1st level interconnect technology followed by tape-automated bonding (TAB), solder, conductive adhesive, and thin film sputtering. Connection joints formed by these methods are typically associated with pressure or heat to form the connection.

Electrochemical Plating (ECP) is widely used in the copper IC fabrication due to its low cost and better electrical characteristics. Wafer lever gold or solder bumping for TAB and conventional flip chip applications is another example. In double-sided or multi-layer PCB, electrolytic copper is commonly used as the connecting material for through-hole plating. However, all these processes require seeding layer to provide the initial plating base. MOCVD, sputtering or e-less has all been proposed to place down the conductive seeding layer in either front-end or back-end processes. However, due to the nature of the plating bus, isolation processes such as chemical mechanical polishing (CMP) or selective patterning and etching is necessary to remove the seeding layer and isolate the patterns. CMP is far too expensive for back-end assembly. Semi-additive approach (e.g., plate-N-etch) is generally acceptable in the large panel PCB environment, but is still too expensive or impractical when single chip or few-chips

module is the processing unit especially when photo process is required. Furthermore, electroless seeding requires resins with special chemical properties and adequate surface conditions are necessary for a reliable adhesion. Currently, only a few plastics have demonstrated a good interfacial adhesion after proper surface pre-treatment. Electroless seeding is therefore greatly constrained by the dielectric material that can be applied.

One of our packages uses electrochemical process for first level interconnect without using any seeding player. The basic concept is; if connecting circuitry is pre-fabricated and can be placed in the close proximity to the bonding pad, just a little extending of the circuitry by electrolytic or electroless plating will eventually finish the "very last microns" between the circuitry and the designated bond pad. Once the isolated bond pad is contacted, electrochemical potential of the bond pad will be shifted to that of the trace where plating reaction is carried on. This "microscopic connection method" will lower the electrical potential of the connecting side thereby initiating the plating process on its surface automatically. The simultaneously plated material will serve to join the two ends thereby making the connection homogeneously (Fig. 3). Common plating materials such as copper or gold will provide a robust, permanent electrical connection between pad and the conductive trace.

As this is a low temperature electrochemical process, other materials such as nickel, tin, silver and palladium can be electrolytically deposited as well. Similarly, plating material can extend from the bond pad side directly by electroless nickel-plating process. With this approach, the aluminum bond pad has to be modified either by thin film or by zincation in order to activate the e-less nickel plating.

In practice, a wide variety of methods can be used to make the connection joints as long as the re-routing trace is pre-fabricated and placed in close proximity to the corresponding pad. Methods such as direct liquid solder dispensing, solder paste printing; conductive adhesive bonding and ball bonding can all be applied depending on the final applications. The shape and material composition of the joint depends on overall design and reliability considerations.

With this approach, the mode of the connection shifts from the initial mechanical coupling to metallurgical coupling to ensure sufficient metallurgical bond strength. Furthermore, the conductive trace is mechanically coupled to the chip without wire bonding, TAB, or solder reflowing.

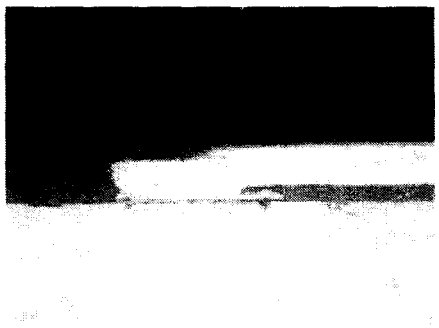

Fig. 3 Electroplated copper connects the trace and bond pad directly and forms a homogeneous joint.

Manufacturing throughput can be enhanced with the use of batch processing since all the bonds and traces can be connected simultaneously. Yield and performance characteristics compare well with most conventional packaging techniques. Moreover, the connection is well suited for use with copper chips and for lead-free environmental requirements.

2nd Level Interconnect. In a conventional leaded package, package-board strain is relieved through the compliant gull wing leads. In the area array packages, the strain must be relieved in the solder joint. The important mechanical variables for strain relief determined by ball distance from neutral point (DNP) which is determined by the chip size and bump pitch, the bump standoff height and the number of bumps.

Most of these considerations and models are based on the existing solder balls grid array packages. For most solder alloys, thermal fatigue failure frequently results in cracked solder joints. In high temperature regimes, a significant amount of creep and creep-induced fracture can also occur. Since the thermal fatigue of solder joints is strongly affected by a number of parameters such as package configuration, manufacturing, material composition and interfaces, modifying some of these parameters may significant affect package's board level reliability.

Polymer stud bumps are one of the recent examples proposed by Siemens, now Infineon. The polymer stud grid array (PSGA) substrate is a polymer injection molded body with polymer studs to make contact with a PCB using standard SMT soldering techniques [1]. Initial reliability results demonstrate good solder joint reliability and 3D non-linear finite element simulations have shown that the polymer stud behaves like an elastomer and the induced plastic strains are much lower than that in conventional PBGA packages.

Bumped chip carrier (BCC) packages developed by Fujitsu feature similar resin bumps at the bottom of the package [2]. These resin bumps are connected to the bond pad by wire bonding and covered with metal thin film to serve as interconnects from the package to the PCB. The reliability of the BCC solder joints was evaluated with thermal cycling conditions between –65 °C and 150 °C and no degradation in solder joint strength was observed during these tests. According to Fujitsu, this package has the performance and reliability equivalent to those of leaded packages. The first level interconnects were gold wire bonds.

In our package design, the package terminal is part of the routing circuitry. In other words, the electroplated conductive trace includes a bumped terminal that was originally a recess in the copper plate. This method requires forming a series of recesses in the copper base first, followed by electroplating the conductive traces onto the base such that each conductive trace includes the bumped terminal in the recess as well as the routing line outside the recess to the die pad. Thus, each conductive trace becomes a single continuous low-profile metal segment. After die attach or encapsulation, resin fills each cavity will convert into resin-filled bumps when copper carrier is removed.

An advantage of this approach is that the process has very low manufacturing costs and need not include complicated precious metal plating and wire bonding steps. The elastic properties of the resin permits each bumped terminal to provide a compressible compliant contact terminal thereby ensuring excellent board level reliability.

FABRICATION

Fig. 4 illustrates the various process steps in the fabrication of a bumpless flip chip package in a generalized process flow. We have demonstrated the compatibility of our process for DDR SDRAM memory packages with die pads located in the center.

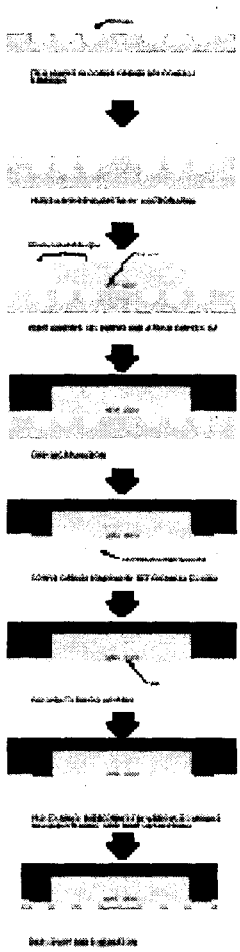

Fig. 4. Generalized Process Flow

The packaging process is as follows: Die pads, terminal locations and fine line trace pattern are defined with system and chip designers. A series of recesses or dimples corresponding to the terminal locations are formed by half-etching in a copper panel along with tooling holes to handle the panel. Power/ground lines and signal traces are formed by dry-film patterning and electroplating process. Die attach adhesive is precisely dispensed to ensure complete filling of recesses in the copper carrier. Bare chips are flipped and bonded onto the copper frame using an image scan to align the traces and the die pads. The composite structure of chips and frame is cured under heat and encapsulated with

mold compound using automated transfer molding. Parts of the copper frame under each chip is left exposed and removed by a wet chemical etching process. The die attach adhesive and trace material act as an etch stop and a series of raised bumps is revealed. Via holes, typically 50 um wide and 10 um in depths, are drilled by laser over the chip pad positions. Any polymer debris and residual film are removed by plasma etch. Via hole taper can be adjusted by varying the laser scan condition and can be formed with high reliability and continuity in the via hole. The via filling step is performed by electroplating or electroless plating to form the connection joints between each trace and chip pad. Plating is precisely controlled by design such that the traces do not grow laterally and violate line/space design rules but make excellent contact with each chip pad. The package is sealed with a final layer of epoxy leaving the tops of each bumped terminal exposed for board level contact and singulated.

Fig. 5 shows four different close-up views of key elements of the bumpless flip chip package.

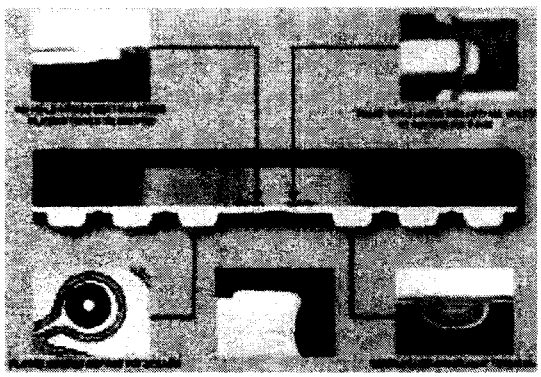

Fig. 5 Close-up views of the package

CONSIDERATIONS FOR COST/ PERFORMANCE DRIVEN DEVICES

Package Performance. The reduced inductance and capacitance of these bumpless flip chip packages improve noise characteristics to enable higher system-level performance. Improved thermal impedance and BLR requirements have been demonstrated. Costs savings in both PCB real estate and actual component cost have been estimated to contribute significantly to system level savings. Package designs follow JEDEC standards and fit completely to the existing board assembling infrastructures. However, our design flexibility still allows some non-standard packages to be built (e.g., 3D structure) when requested by the customers.

Improved Manufacturing. This packaging approach also presents a paradigm shift in the packaging technology and design cycles where various packages can be manufactured virtually on the same manufacturing platform. In other words, both leaded packages (e.g., TSOP, TQFP, etc.) and area array packages (e.g., CSP, BGA, etc.) are under the same manufacturing process flow with only minor differences. Chip-level or system-level improvements such as die shrinkage are transparent from the packaging process viewpoint.

Most importantly, these manufacturing techniques are in line with or an extension of current lead-frame, PCB and semiconductor back-end manufacturing processes. Thus, new investment or transition toward new manufacturing infrastructures is largely avoided.

Future process and material innovations in package assembly and testing such as improved automated optical inspection, high temperature tape, low D_k die attach material, tape-less singulation, strip test are expected to further enhance performance and throughput and allow for cheaper, faster, better, and smaller packaging trends to continue well into the future.

Design Flow. In general, system-level performance is measured in terms of timing, signal integrity, power supply noise, and radiated emissions budgets. These characteristics are directly related to the electrical characteristics of the interconnect such as its characteristic impedance, crosstalk and switching characteristics, resistance, loop inductance and capacitance. These, in turn, are affected by the physical design of the interconnect and material selections.

In our approach, characteristic impedance is largely determined by the adhesive's dielectric constant between layers, and the width and height of the traces. Trace resistance is determined by the resistivity of the plated metal, plating height and width, and the length of the traces. Joint resistance is determined by the choice of connection type and material. Crosstalk is determined by trace spacing, the number of layers and the dielectric constant of the material between layers. Switching, loop inductance and capacitance are determined by

the location and orientation of power and ground planes, vias and the location and orientation of discrete capacitors.

Design flow and choices made are very important in determining the electrical and mechanical characteristics of the package and ultimately, the performance of the overall module or system. With our approach, design cycles for cost/performance driven packages, for the first time, may be synchronized with die-level and system-level design cycles to minimize sub-optimization and tradeoffs.

SUMMARY

In all packaging technology development, it is paramount that cost targets be met without compromising performance. As chip and system-level performance improved at exponential rates, the role of packaging that enables such high performance at low cost is increasing importance.

The innovative packaging approach presented here represents a bold step forward to demonstrate that existing, robust, flexible yet low-cost manufacturing infrastructure for advanced packages is available. This approach not only addresses the current issues, but also challenges the future needs to ensure performance requirements are met from various aspects.

Combined with a design for manufacturing approach in which performance and cost trade offs are made concurrently with die-level and/or system-level, we believe that we have delivered a cost-effective yet highly reliable solution for cost/performance driven devices for the long term.

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