



# **Chip on Glass Technologies for High-Performance LCD Applications**

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Thin Film Materials and Electronic Packaging Lab.



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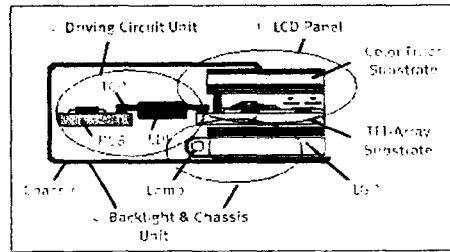
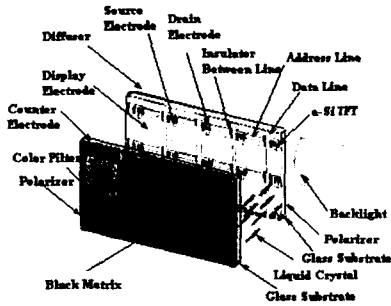
- ✓ **Introduction**
  - Requirements and Trend in LCD driver IC packaging technology
  - Chip on Glass (COG) Technology
  - Approach
- ✓ **Process development**
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- ✓ **Summary**

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## TFT-LCD Display

### ✓ Structure of TFT-LCD Display



(Sourced by Samsung Electronics)

### ✓ Key requirements of driver IC packaging

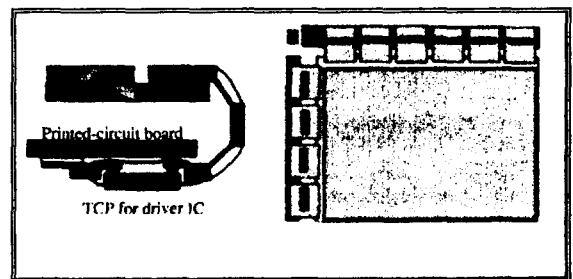
- Higher density connection to the panel
- Lower packaging cost
- Lower product profile
- Acceptable joint resistance
- Lower temperature process
- Reworkability

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## Trend in TFT-LCD Driver IC Packaging Technology

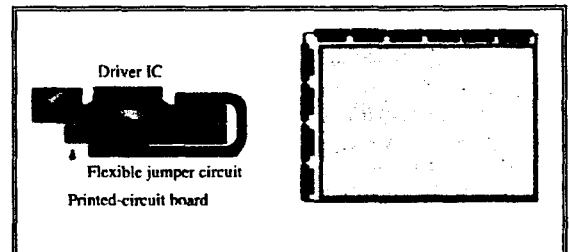
### ✓ TAB (Tape Automated Bonding)

- Widely used
- Applied to large display
- Minimum pitch  $\approx 55 \mu\text{m}$



### ✓ COG (Chip on Glass)

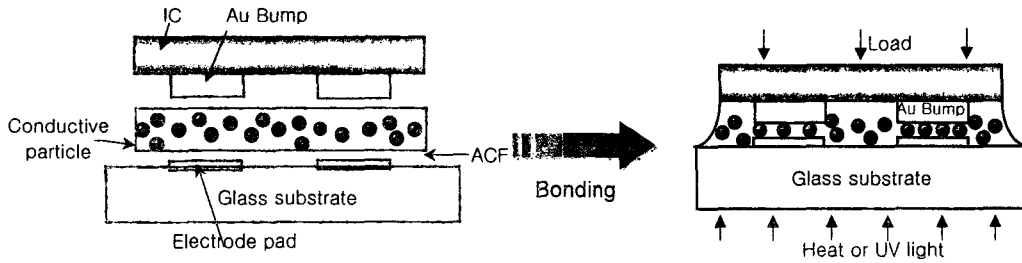
- Slim and simple construction
- High reliability
- Applied to small display



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## Chip on Glass (COG) Technology

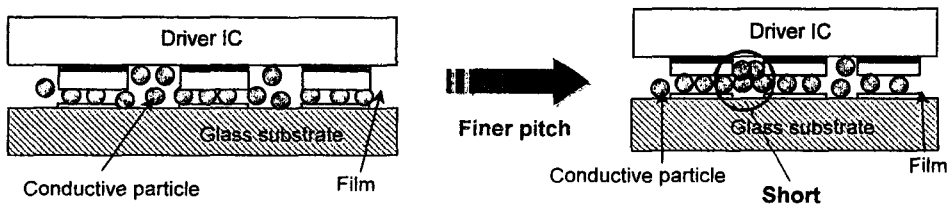
- ✓ Au bump formation on driver IC
- ✓ Bonding using Anisotropic Conductive Film (ACF)
- ✓ Conventional flip chip bonding using ACF



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## Problems of COG Technique Using ACF Due to Ultrafine Pitch Application

- ✓ Increased possibility of electrical short



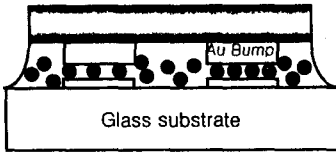
- ✓ Increasing contact resistance due to reduced conducting particles in a bump

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## COG Process Using Solder Bumps

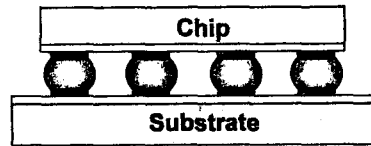
- **Conventional method**

- Using anisotropic conductive film (ACF)

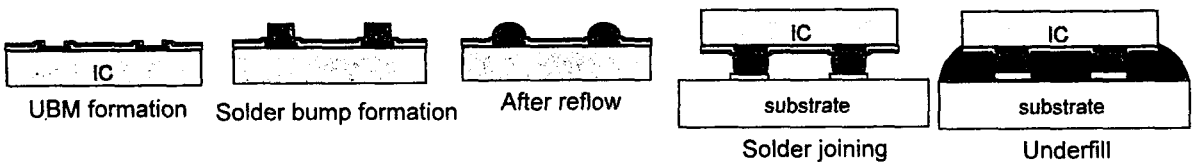


- **New method**

- Using flip chip solder joining



- ✓ **Flip chip solder joining process**



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## Flip Chip Solder Joining for LCD Driver IC Packaging

- ✓ **Advantages**

- Finer pitch capability
- Self-alignment due to the surface tension of liquid solder
- Good electrical performance
- Easy reworkability

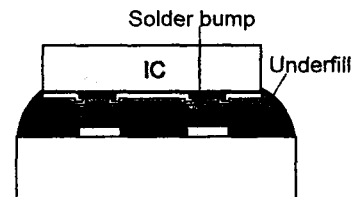
- ✓ **Problems**

- High temperature process ( $T > 200^\circ\text{C}$ )  
ex) 37Pb-63Sn  $T_{mp} = 183^\circ\text{C}$   
95Pb-5Sn  $T_{mp} = 304 - 312^\circ\text{C}$
- Liquid crystal or color filter can be degraded.

- ✓ **Approach**

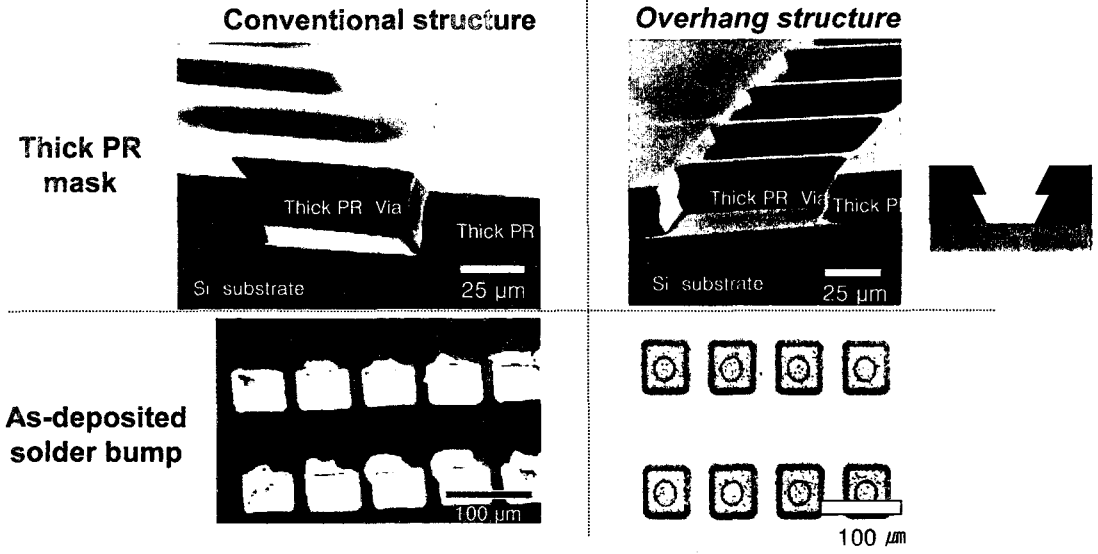
- Using low mp solder
- 58%Bi-42%Sn( $138^\circ\text{C}$ ), 97%In-3%Ag( $141^\circ\text{C}$ )

➔ Flip chip solder joining should be processed below  $160^\circ\text{C}$ .



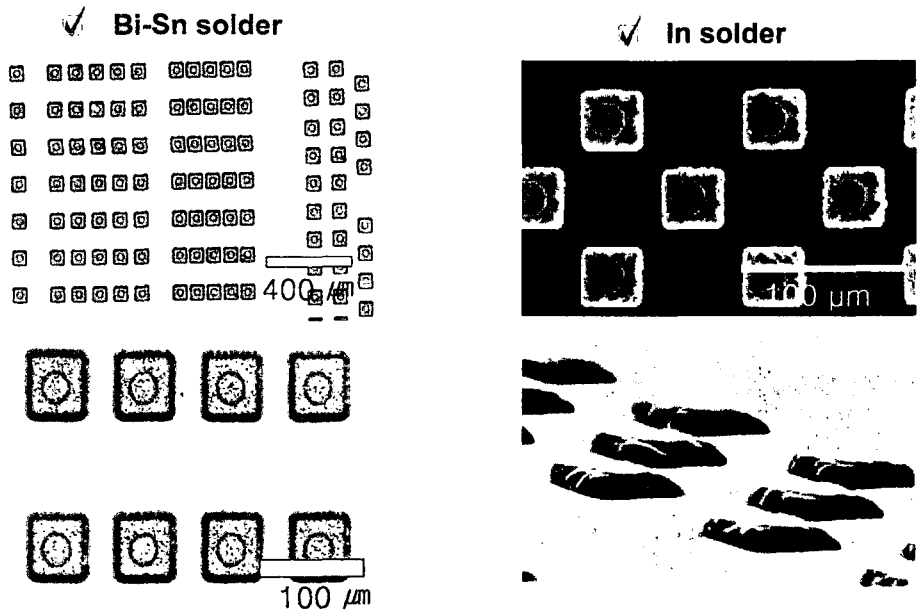
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# Ultrasmall Solder Bump Formation Using Lift-off Process



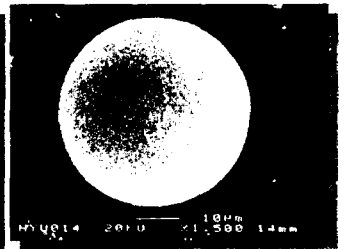
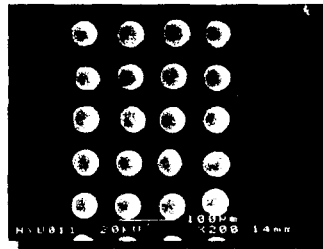
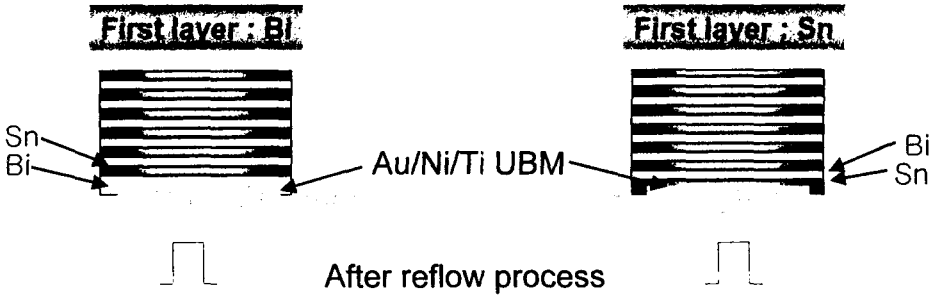
*Overhang structure is more effective for perfect lift-off conventional one. Perfect lift-off is important for ultrasmall solder bump formation.*

# As-deposited Solder Bumps after Lift-off Process



# Wetting Characteristics of Bi-Sn Solder on Au/Ni/Ti UBM

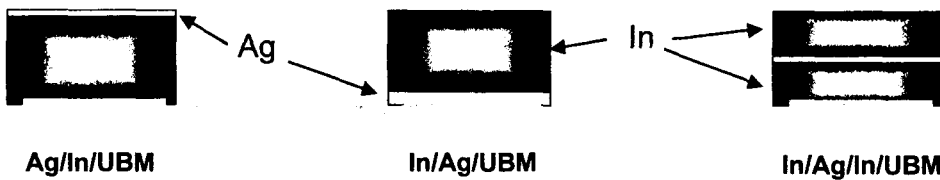
- Cross-sectional schematic view of as-deposited solder



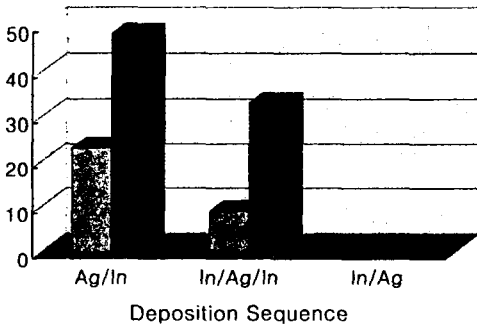
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# Ultrasmall Bump Formation of In-Ag Solder

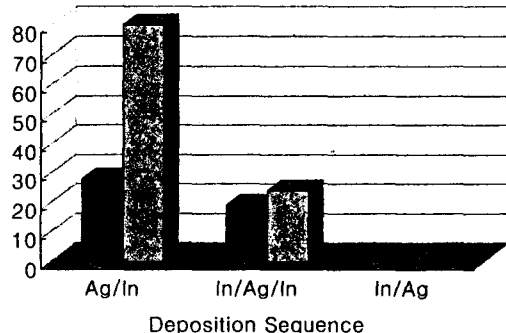
- Cross-sectional schematic view of as-deposited solder



Ball Formation Ratio with Solder Size



Ball Formation Ratio with Solder Density



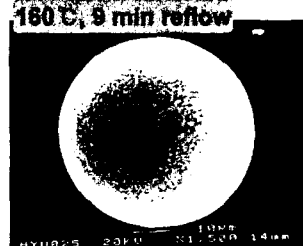
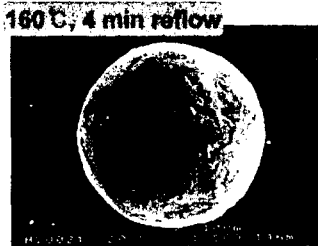
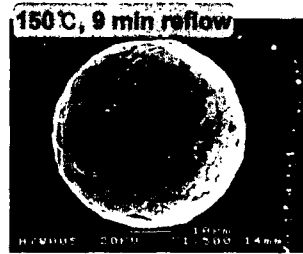
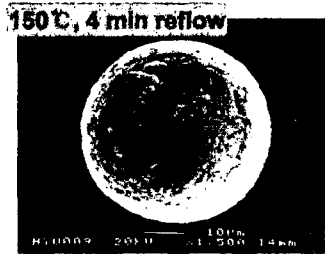
■ 50 μm solder ball ■ 30 μm solder ball

■ Pitch size < 100 μm ■ Pitch size < 300 μm

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## Surface Morphology of Bi-Sn Solder Bumps

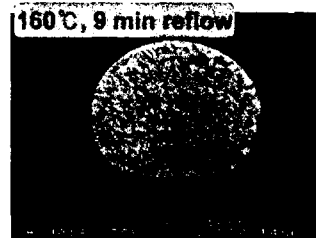
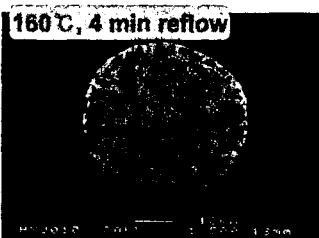
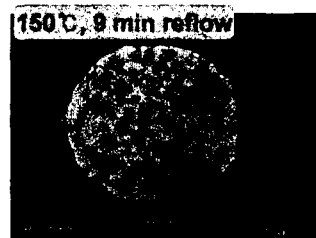
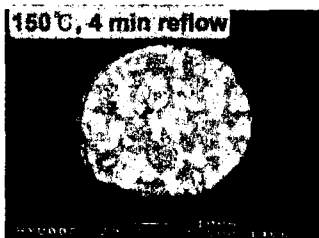
- Au/Cu(1  $\mu\text{m}$ )/Cr UBM
- Intermediate cooling rate (10  $^{\circ}\text{C}/\text{min}$ )



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## Cross-sectional Images of Bi-Sn Solder Bumps

- Au/Cu(1  $\mu\text{m}$ )/Cr UBM
- Intermediate cooling rate (10  $^{\circ}\text{C}/\text{min}$ )

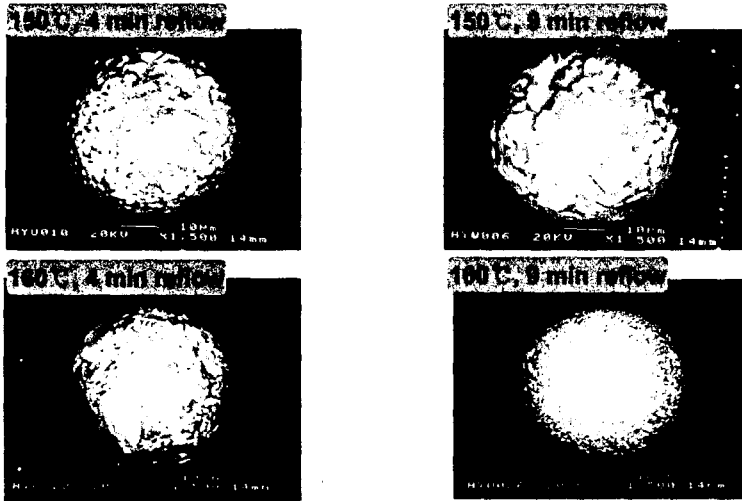


*Finer microstructure makes smoother surface and more spherical shape*

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## Backscattered Electron Images of Bi-Sn Solder Bumps

- Au/Cu(1  $\mu\text{m}$ )/Cr UBM
- Intermediate cooling rate (10  $^{\circ}\text{C}/\text{min}$ )



The surface morphology is controlled by the microstructure of Bi-Sn solder

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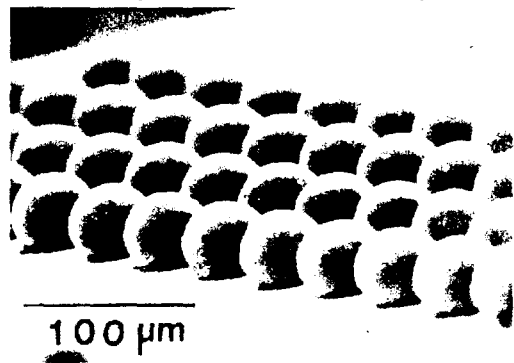
## Solder Bumps after Reflow Process

- Peak temperature : 160  $^{\circ}\text{C}$

50  $\mu\text{m}$  pitch Bi-Sn solder bumps



80  $\mu\text{m}$  pitch Bi-Sn solder bumps



Ultra-small and spherical solder bumps can be uniformly fabricated. Uniform and smooth solder bumps are suitable for flip chip bonding.

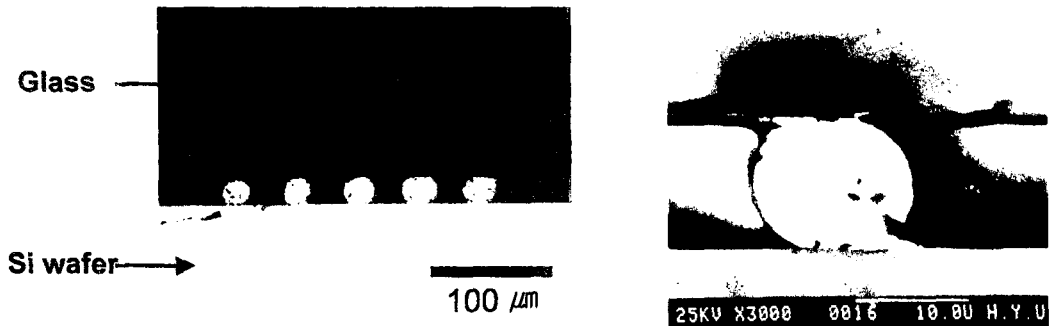
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## Cross-Sectional SEM Images of Solder Joints

- ✓ In-Ag solder on Au/Cu/Cr (50  $\mu\text{m}$  pitch)  
Reflow temperature : 160  $^{\circ}\text{C}$

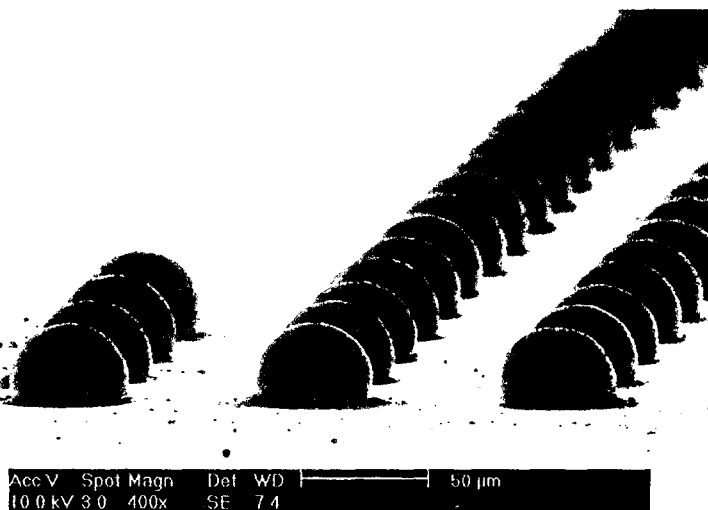


*The ultrasmall solder joints having 50  $\mu\text{m}$  pitches were assembled successfully.*

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## SEM Image of Electroplated Bi-Sn Solder Bumps after Reflow



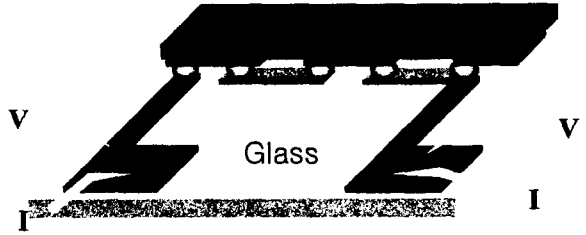
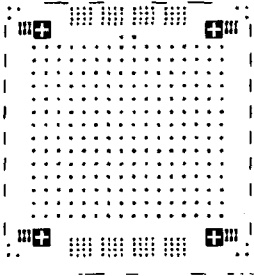
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# Electrical Test Using Daisy Chain Method

## • Test vehicle

- Pitch size : 80  $\mu\text{m}$ , 200  $\mu\text{m}$
- Maximum pad number of a daisy chain : 112
- Solder material : Evaporated eutectic Bi-Sn



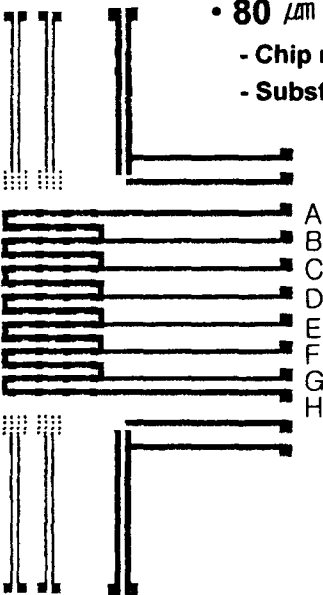
Schematic view of electrical test vehicle



# One Example of Contact Resistance Measurement Data

## • 80 $\mu\text{m}$ pitch Bi-Sn solder joint

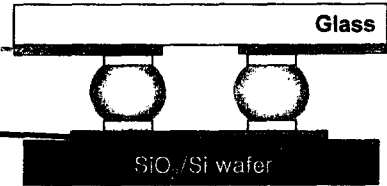
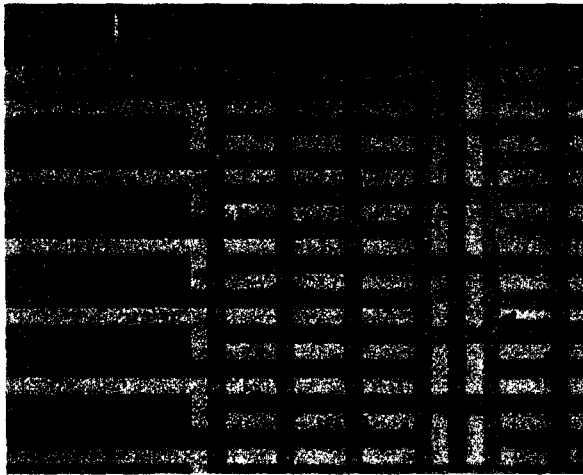
- Chip metallization : Au/Cu/Ti
- Substrate metallization : Au/Cu/Ti



Probing pad	# of solder joints	Total resistance ( $\Omega$ )	Resistance per section ( $\Omega$ )	Contact resistance per solder joint ( $\Omega$ )
A-B	16	0.620		
A-C	32	0.908	0.288	0.0180
A-D	48	1.152	0.244	0.0153
A-E	64	1.474	0.322	0.0201
A-F	80	1.824	0.350	0.0219
A-G	96	2.148	0.324	0.0203
A-H	112	2.484	0.336	0.0210
Average contact resistance per solder joint				0.0194

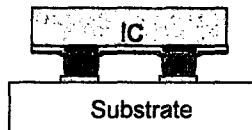


# Optical Micrograph of Electrical Test Specimen



# Contact Resistance of Ultrasmall Bi-Sn Solder Joints

- Before underfill process
- Average value in several specimens



Solder Joint	Chip Metallization	Substrate Metallization	Contact resistance (Measurement)		Contact resistance (Calculation)
			Average ( $\Omega$ )	Standard deviation	Average ( $\Omega$ )
80 $\mu\text{m}$ Pitch Bi-Sn Solder	Au/Cu/Ti	Au/Cu/Ti	0.019	0.003	0.008
		Au/Ni/Cu/Ti	0.035	0.006	0.012
50 $\mu\text{m}$ Pitch Bi-Sn Solder	Au/Cu/Ti	Au/Cu/Ti	0.060	0.019	0.042

*The contact resistance of Bi-Sn solder joints is much lower than that of conventional ACF bonding for COG technique.*

# Contact Resistance of Solder Joints after Underfill

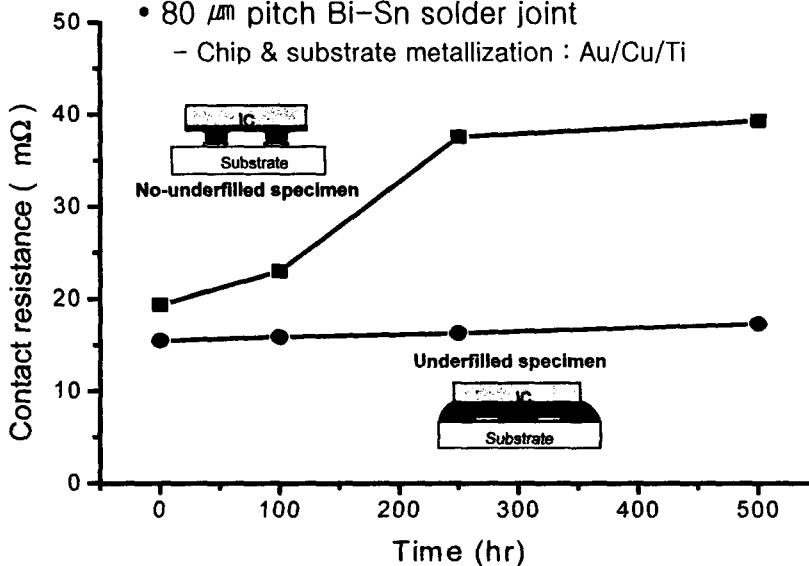
- **Underfill process**
  - Material : Epoxy (AMICON E 1355)
  - Curing condition : 160°C, 5 min holding



Solder Joint	Chip Metallization	Substrate Metallization	Underfill	Average contact resistance ( $\Omega$ )	Standard deviation
80 $\mu\text{m}$ Pitch Bi-Sn Solder	Au/Cu/Ti	Au/Cu/Ti	Before Underfill	0.019	0.004
			After Underfill	0.023	0.007

# Contact Resistance after 85 °C/85% RH Storage

- 80  $\mu\text{m}$  pitch Bi-Sn solder joint
- Chip & substrate metallization : Au/Cu/Ti



**The contact resistances of Bi-Sn solder joints did not change even after hot humidity test.**



## Summary

- Using eutectic In-Ag and Bi-Sn solder materials, we developed the COG technique having a minimum pitch of 50  $\mu\text{m}$ . The maximum temperature in this process is 160 °C.
- We fabricated spherical and uniform solder bumps by controlling the microstructure of Bi-Sn solder bumps.
- The contact resistances of Bi-Sn solder joints were 19 m $\Omega$  at 80  $\mu\text{m}$  pitch and 60 m $\Omega$  at 50  $\mu\text{m}$  pitch, respectively. These values are much lower than the contact resistance of the conventional ACF bonding.
- The contact resistances of the solder joint are almost the same before and after the underfill process. The contact resistance of the underfilled Bi-Sn solder joint did not change even after reliability test.