ISMP 2002

Current Trend of Packaging Technology Development in Japan

IMAPS Japan
Nagano Institute of technology
Dr.Sei-ichi Denda

Sept.10, 2002 in Seoul

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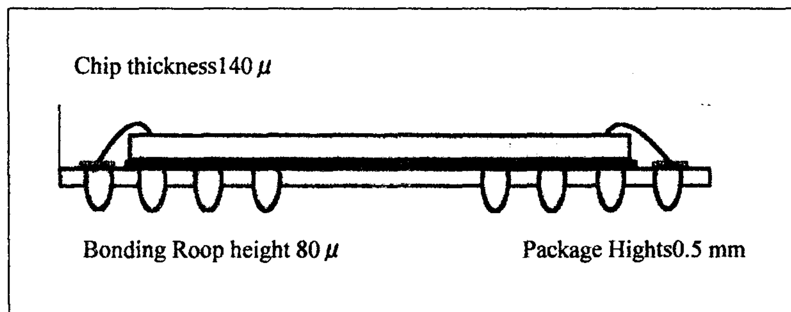
Thin 0.5H FLGA Series (Fujitsu)



14 x14mm x 0.5mm, chip 8.5mm,
368pin TBGA

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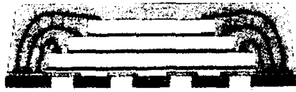
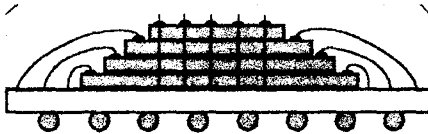
Chip Stack Packages



3 stack CSP, Chip140μ, 1.4mmH

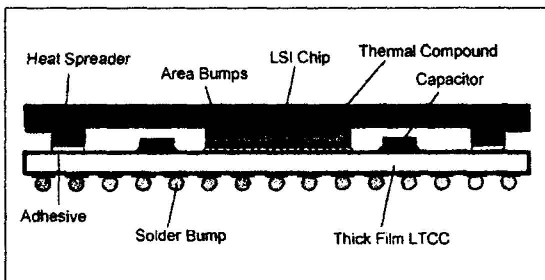


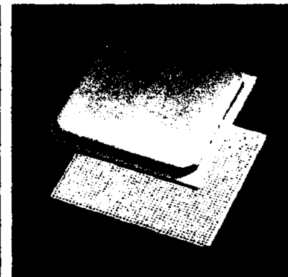
4 stack CSP by Sharp, Chip 100μ

1.4mmH

Sharp

Fujitsu



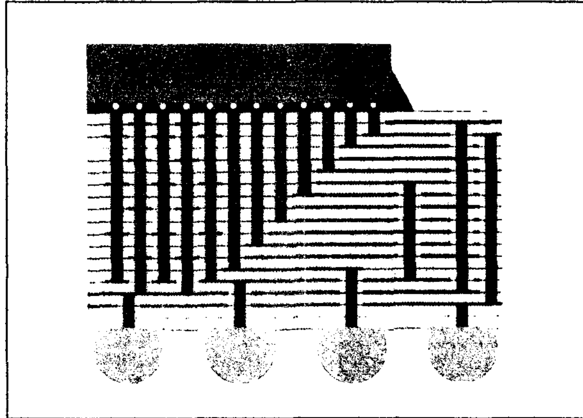


FC CBGA for 450MHz CPU (Fujitsu)

Chip: 0.18μ Rule, Cu Wiring 6 Layer, 15mm sq. , 223μ Pitch
4032 Sn-Ag Bumps, 550μ Thick

Package: LTCC 18 Layers, 37mm sq., Solder 1206 Bumps,
1mm Pitch, 606 Signals, AlC Heat Spreader, θ =10°C/ W

18Layer Ceramic Interposer (Fujitsu)



L/S=70 μ ,Via Hole:75 μ , pitch:223 μ , CTE:11.5

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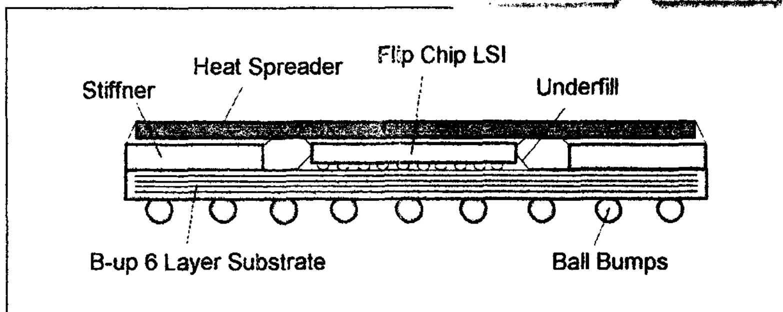
Flip Chip BGA (NEC)



45x45x2.4Hmm, 1898 Bumps, Pitch 1mm,
FC17.5x17.5mm, 6880 Pins, 0.13 μ CMOS, Al 8 Layer

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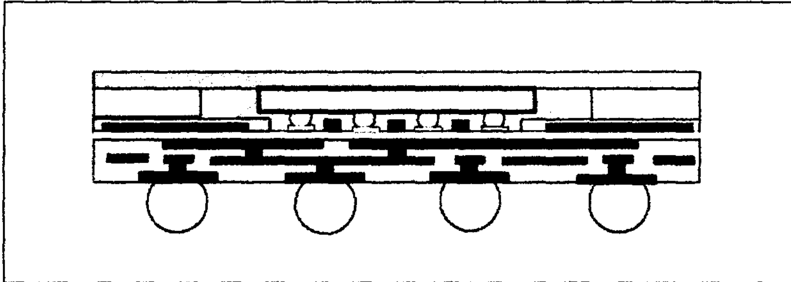
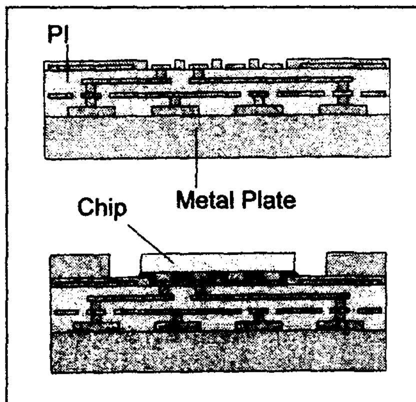
Tape Stacked BGA Package (NEC)

- High Density, High Speed • No Through Hall
- Stripline Wiring • 12 (Bup) Layers ⇒ 4 Layers

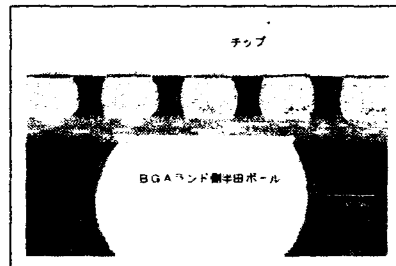


- L/S=20/20 μ • Via/Land=40/60 μ • FC Pad 2500 • Pad Pitch 240 μ
- BGA Bump 1296, • Bump Pitch 1mm • Size 37.5mm□

Tape Stacked BGA Package (NEC)



Tape Stacking Process

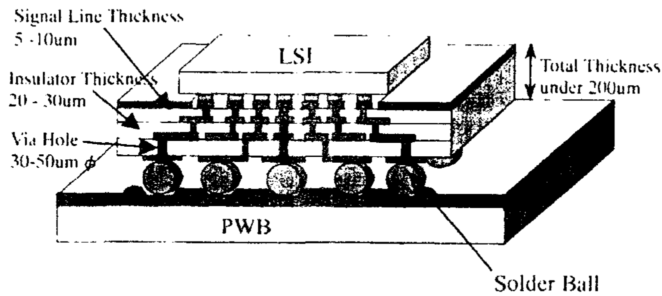


Cross Section

Pad Pitch 240 μ

Multi Layer Tape BGA Package (Toppan)

High Frequency Interposer



・Polyimide 4 layer ・Real to real process ・I/O=2000・Cu via

・150 μ Pad pitch・L/S=20/20 μ ・Microstrip wiring structure

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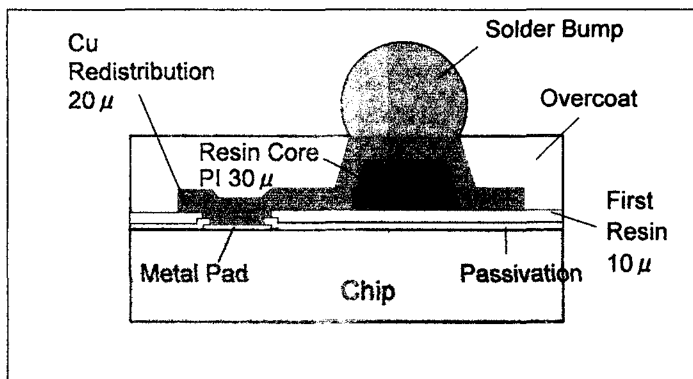
WLP with Resin Core Post Bump

(Fujikura)



0.5mm Pitch, Chip Size 5-6mm, I/O 20-30

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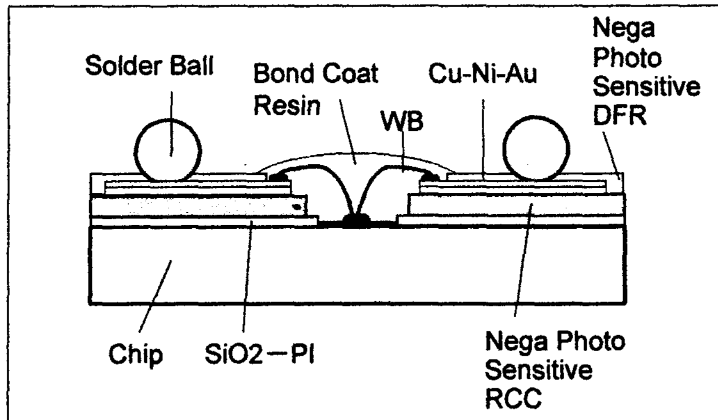
Wafer Level Package for Substrate House（NEC)

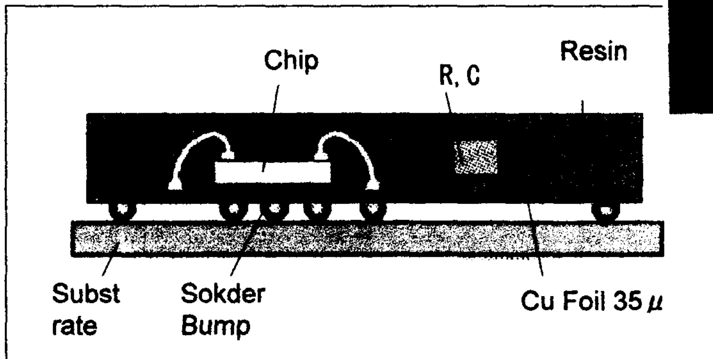
Eliminate redistribution process and one
chemical etching to complete WLP



Subtractive WLP-NEC

Interposerless Package (Sanyo)

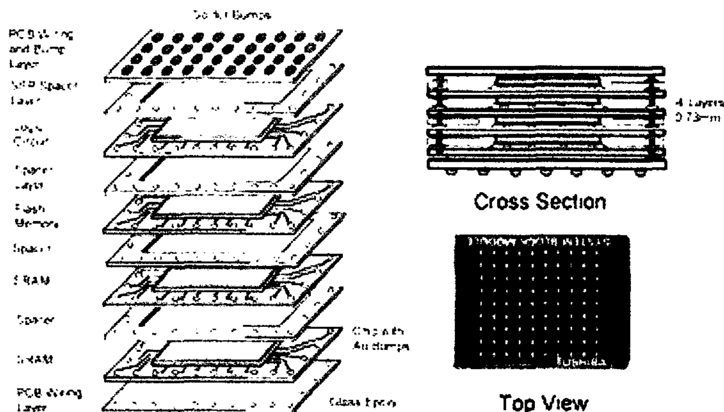
ISB（Integrated System in Board)



Low cost, heat dissipation, hybrid
IC like process

How to make?

System Block Module



Ibiden-Toshiba System Block Module utilizing SSLP

Glass Epoxy Substrate 40μ, Chip 50μ with Au Bumps L/S=25μ Cu Film 9μ,
Laser Via 60μ, Press Stacking at 180C, Total 0.73mm (w/o Solder Bump)

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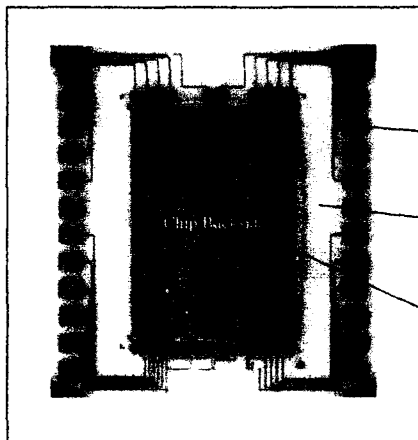

Test Pad

Interposer

Underfill

SBM PTP substrate (X ray image)

(NAND Flash Memory)

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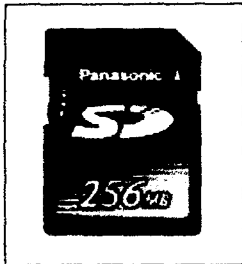
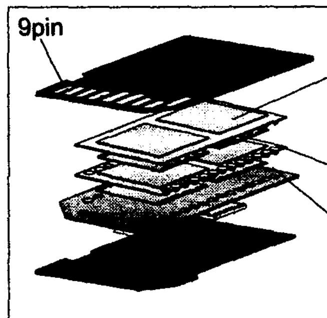
SD Memory Card (Matsushita)

Secure Digital—Matsushita, Toshiba, Sundisk, 300 others



Stamp Size
Flash Memory
256byte



80 μ Chipx8
ACF Sheet
SBB FC
Cu
FR4
0.1mm

Card 32x24mm, 2.1mm thick, Chip 12x17mm

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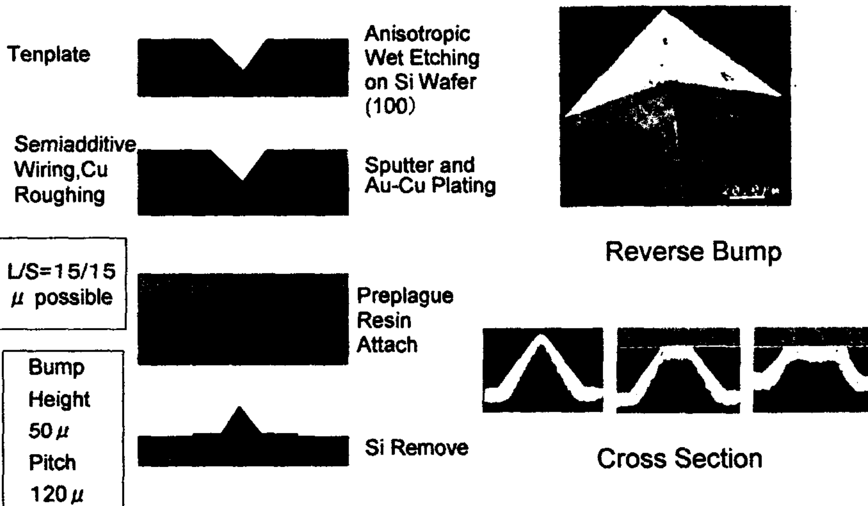
Reverse Bumping (Toshiba Chem)



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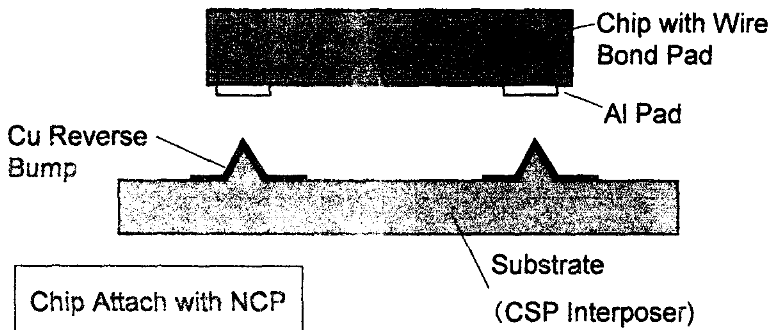
Reverse Bump Connection

(Toshiba-Toshiba Chemical)

Resin Core Reverse Bump for CSP Package



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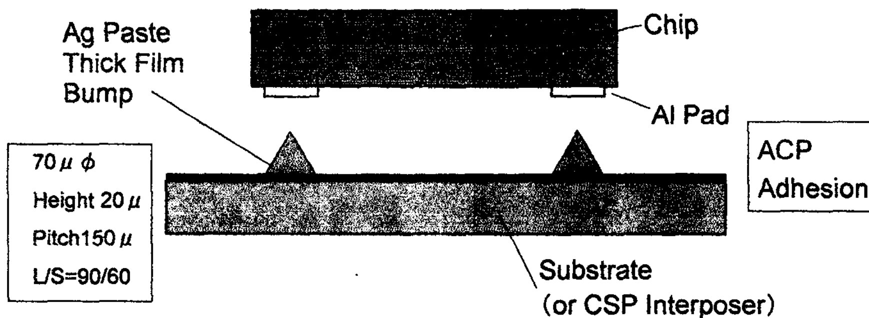
Thick Film Reverse Bump

Bumps for flip chip attach formed on the substrate
with square bit－BOSS

DTCT-Weisti—B2IT Extension



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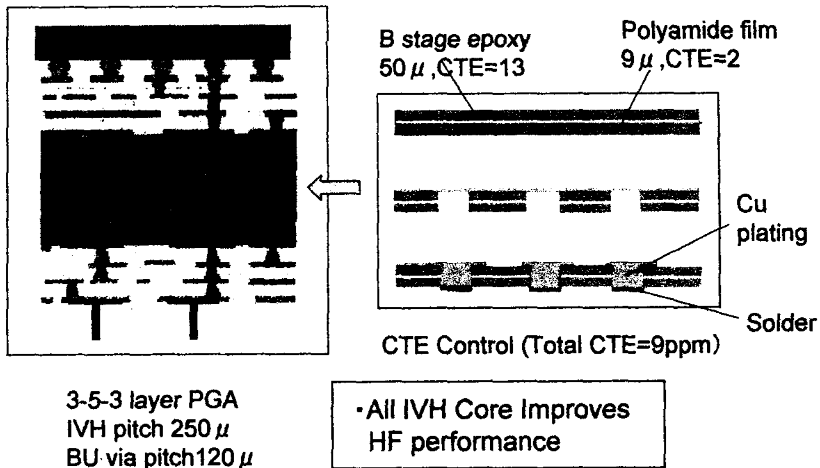
CTE Controlled IVH Core Built up Substrate for CPU Packages (Shinko)



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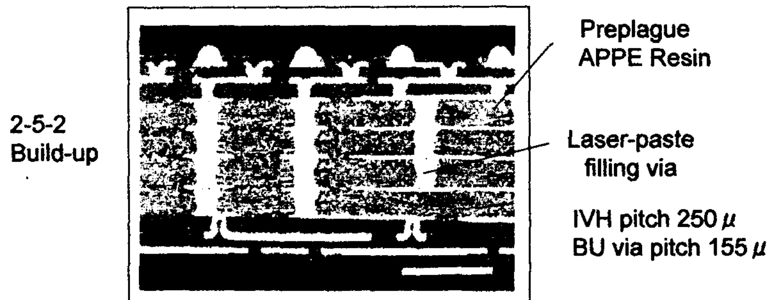
Stacked IVH Core Built up Substrate - Super HDBU Packages (Kyocera)



- IVH Core Improves HF performance
- Circuits made with tape transfer
- L/S=30/30 μ

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Resin Core Solder Bump (Sekisui)

- Bridged Polymer Core Bump
- Inner Stress 25%
- Board Reliability : x2 Cycles
- Standoff Hold

Polymer
Modulas : 4,700Mpa
(Solder: 31,700Mpa)
CTE: 50 (Solder: 24, FR4: 14)

Polymer—(750μ)-Cu (5μ)-Eutectic Solder (20μ)

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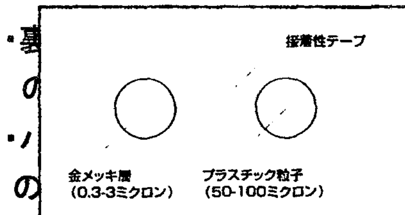
Flip Chip Tape (Sekisui)



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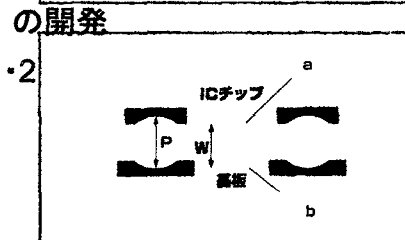

- Au Plated Plastic Ball in Film
- Tape Adhesion Keeps Electrical Connection
- No Underfill
- Al Pad Chip Applicanble

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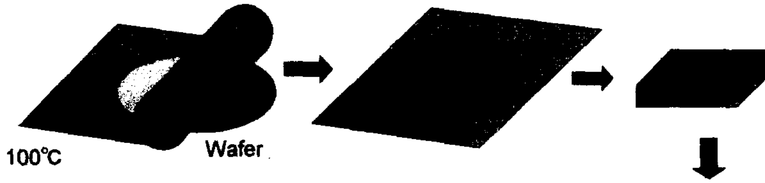
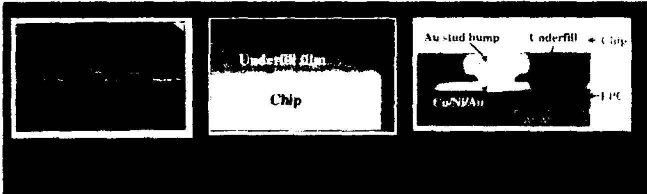
Wafer Level Underfill (Nitto)

Underfill Sheet Attach → Back grinding Wafer Dicing → Flipchip with Underfill





Flipchip Bonding 250℃, 60sec with Pressure

Sheet:Polycarbodiimide 20μ, Shelf Life 3Months in RT

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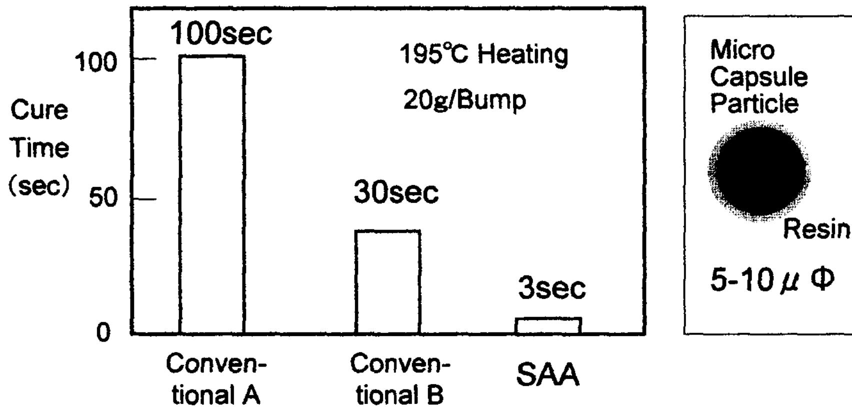
Short Curing ACP (Fujitsu-Threebond)

SAA (Snap Attachment Adhesive)

Self Heat Generation Cure Accerarator



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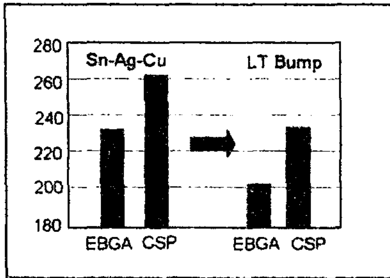
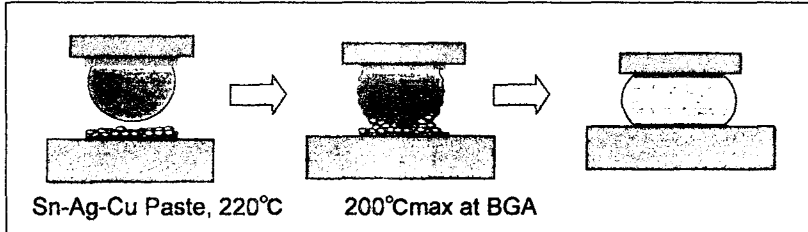
Component Temperature



Low Temp Pb free Solder Bump for Large BGA

Sn-57Bi (Eutectic)
138℃, EBGA 45 mm□, Fujitsu



Sn-Ag-Cu Paste, 220℃ 200℃max at BGA

Reliability better than Pb-Sn Eutectic

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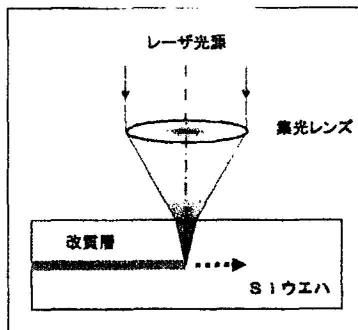
Thin Wafer Dicing

Stealth Laser Dicing (Hamamatsu)



- Silicon Structure Change in Wafer ⇒Breaking
- Dry Process
- High Speed (30cm/s)
- Cut Width less than1 μ
- No Chipping

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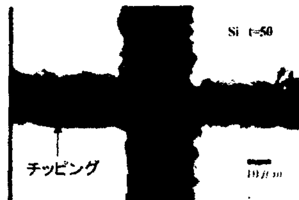
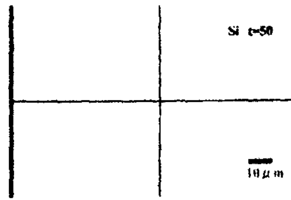
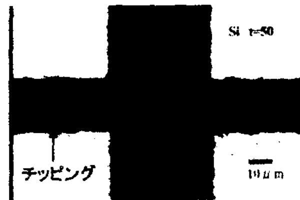
Stealth Laser Dicing (Hamamatsu)



Saw Dicing



Stealth Dicing



Dicing before Grinding

Brake and Expansion

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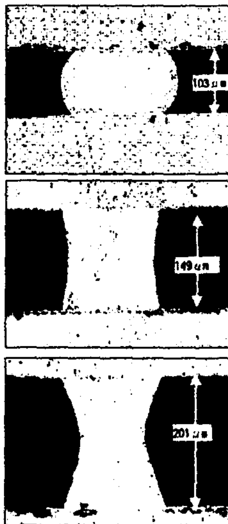
Standoff Control Flip Chip Bonding (NEC)



- Solder Bump Collapse with Weight and Heat
- Chip Touches to Substrate⇒ Start Heating⇒ Solder Melt⇒ Chip Pull up ⇒Spacing djust⇒ Cool down

- Chip Size1mm□~25mm□
- Substrate Size <100mm□
- Accuracy 2μ
- Weight 5~20Kg
- Temp. max600℃
- O2 Conc.100ppm以下

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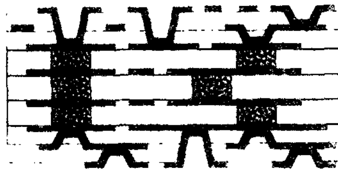
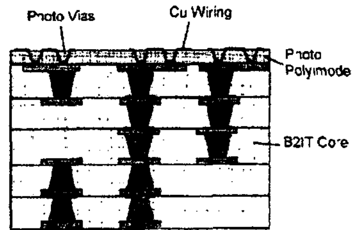
2nd Generation All Layer IVH Built up Substrate

Design Flexibility, High Density, Thin, Light

Film 12 μ





ALIVIL, ALIVH-CALIVH FB	B2IT Fine
Core L/S=45/45 μ	Core L/S=30/30 μ
BU L/S=25/25 μ	BU L/S=20/20 μ
Matsushita, Victor, CMK	Toshiba, DTCT

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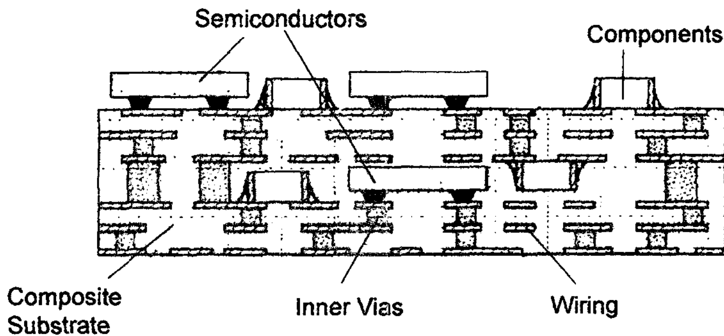
Super Integrated Module —SIM (Matsushita)

Includes Semiconductor Chips -Extension of ALIVH



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