Taiwan Packaging Status

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Abstract

The status of IC industry in Taiwan will be mentioned briefly in the first place. Focus will be mainly on the technology and business of packaging industry in Taiwan. The developments and accomplishments of packaging technology by either research institute or packaging industry will also be introduced.

Introduction

Taiwan, having been as one of the five major participants in worldwide IC manufacturing activities, has played an important role in IC packaging industry.

The global positioning of Taiwan IC industry is illustrated as Table 1. The total revenue of all IC products was over 9 billion USD in 2000. The global ranking was no.4 led by USA, Japan and Korea. Same ranking was observed for the IC fabrication industry, with total revenue of about 15 billion USD in 2000. IC design industry, with a revenue of 3,6 billion in 2000, was ranked no.2, second to USA. However, the global ranking of IC foundry industry was no. 1 in 2000, with a total revenue of about 9.5 billion USD. Packaging industry, with a total revenue of over 3 billion USD, was also ranked first in 2000 [1]. Comparing to the revenue of IC industry in 1999, which was 13.1 billion USD, the total revenue of IC industry enjoyed a rather high growth up to 22.3 billion USD in 2001.

Infrastructure of Taiwan IC Industry

The infrastructure of Taiwan IC industry can be depicted as Fig. 1. There are more than 200 companies in IC industry. Which includes 140 IC design houses, 16 IC Fabs and foundries, 48 packaging houses and 37 testing companies. All these companies form a strong and complete infrastructure for IC industry. They have contributed not only the high growth of IC industry, but also the high-tech business and the high growth of economy. Unfortunately, as the "severe winter" of global IC industry came and is going to have a 17% or above recession, Taiwan, unavoidably, also seriously suffered from this worldwide marketing depression and the depreciation of NTD to USD exchange rate. Consequently, the first time with a negative growth rate of revenue simultaneously happened in Taiwan in

Table 1 Global Positioning of Taiwan IC Industry (2000)

	Item	Revenues (MUSD)	Global Mkt Share	Global Ranking	Leading Countries
Product	All IC	9,159	5.10%	4	USA, Japan, Korea
	DRAM	4,941	15.30%	4	Korea, Japan, USA
	SRAM	398	6.10%	4	Japan, Korea, USA
	Mask ROM	630	57.50%	1	Taiwan
Industry	Design	3,669	20.70%	2	USA
	Fabrication	14,886	7.80%	4	USA, Japan, Korea
	(Foundry)	9,446	76.80%	1	Taiwan
	Packaging	3,115	34.10%	1	Taiwan
	Testing	1,045	34.60%	-	-
	Production Capacity	-	13.50%	3	Japan, USA

2001 since 25 years ago. The total revenue of Taiwan IC industry decreases with a negative growth rate of 19.7% to 17.9B USD (exchange rate NTD : USD = 34.5 : 1) in year 2001. For the revenue of IC packaging, it increased from 2.04B USD in 1999 to 2.67B USD in 2000 with a 30.9% growth rate. However, due to the global depression as mentioned, it is expected to reduce to 2.16B USD in 2001, which is a 19.1% decrease.

In this bad situation, the bigger one is still bigger. Therefore, as the same results of year 1998 and 1999 [2, 3], 75% of the revenue in year 2000 was created by the top 5 companies, ranked as ASE, SPIL, OSE, ASECL and Greatek. On the other hand, about 66% of the total revenue was contributed from QFP (Quad Flat Pack), BGA (Ball Grid Array) and CSP (Chip Scale Package) production although it only shared 26% of total package units.

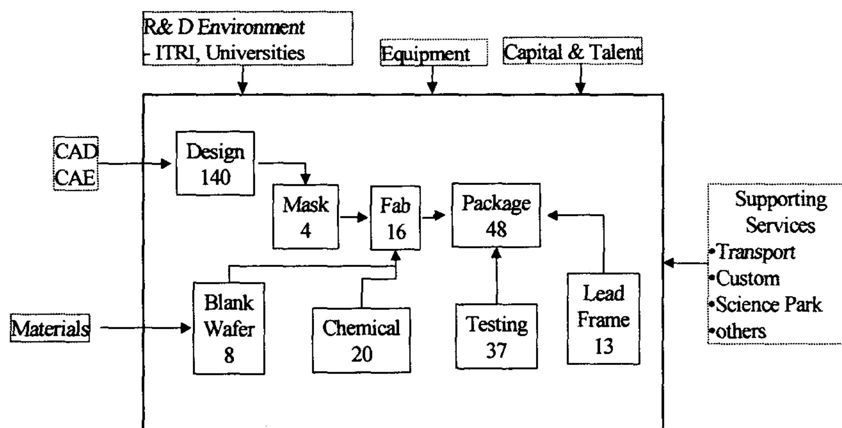

Figure 1 Infrastructures of Taiwan IC Industry

Another important issue has to be mentioned here is that the marketing sharing of the IDM orders in total packaging revenue decreases from 43.5% of 1999 to only 35.9% in 2000 which is even lower than 36.3% of year 1998. This information also significantly implies that the "winter" of the IC industry is coming, hence, the first priority for those IDM companies is to fulfill their own capacities for saving costs, rather than sub-contract it.

Revolution of Taiwan Packaging Industry

Coming from the early days of IC assembly, Taiwan packaging industry has built its own infrastructure. Following the needs of its market, advanced packaging technologies are developed to meet the requirements. In 1998-1999, owing to the new markets of wafer foundry, DRAM foundry and IDM, Area-Array packaging replaced the Lead-type packaging. PBGA and TSOP were the typical packaging types. In 2000, the panel foundry and the driver IC for TFT-LCD became the major markets, and Flip Chip technology was emerging to replace Wire Bonding technology. Where the packaging types included Enhanced PBGA, CSP/Flip Chip, Ultra-thin Package, Stacked Package and TCP.

In 2001, the new market opportunities such as high I/O IC, RF-IC and optoelectronic devices persuade Taiwan Packaging Industry to pursue new and innovative packaging technologies. To name a few there include Wafer Level Package, Ultra-thin Package, Stacked Package, Cu Chip Package, Chip on Film and Optoelectrical Package.

Packaging Technology Development in Industry

According to the revenue of different packaging types , listed as packaging distribution in Table 2, BGA and QFP are ranked the top two in 2000. However, by taking the units into consideration, BGA and CSP are the two most profitable, and CSP has the highest growth rate compared with 1999, both in revenue and units.

Table 2 Packaging Distribution, 2000

	Revenue%	Units %
CSP	5.2(0.3)	2.3(0.2)
BGA	32.3(32.6)	4.4(4.2)
QFP	28.9(26.0)	19.5(15.1)
PLCC	3.4(2.9)	4.6(4.7)
TSOP	10.7(10.2)	19.4(22.8)
SOP/SOJ	14.0(17.8)	32.4(31.4)
DIP	4.1(7.3)	8.9(16.1)
TAB	0.2(0.0)	0.2(0.0)
Others	1.3(2.9)	8.3(5.5)

( ) for 1999 Source : IT IS, IEK/ITRI, Mar. 2001

BGA and QFP might be cash cows for the packaging industry. Most revenues generated from these two types of packages occupied around one-third of revenues each. Based on the conclusions of last packaging meeting of TSIA (Taiwan Semiconductor Industry Association) held in July 2000, flip chip package was reported to be an emerging technology to meet customers' major requirement in the coming future. Of course, those tier-1 packaging houses, namely ASE, SPIL and OSE as well as many tier-2 companies are also developing the same capacity in this area to continuously enlarge their competitive edge in the near future.

Besides, due to environmental issue, most of Taiwan packaging houses are asked to provide their lead free packages by the customers in the coming future. In May 2000, *Advanced Packaging Technology Consortium*, which was held by ERSO, conducted a SIG meeting regarding the lead free issues with its 39 members. The attendants presented their lead free roadmap and customers' demands. The summaries were complied as that for system level packaging, such as notebook and desktop PCs, the lead free requirement is around by Q4, 2001; however, for component level packaging, the lead-free BGA and CSP were assumed to be ready by Q2, 2002 for most major packaging houses. Most attendee also listed their concerns about the development of lead free products, e.g. lack of lead-free standards and certification, lack of enough lead-free components for their studies, etc.

Packaging technology development in ITRI

Paralleling to the industrial efforts, institute such as ITRI (Industrial Technology Research Institute) has also devoted tremendous effort on the packaging technology. ITRI, which is a non-profit R&D organization partially funded by the Ministry of Economic Affairs (MOEA) of the ROC since 1973, has 6,000 employees distributed in seven laboratories and four centers. Among these resources, approximately 100 engineers and 6M USD budget per year have been dedicated to packaging technology development. This includes efforts from Advanced Packaging Technology Center in Electronic Research & Service Organization (APC/ERSO) and Material Research Laboratory (MRL). In the 2nd five-year packaging program, APC/ ERSO has developed many advanced IC packaging technologies, such as Cu chip packages, wafer level chip scale packages, and flip chip packages, etc, in addition to the development for the mixed mode assembly, functional substrate design, and RF packages and modules. On the other hand, MRL has been responsible for new material development, such as underfill, liquid encapsulant, and photosensitive PI. A few selected accomplishments, the present technology progress and the plans will be discussed as follows.

Cu chip package

In year 2000 and 2001 APC/ERSO has focused on the studies for the pad metallization and bondability for wire bonding packages as well as the flip chip bumping and assembly technologies for flip chip packages in Cu chip packaging project.

In the wire bonding project, a series of experiments were conducted to compare the reliability of wire bonds on four different types of pad structure, namely as copper pads without any caps, Cu-Al pad structure (aluminum capped copper pads, without any barrier layer in between), Cu-barrier-Al pad structure, and Cu-Ni-Au pad structure (electroless Nickel/gold capped copper pads).

To evaluate the quality of the wire bonds, pull tests based on MIL-STD-883E and shear tests according to JEDEC standards are conducted in the experiments.In addition to the development of wire

bonding technologies on Cu interconnect wafers in past years, the flip chip technology on Cu interconnect wafers is also developed in APC/ERSO. Both the electroplated solder bumping process with sputtered UBM (under bump metallurgy) and the process for stencil printed solder bumping on electroless plated Ni/Au UBM have been successfully developed. Table 3 shows the results of the high temperature storage for the specimens with electroless Ni/Au UBM and printed solder bumps, it could be found that the reliability result is quite good.

Table 3. High temperature storage (150C) reliability data for low cost bumps on Cu wafer

Hours	Initial	250	500	1000	1500
Shear Strength (g)	48.62	49.28	49.9	48.66	47.94
Failure	S	S	S	S	S

Failure Mode： S (Solder); U (UBM); Pad Size = 85μm; Solder Bump Height = 100μm

Wafer level chip scale package

In addition to the development for flip chip PBGAs and CSPs, efforts that include form factor design, process development and material evaluation, are also devoted on the development of wafer level CSPs in APC/ERSO. In year 2000 and 2001, one of the patented structures of wafer level CSPs that targets at high frequency memory applications has been extensively investigated. Rambus™ DRAM is employed as the test vehicle. According to the electrical simulation results listed in Table 4, this patented wafer level CSP can satisfy the harsh electrical specification that Rambus™ DRAMs required, in addition to its low stress character. The first prototype had been developed with passing the pressure cook test of 168 hours in the end of year 2000. Besides, many essential technologies of wafer level CSP have been established, such as thick (40μm) compliant layer, thick (40μm) Cu plating technologies. The process improvement was expected to be finished in August 2001. Then the wafer level CSP will be mounted on RIMM™ for reliability test.

Table 4. Electrical Simulation Results of APC/ERSO wafer level CSP (Note: not includes I/O capacitance)

Rambus DRAM Specifications		APC/ ERSO Wafer Level CSP Results
RSL pins		
L_i	max 4nH	max 2.65nH
C_i	max 0.4pF min 0.2pF	max 0.28pF min 0.25pF
ΔC_i	Max 0.06pF	max 0.03pF
L_{12}	Max 0.2nH	max 0.12nH
C_{12}	max 0.1pF	max 0.04pF
CMOS pins		
L_i	Max 8.0nH	max 1.19nH
C_i	Max 0.4pF	max 0.21pF

Lead free packages

Due to environmental and market issues, the study of green packages, including lead-free solder, halogen-free substrate, anisotropic conductive adhesion, surface mounted technology (SMT) etc, has become a hot topic recently. In order to provide a total solution, from upstream to downstream, to Taiwan's IC industry, a consortium named *Advanced Packaging Technology Consortium* was formed by ERSO/ITRI

and MRL/ITRI in 2001. Major efforts, including lead-free packaging study, are to disclosure the trends and strategies of advanced packages to its 39 members. In addition, the study of the reliability issues in the lead-free flip chip packages and SMT process as well as the development of green materials are selected as an important R&D activity in ITRI's packaging program. For the lead free SMT process study, both BGA and QFP with Sn/Ag/Cu solder mounted on FR-4 PCB were studied. It was found that the process window of reflow profile of lead free SMT is narrow than that of eutectic solder, Sn/Pb.

New Packaging Business in Taiwan

The packaging business was not as good as usual in 2001 due to the "severe winter" of IC industry. However, out of the efforts and achievements in technology development in the past, there are still new packaging companies started in niche or new opportunity markets.

In 2001, a new packaging company started their business with MEMS packaging technology. The first product will be used in mobile telecommunication. Another company, following the model of "IC design house" in IC industry, started its packaging design house business. It was at the end of last year, ITRI announced packaging technologies for 2.5 Gbps optical active component. One can thus expect some opto-electrical packaging companies in the near future. In January this year, a new plant was established that offers wafer-level CSP services including testing, packaging, burn-in and assembly for DRAM and SRAM. Services for Flash memories and consumer logic ICs will be available later this year [4].

Summary

Taiwan, a growing place with bright potential in IC packaging industry, has already focused on advanced packaging and innovative technology to meet the challenges ahead. Many packaging companies are either ready or preparing to provide their services on flip chip and wafer level CSP to their customers. On the other hand, the formation of Advanced Packaging Technology Consortium evidenced the join efforts in seeking the solutions of advanced packaging and green packaging. In order to keep the advantages from the following countries, advanced packaging technologies are essential. While in competing with the leading countries, the development of innovative technology will be the most important task. Besides all these, constantly pursing cost reduction, globalization and niche market will be the key to success for packaging business in Taiwan.

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