ISMP 2002
"The 1st International Symposium on Microelectronics and Packaging "
September 10,2002
ASEM Hall at the COEX Convention Center

" New Flip Chip Attach Technology by Bumps Formed on Substrate "

BossB²it Technology

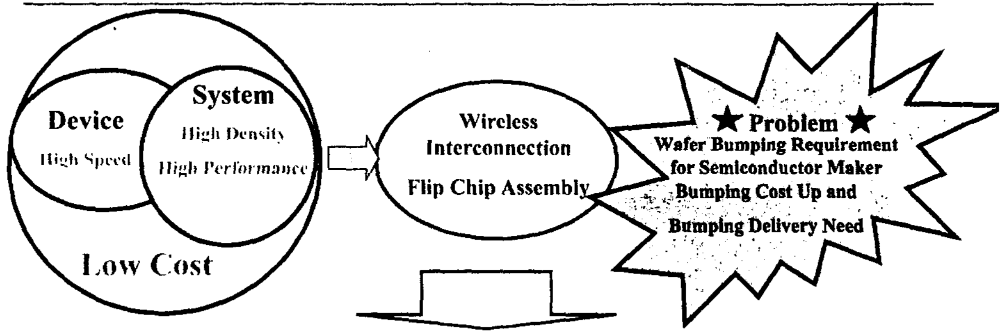
Bumps for flip chip attach formed On the Substrate with Square Bit(B²it™)

(B²it™ + FCA (Flip Chip Attach) Technology)

Weisti (Worldwide Electronic Integrated Substrate Technology Inc.)
President
Yoshitaka Fukuoka

Contents

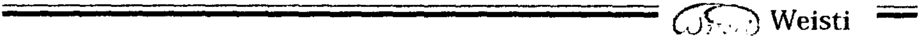
1. **Introduction**
2. **Feature, Process and Structure**
    - 2-1. BossB²it Features
    - 2-2. Structure
    - 2-3. Manufacturing Process
3. **Process Conditions and Contact Interconnection Resistance**
    - 3-1. Ag Paste Bump Forming Process Condition
    - 3-2. BossB²it New Flip Chip Attach Process Condition
4. **BossB²it Reliability**
5. **Actual MCM Development Sample and Specification**
6. **Electrical Characteristic**
    - 4-1. High Speed Logic Circuits Signal Transmission
    - 4-2. High Frequency Characteristic
7. **Cost and Development Road map**
8. **Embedded Actives & Passives Utilizing BossB²it and B²it™**

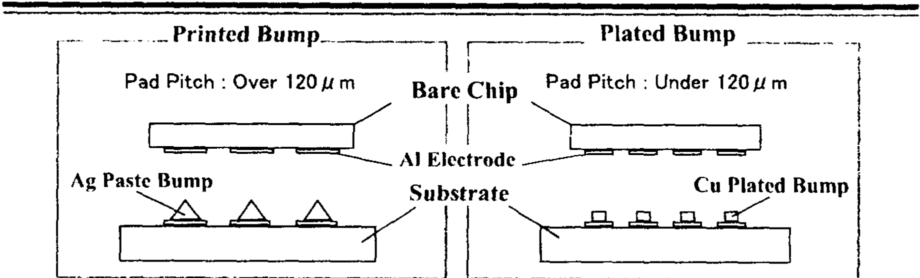


New Filp Chip Technology ; Bumps are formed on the Substrate

Every Kinds of Devices from Every kinds of Semiconductor Makers can be Used

BossB²it (B²it™+FCA)



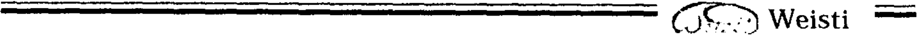


Low cost High density

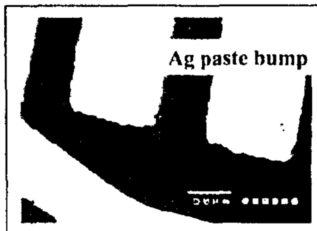
Concept & Features

- ★ Bumps are formed on the substrate for electrical interconnection between chips
- ★ No wafer bumping process (Every kinds of devices from all device maker can be used)
- ★ Short interconnection by FCA → low resistance & low inductance
- ★ High density assembly almost same as chip size
- ★ Pb free process
- ★ No cleaning process and very simple process
- ★ High performance by combining between substrate and assembly technology
- ★ Low cost and high density module can be realized by using B²it substrate
- ★ Low cost process and low cost module can be realized by underfill resin sealing

New FCA Technology *(BossB²it ; B²it™ +FCA)*

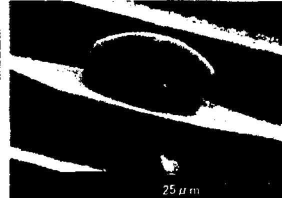


Diameter: 300 μm φ
Height : 200 μm
(a) Printed Ag paste bump



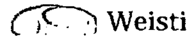
Ni/Au plating before ↑ after ↓

Diameter : 70 μm φ
Height : 20 μm
(b) Ni/Au plated Ag paste bump

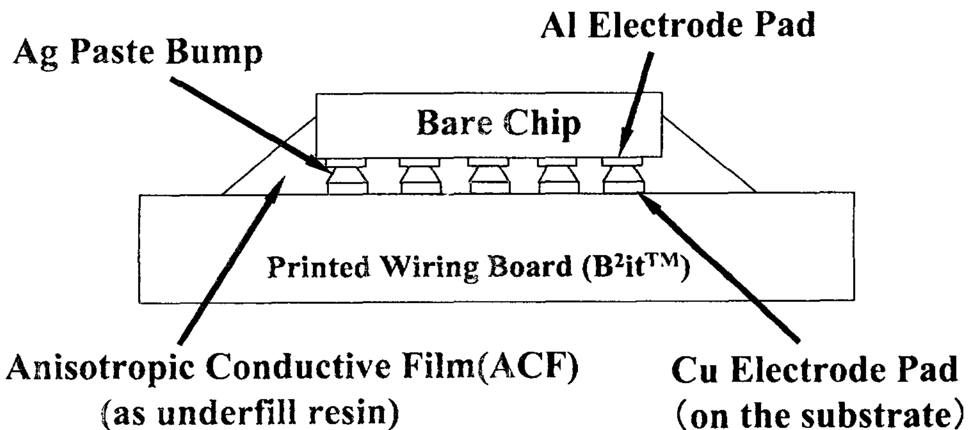


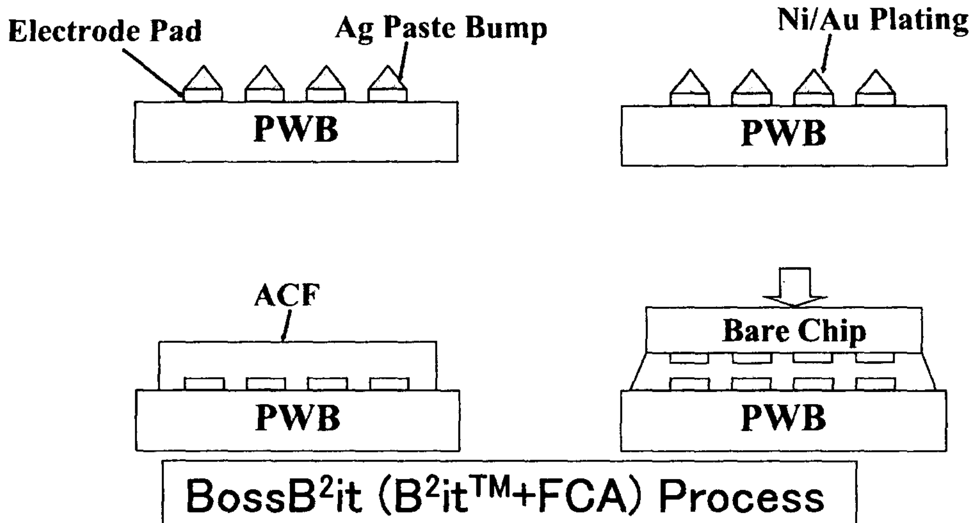
Diameter : 50 μm φ
Height : 30 μm
(c) Cu plated bump

BossB^{2}it (B^{2}it^{TM}+FCA)Each Bumps Appearance on PWB



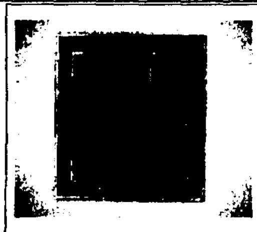
Structure of BossB^{2}it





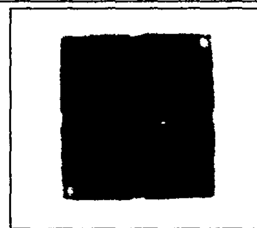
BossB²it (B²it™+FCA) Process

Weisti



Size	8×8 ×0.6mmt
Electrode material	Al
Electrode size	0.1×0.1mm
Electrode pitch	0.15/0.12 mm
Number of electrodes	184/260

(a)Test chip



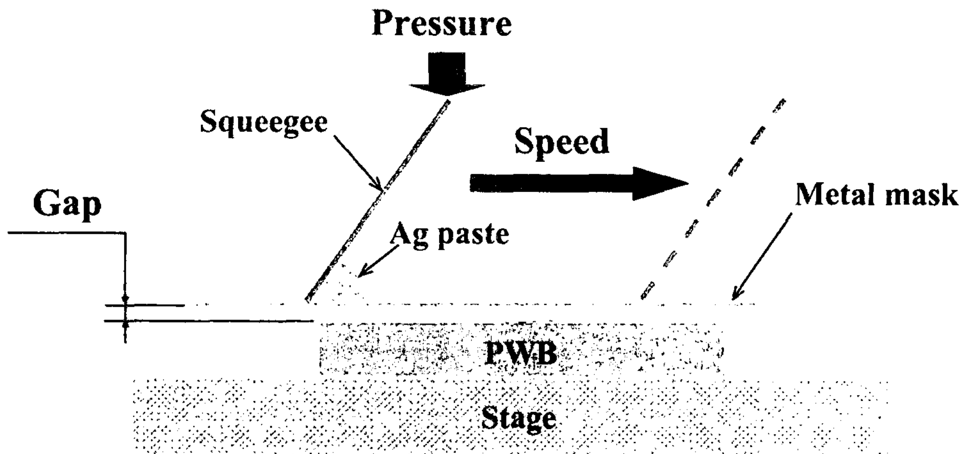
Size	38×38 ×0.6mmt
Electrode material	Cu
Electrode size	0.09×0.09mm
Electrode pitch	0.15/0.12 mm
Number of electrodes	184/260
PWB material	BT Resin

(b)Test PWB

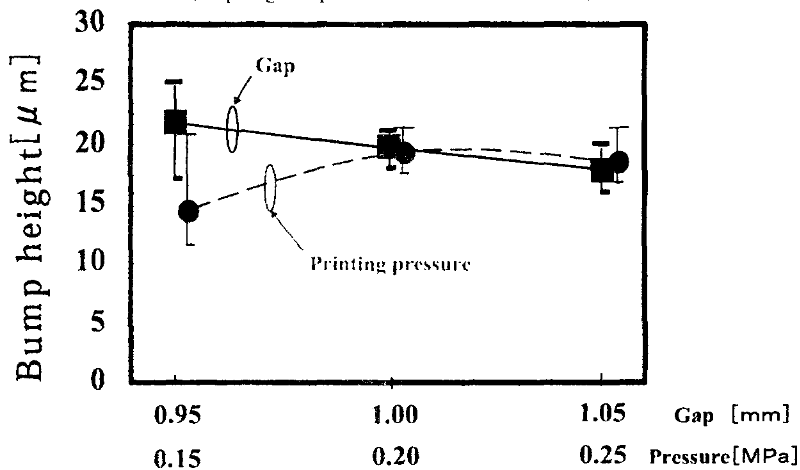
Specification of test chip and PWB

Weisti

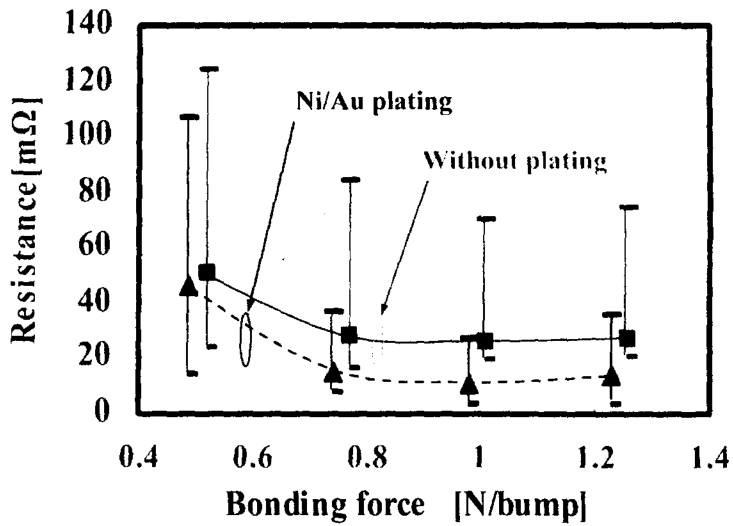
Screen printing condition



Bump height vs. Gap between metal mask and PWB vs. Printing pressure

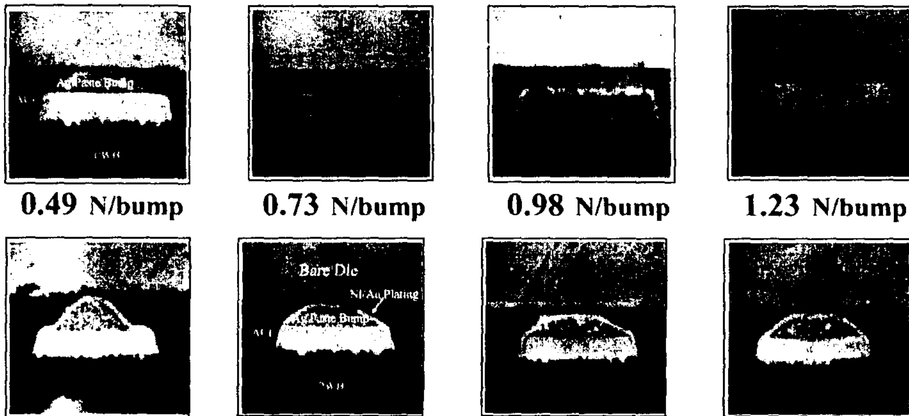


Connection resistance v.s. bonding force



Weisti

(a)Cross sectional view of Ag paste bump without plating connection

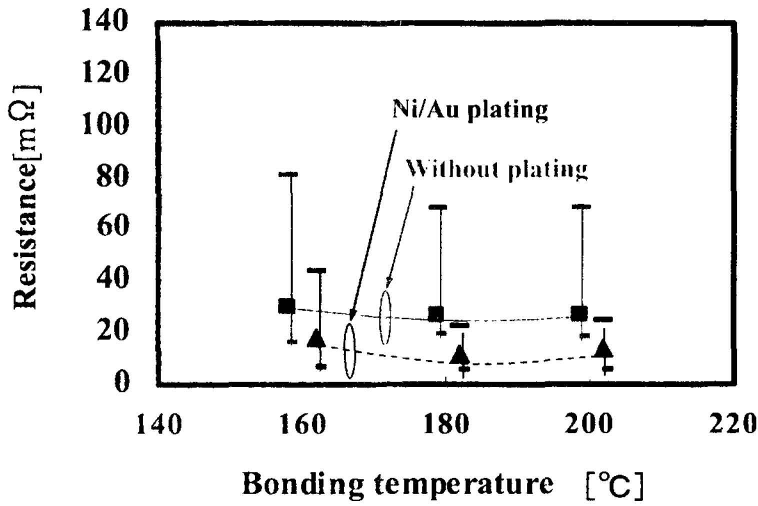


(b)Cross sectional view of Ni/Au plated Ag paste bump connection

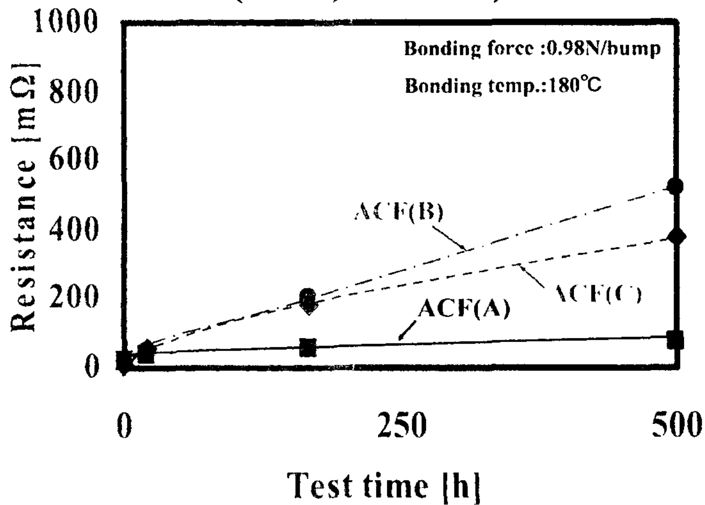
Bonding force v.s. Ag paste bump shape

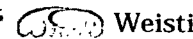
Weisti

Connection resistance v.s. bonding temperature

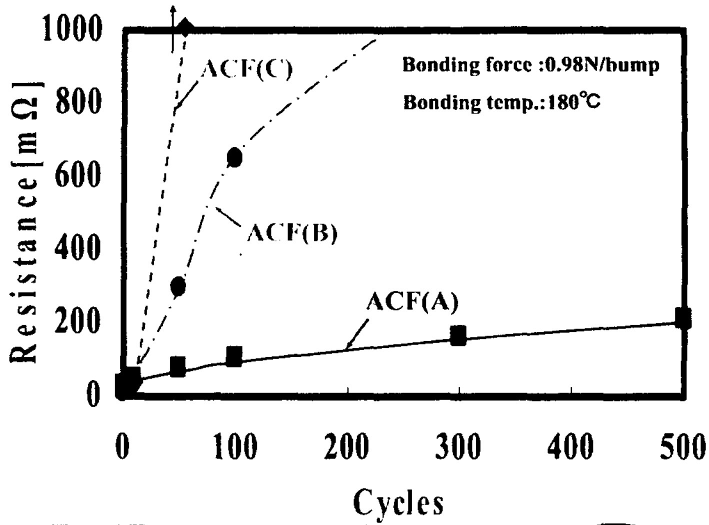


High-temperature and high-humidity test (85℃,85%RH)





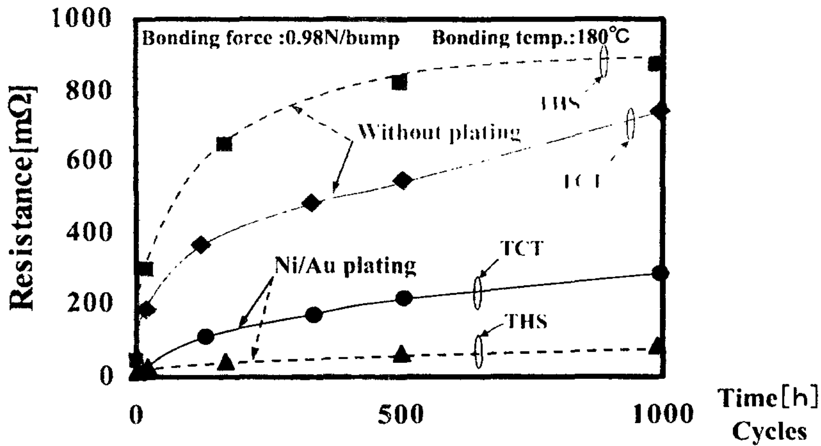
Temperature cycling test (-55°C/20min.~125°C/20min.)



Selecting ACFs

Property	ACF(A)	ACF(B)	ACF(C)
Conductive particle type	Au plated plastic ball	Ni ball	Au plated plastic ball
Tg (°C)	144	145	145
α (ppm/°C)	28	50	50
Water absorption rate(wt%)	1.3	1.4	1.4

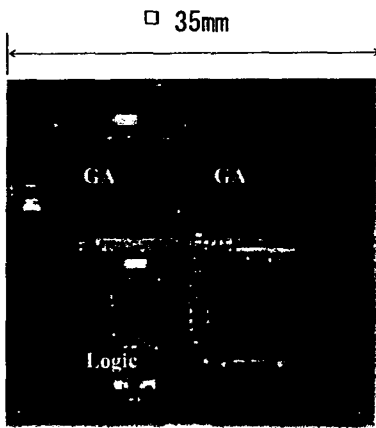
THS(85°C,85%RH)
TCT (-55°C/20min.～125°C/20min.)

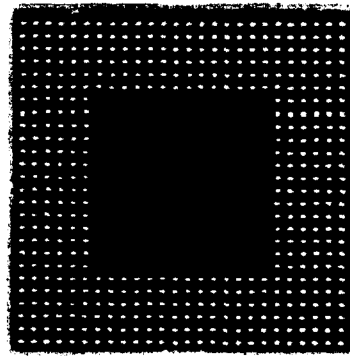


BossB²it(B²it™+FCA) Technology Result of Approval Test

No	Test item	Test condition	Judgment condition	Sample No.	Result
1	High temperature storage	125°C、1000h	Max 500mΩ or less	10p	Pass
2	Low temperature storage	-55°C、1000h	〃	10p	Pass
3	High temperature and high humidity storage	85°C、85%、1000h	〃	10p	Pass
4	Temperature cycling test	-55°C～125°C 300、1000∞	〃	10p	Pass
5	High temperature and high humidity bias	85°C、85%、5.5V 1000h	1x10 ^{8} Ω or more	10p	Pass
6	Mechanical shock	1m height dropping 6 directive 20 times	Max 500mΩ or less	10p	Pass
7	Vibration fatigue	20～2000Hz 20G	〃	10p	Pass
8	Visual inspection	Position accuracy	No problem	1p	Pass
9	SEM inspection	Connection cross section	No problem	1p	Pass
10	Pull strength test	Initial	8mm:40N or more 12mm:75N or more	5p	Pass
11	〃	Pre-condition and after reflow		5p	Pass
12	〃	After each test		5p	Pass
13	Initial connection resistance measurement	Connection resistance and dispersion	Process capability :Cp=1.33 or more	100p	Pass

□ 35mm





(a)Surface(Chip attach side)　(b)Back side (I/O side)

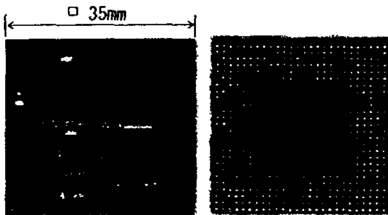
Real operating MCM for BGA type

Weisti

BossB²it (B²it™+FCA)Technology MCM

Buried Bump Interconnection Technology & Flip Chip Attach

□ 35mm

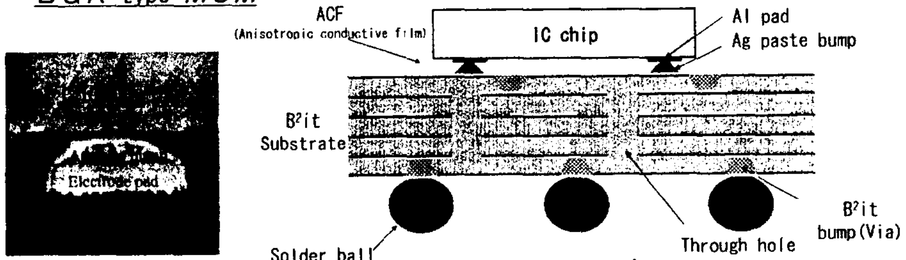


BGA type MCM

Specification

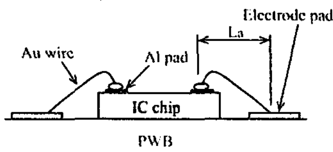
FCA　Ag paste bump Diameter: φ70μm
Height : ᵗ20μm
Pad pitch 150μm(Line/Space=90/60μm)

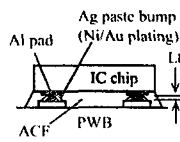
B²it Substrate
Layer : 6
Thickness : ᵗ0.7mm
B²it bump / Land : φ200 / φ400μm
Through hole / Land : φ300 / φ600μm
Material : BT Resin

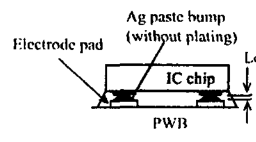


Connection of BossB²it(B²it+FCA)　Cross section

Weisti







Wire-Bonding technology

La = 1.5 mm

BossB²it(B²it™+FCA) technology

Lb = Lc =0.02 mm

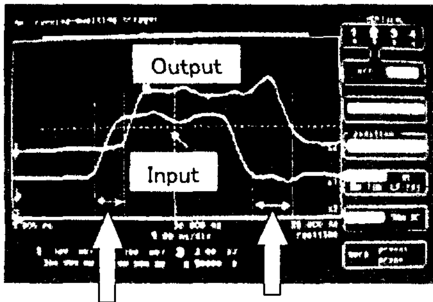
Connection resistance

Ave. 0.5 mΩ(Ra)	Ave. 11 mΩ(Rb)	Ave. 44 mΩ(Rc)
Max. 1.0 mΩ	Max. 27 mΩ	Max. 70 mΩ

$Ra < Rb < Rc$

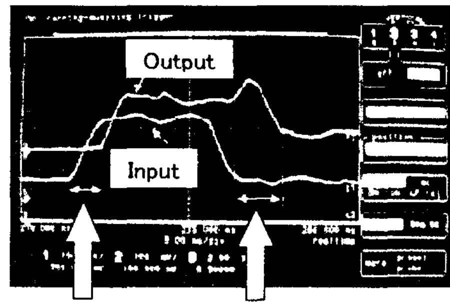
Wiring length and connection resistance comparison between BossB²it technology and conventional Wire-Bonding technology

Signal Waveform in BossB²it



3.51ns 3.69ns

Signal Waveform in Wire-bonding

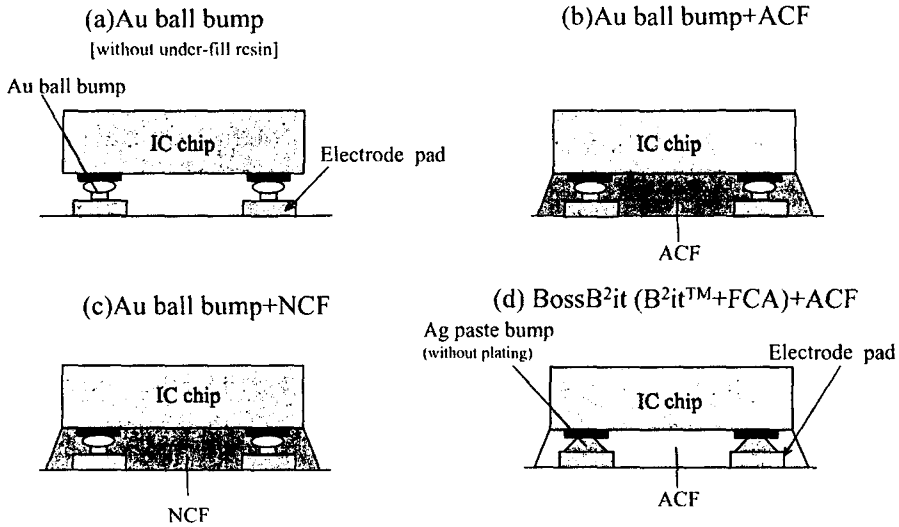


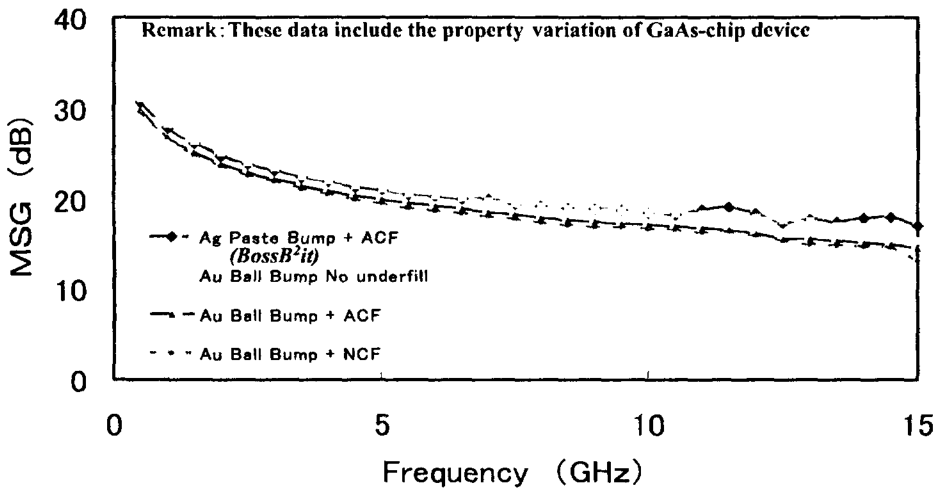
3.58ns 3.72ns

Rising and falling delay time of input/output signal:
BossB²it (B²it™+FCA) technology < Wire-bonding technology

Electrical signal propagation comparison between BossB²it technology and conventional Wire-Bonding technology

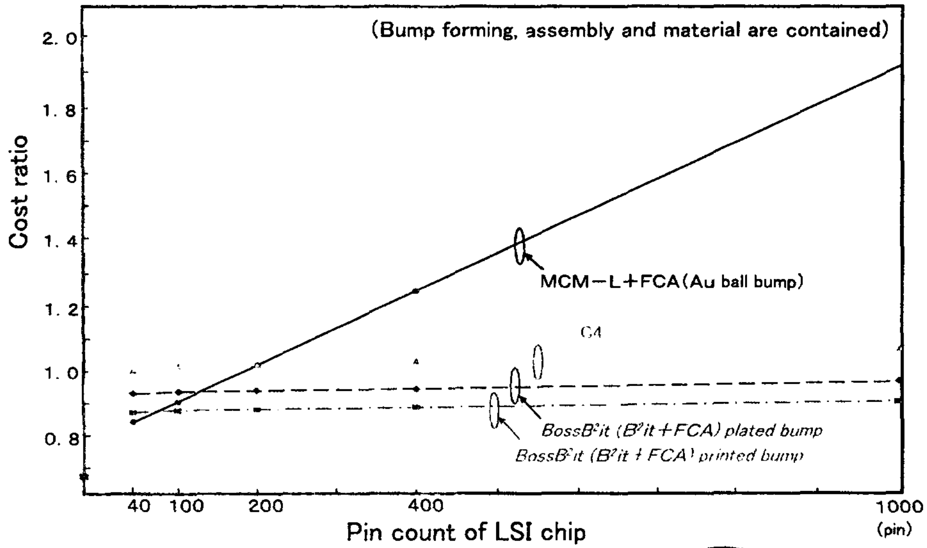
Each structure of FCA



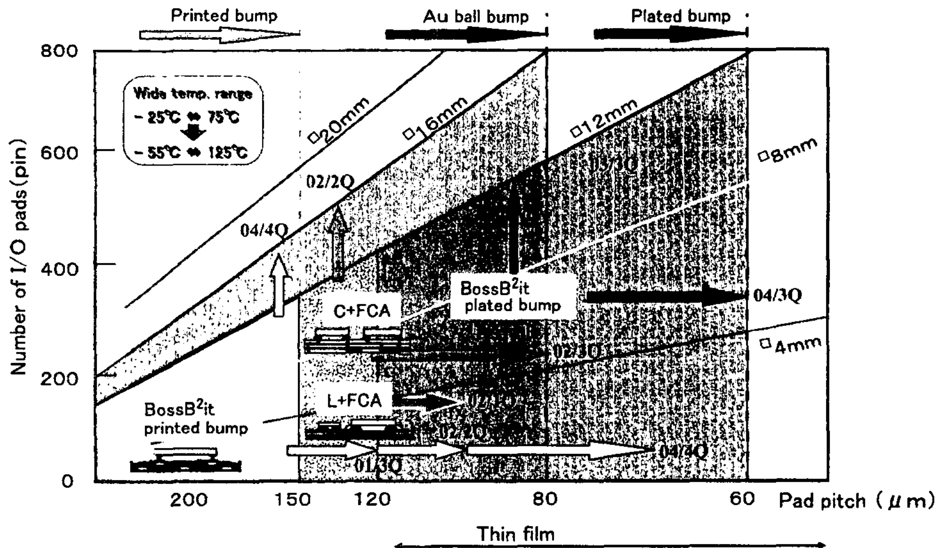


MSG Property : Ag paste bump(using ACF) > Au ball bump(without under-fill resin)

MSG(Maximum Stable power Gain) **Property under High-frequency**

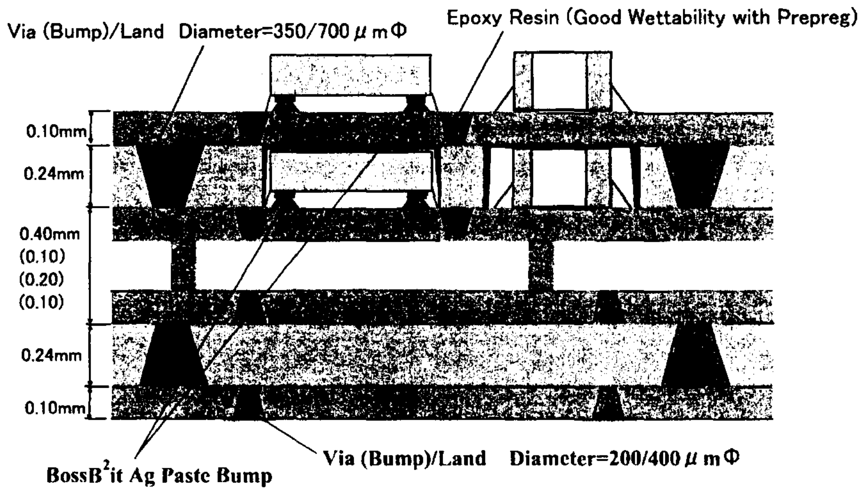

Cost comparison among each Flip Chip Attach technology
(Bump forming, assembly and material are contained)
Cost ratio
2.0
1.8
1.6
1.4
1.2
1.0
0.8
MCM−L+FCA(Au ball bump)
C4
BossB²it (B²it+FCA) plated bump
BossB²it (B²it+FCA) printed bump
40
100
200
400
1000
(pin)
Pin count of LSI chip

Weisti

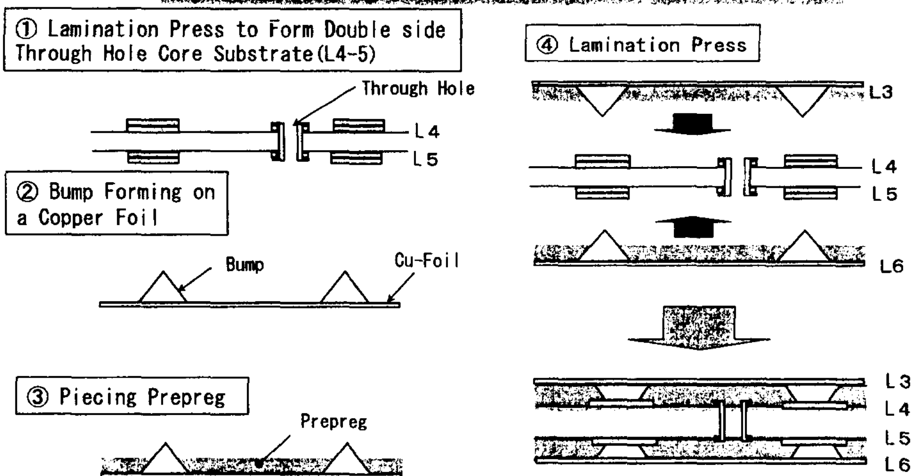

FCA technology development road map
Printed bump
Au ball bump
Plated bump
Number of I/O pads (pin)
800
600
400
200
0
Wide temp. range
−25℃ ⇔ 75℃
−55℃ ⇔ 125℃
□20mm
□16mm
□12mm
□8mm
□4mm
02/2Q
04/4Q
C+FCA
BossB²it
plated bump
04/3Q
L+FCA
BossB²it
printed bump
01/3Q
02/3Q
02/2Q
04/4Q
200
150
120
80
60
Pad pitch (μm)
Thin film

Weisti

Embedded Actives and Passives Device B^2it™ Substrate Structure with BossB²it FCA Technology

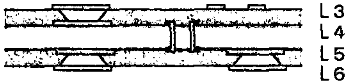


Embedded Actives and Passives B²it Substrate Fabrication Process Flow (1/3)

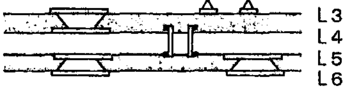


Embedded Actives and Passives B²it Substrate Fabrication Process Flow (2/3)

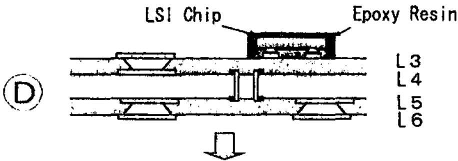
⑤ Patterning (L3-L6)



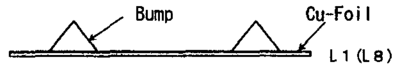
⑥ BossB²it™ Bump Forming



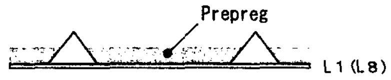
⑦ FCA(BossB²it™)



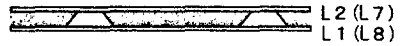
⑧ Bump Forming on a Cu-Foil



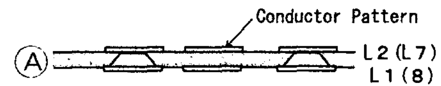
⑨ Piecing Prepreg



⑩ Lamination Press to Form Double Side B²it Core Substrate



⑪ Patterning (L1/L2 & L7/L8)



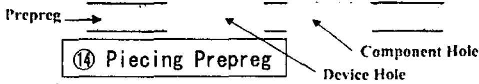
Weisti

Embedded Actives and Passives B²it Substrate Fabrication Process Flow (3/3)

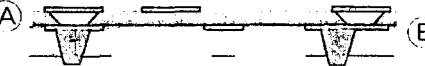
⑫ Bump Forming on Core B²it Substrate

⑬ Component & Device Hole Forming

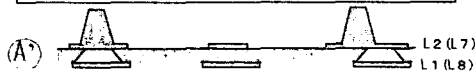
⑭ Piecing Prepreg



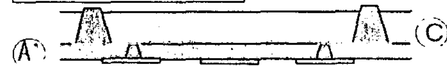
⑮ Bump Forming on Core B²it Substrate

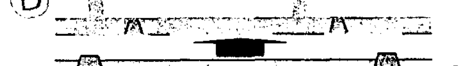


⑯ Piecing Prepreg

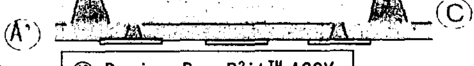
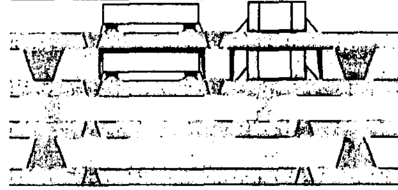


⑰ Lamination Press





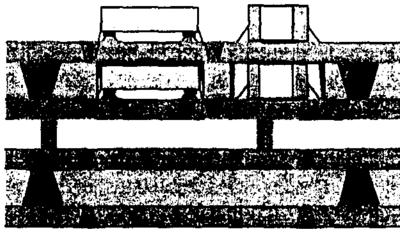
⑱ Device BossB²it™ ASSY

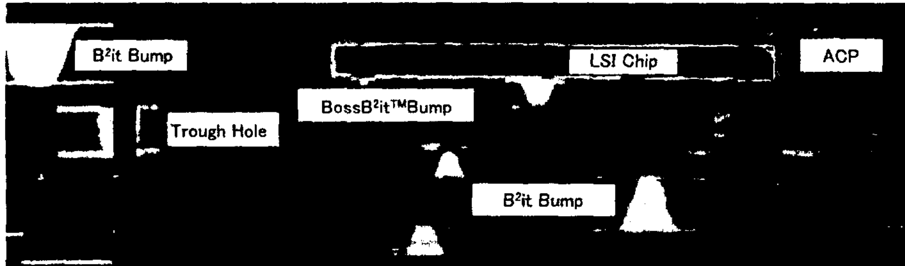
Weisti

3D-Mounting Structure with Embedded Actives & Passives Utilizing B²it™ and BossB²it Technology

Cross Sectional Structure



Cross Sectional Photograph



Conclusions

(1) New flip chip attach technology named BossB²it™ have been developed in which bumps are formed on the substrate without bump formation process on the semiconductor device aluminum electrode.

(2) Good reliability of BossB²it™ have been confirmed by not only various kinds of advanced reliability test measuring the contact resistance change by many kinds of TEG but also many kinds of actual multi chip module reliability tests using developed multi chip module utilizing BossB²it™ technology.

(3) BossB²it™ technology is extremely cost attractive because BossB²it™ process is extremely simple and dry as compared with the other flip chip attach technology such as C4(Controlled Collapse Chip Connection) and Au stud bump technology even if the device pin counts are increasing. Furthermore, severe coplanarity and surface flatness control does not required to the substrate in BossB²it technology.

(4) Better electrical characteristics of BossB²it™ have been confirmed as compared with conventional Chip & Wire assembly technology. Furthermore, good high frequency electrical characteristics of BossB²it™ have been confirmed as compared with Au stud bump technology.

(5) Narrower bump pith for larger chip size in the application of BossB²it™ has been developing consequently. Furthermore, embedded actives and passives utilizing both BossB²it™ and B²it™ has been developing for the high density 3-dimensional mounting technology.