Reducing Electromagnetic Radiation in Split Power Distribution Network of High-Speed Digital System

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Abstract

Electromagnetic(EM) radiation problems and their possible solutions are addressed in this paper for the split power plane of high-speed digital systems. Stitching and decoupling capacitors are proved to be very effective for reducing signal noise, ground bounce as well as electromagnetic radiation from the split power plane. Simulations based on 3D-Finite Difference Time Domain (FDTD) method are utilized for the analysis of practical high frequency multi-layered PC main board

Key words: FDTD, split power plane, EMI, stitching and decoupling capacitor

I. INTRODUCTION

In modern high performance microprocessor design, multiple power and ground planes are indispensable elements due to the requirement of various power sources. However, the split reference plane causes serious signal integrity problem as well as electromagnetic (EM) radiation, affecting the performance of high-speed microprocessor circuit board. Spurious electromagnetic radiation occurs from the split power plane discontinuity, because currents are forced to flow around the slot and charges accumulate on its edges. As the current travels down the trace, the return current is induced on the reference plane. When signal reaches the gap, one portion of the reference current propagates across the gap via the gap capacitance, and the other portion is forced to travel around the gap or reflected backward. Both coupling and radiation caused by non-ideal return current path could lead to deteriorated signal integrity as well as electromagnetic compatibility problems in high-speed digital circuit. Works have been done to analyze noise tendency in this discontinuity model especially in signal distortion on transmission line [1][2][3].

This paper verifies the level of signal noise from different point of views such as scattering parameter, time domain noise distribution as well as EM radiation with and without placing the stitching and decoupling capacitors in small practical micrometer trace and slot structure.

II. RETURN CURRENT AND MODE CONVERSION AT POWER SPLIT

The signal line above the slot in the power plane is modeled as series inductor, and the decoupling or stitching capacitors are added near the slot to compensate signal noise due to the series inductance effect. As shown in Fig. 1, the return current from driver at *A* cannot flow directly under the trace between *A-B*. Instead, it diverts around the ends of the power plane slot. The diverted current makes a large loop, increasing the inductance of signal path *A-B*, which effectively makes large loop antenna as a source of EM radiation. The stitching capacitor method provides direct return path on power plane, while the decoupling method creates return path below the slot by changing reference planes; this is, power plane to ground plane and vice versa.

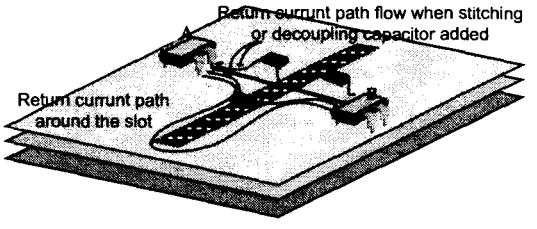

Fig. 1. Return current path in split power plane

In Fig. 2, FDTD results are shown for a Gaussian pulse propagating on a microstrip that crosses a split power plane. When pulse reaches to the slot, the snapshot of the absolute electric field strength which is obtained above one cell from power plane shows four distinct pulses: the forward and backward scattered pulses on the microstrip and two excited pulses on the power plane slotline.

Fig. 3 shows propagating pulse at each three port (microstrip input port, output port and power plane slotline port) in time domain.

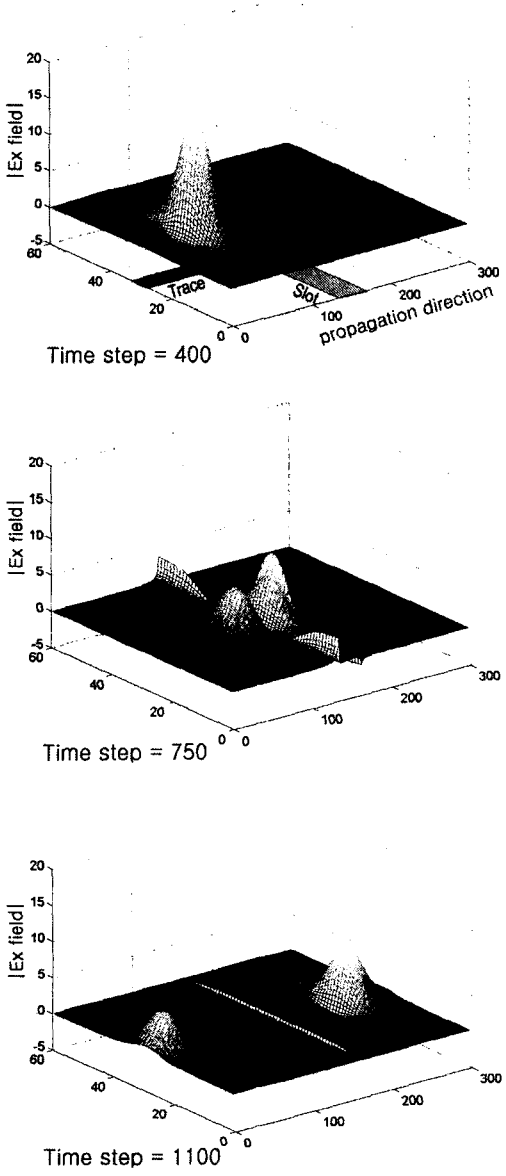

Fig. 2. Mode conversion on power plane using FDTD

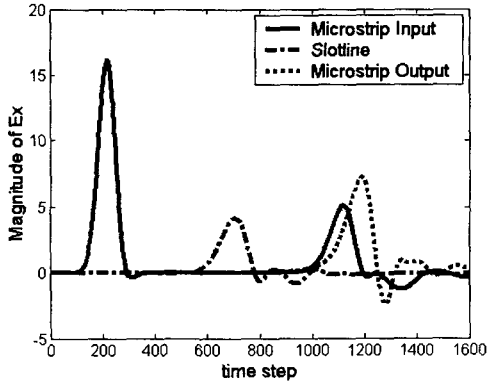

Fig. 3. Pulse scattering on the power plane

III. DESIGN AND FABRICATION

For the characterization of the split power plane, practical 4-layer personal computer main board has been modeled with FDTD method as shown in Fig. 4. The microstrip line has 150 μm width and is crossing the 750 μm open slot printed on the FR4 substrate of ε_r=4.4 and 125 μm thickness, the substrate between power and ground plane has 1000 μm thickness. In stitching method, capacitor is placed between two power planes with different potentials, while in decoupling method, capacitor is located between the power and ground planes. These two methods are designed to provide well-established return current path to reference plane.

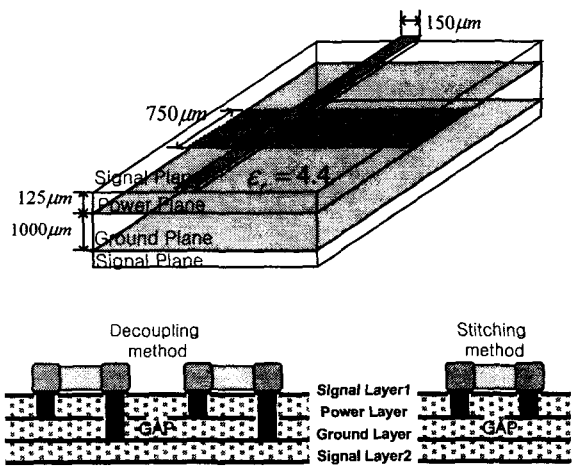

Fig. 4. PCB simulation structure with decoupling and stitching capacitor

As a modeling effort, electrode resister and equivalent series inductance are included for capacitor model for better accuracy as seen in Fig. 5, and 3-D FDTD method generally used in the analysis of a planar structure is applied to analyze the modified circuit including lumped elements. The extended Maxwell equation including lumped element within one cell can be obtained by adding a component of a current source [4][5][6].

Extended Maxwell equation in FDTD

$$E_z^{n+1}(i,j,k) = E_z^n(i,j,k) + \frac{\Delta t}{\varepsilon_0}\nabla \times H^{n+1/2}(i,j,k) - \frac{\Delta t}{\varepsilon_0 \Delta x \Delta y} I_L^{n+1/2}(i,j,k)$$

For modeling of capacitor C

$$E_z^{n+1}(i,j,k) = E_z^n(i,j,k) + \left(\frac{\frac{\Delta t}{\varepsilon_0}}{1 + \frac{C\Delta z}{\varepsilon_0 \Delta x \Delta y}} \right) \nabla \times H^{n+1/2}(i,j,k)$$

For modeling of resistance R

$$E_z^{n+1}(i,j,k) = \left(\frac{1 - \frac{\Delta t \Delta z}{2R\varepsilon_0 \Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R\varepsilon_0 \Delta x \Delta y}} \right) E_z^n(i,j,k) + \left(\frac{\frac{\Delta t}{\varepsilon_0}}{1 + \frac{\Delta t \Delta z}{2R\varepsilon_0 \Delta x \Delta y}} \right) \nabla \times H^{n+1/2}(i,j,k)$$

For modeling of inductance L

$$E_z^{n+1}(i,j,k) = E_z^n(i,j,k) + \frac{\Delta t}{\varepsilon_0}\nabla \times H^{n+1/2}(i,j,k) - \frac{\Delta z (\Delta t)^2}{\varepsilon_0 L \Delta x \Delta y} \sum_{m=1}^{n} E_z^m(i,j,k)$$

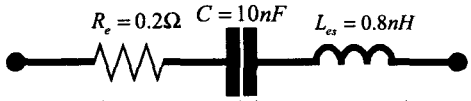

Fig. 5. Equivalent circuit model for 10nF ceramic capacitor

IV. SIMULATION AND RESULT

Time domain results and their Fourier transform was achieved for proving the effect of stitching and decoupling capacitors around the split in power plane using FDTD. When decoupling capacitors are placed between the power and ground planes, the return loss as well as insertion loss characteristics, especially in the low frequency region, are improved as shown in Fig. 6 and Fig. 7. This is mainly due to the return current path established by the capacitors. Even further improvement is possible with the use of stitching capacitors, which can be clearly seen in Fig. 6 and Fig. 7, due to the more reduced return current path compared to the previous approach.

The electromagnetic radiation caused by a non-ideal return path is proportional to the total loss, and the calculation shows that the total loss ($1-|S_{11}|^2-|S_{21}|^2$) can be reduced by adapting decoupling or stitching capacitor as shown in Fig.8. Another point of signal integrity issue is the ground switching noise or ground bounce. Due to the slot in the reference plane, current is forced to flow along the slotline in the power plane and travel on ground plane, which causes ground bounce. The ground bounce also can be alleviated by stitching or decoupling capacitor as depicted in Fig. 9.

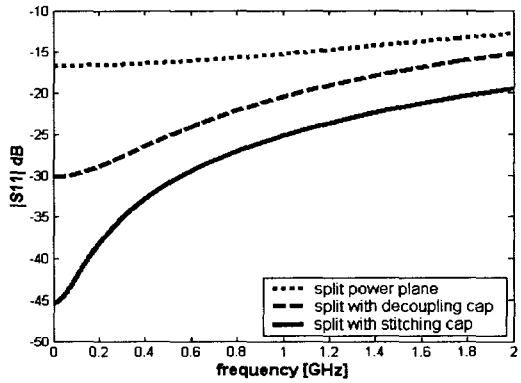

Fig. 6. Return loss of the split power plane

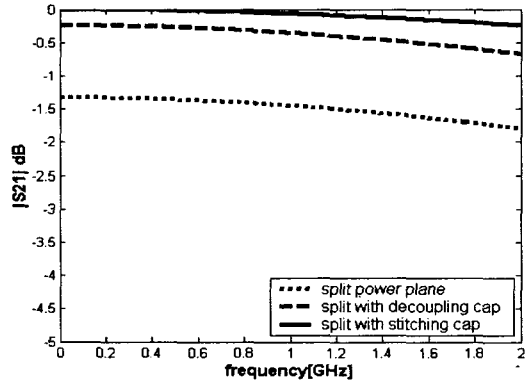

Fig. 7. Insertion loss of the split power plane

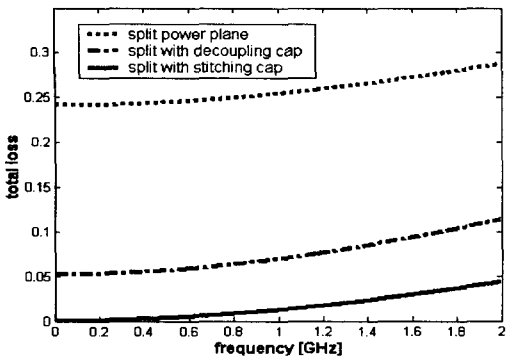

Fig. 8. Total loss of split power plane

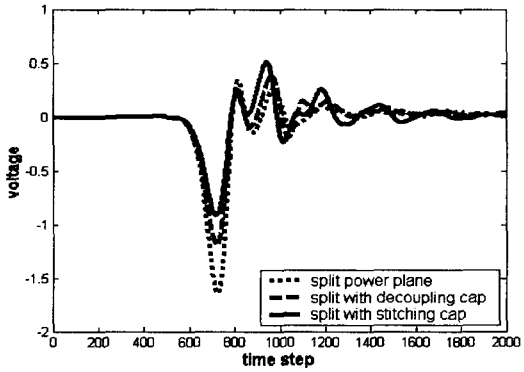

Fig. 9. Ground bounce of split power plane

V. CONCLUSION

In this paper, signal integrity issues in the high-speed digital signal line passing through the slot in the power plane are addressed based on 3D-FDTD simulation. The effectiveness of the decoupling and stitching capacitors have been proven as far as the EMI problem concerns in the practical PC main board design. With the stitching capacitor in the slot, the return loss and total loss are reduced effectively. Further, the ground bounce is reduced to 60%.

REFERENCES

[1] Haw-Jyh Liaw and Merkelo H, "Signal integrity issues at split ground and power planes," 46th *Electronic Components and Technology Conference,* pp. 752 – 755, 1996.

[2] Christian Schuster and Wolfgang Fichtner, "Parasitic modes on printed circuit boards and their effect on EMC and signal integrity," *IEEE Transactions on Electromagnetic compatibility,* Vol. 43, No 4, November 2001.

[3] Ilavarasan, P., Juan Chen, Schaffer, M., Norman, A. J., "Simulation/experimental analysis of single/differential signals crossing splits." *2001 International symposium on Electromagnetic compatibility*, pp. 667-670, vol. 1, 2001.

[4] Sui W, Christensen D. A and Durney C. H, "Extending the two-dimensional FDTD method to hybrid electromagnetic systems with active and passive lumped elements," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 40, pp. 724 –730, April 1992.

[5] M. J. Piket-May, A Taflove and J. Baron, "FD-TD Modeling of Digital Signal Propagation in 3D Circuits with passive and active loads," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 42, pp. 1514-1523, August 1994.

[6] 황윤재, 육종관, 박한규, "FDTD를 이용한 마이크로파 능동회로의 해석," 한국전자파 학회 논문지, Vol. 13, No.6, pp. 528-537, 2002.