A CMOS Downconversion Mixer for 2.4GHz ISM band Applications

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Abstract

This paper demonstrates a CMOS downconversion mixer for 2.4GHz ISM band applications. The mixer, implemented in a 0.18um CMOS process, is based on the CMOS Gilbert Cell mixer. With a 2.5GHz local oscillator and a 2.45GHz RF input, the measurement results exhibit power conversion gain of -6 dB, IIP3 of -6 dBm, input P_{-1dB} of -15 dBm, and power dissipation in mixer core of 2.7 mW with 0dBm LO power and 1.8V supply voltage.

Keywords — Downconversion mixer, Gilbert Cell, conversion gain, IIP3, input P_{-1dB}

1. Introduction

It is not too much to say that the topic of the 21st century is wireless. Moreover, the communication wireless systems have been improved, keeping pace with advances in process technology, and the frequency band of wireless communication standard is getting higher. Specially, the deep submicron CMOS can meet the demand for low cost and high performance in low GHz frequency range [1]. Therefore the CMOS RF ICs technology has become the attractive replacement of GaAs MESFET, Bipolar and Bi-CMOS. The down-conversion mixer is an essential building block, which is located after LNA in the receiver path. Thus, it determines system performance.

In this paper, a modified architecture of the CMOS Gilbert Cell mixer for low supply voltage and high frequency performance is presented. And the circuit design, analysis, simulation, and measurement results of the CMOS downconversion mixer for 2.4GHz ISM band applications are described

2. Circuit Design and Analysis.

The schematic diagram of the down-mixer is shown in Figure 1. The RF input stage is a grounded-source pair topology for the reduction of stacked transistors and has a cascode structure for better high frequency performance. The output buffer is added for measurement to drive 50Ohm.

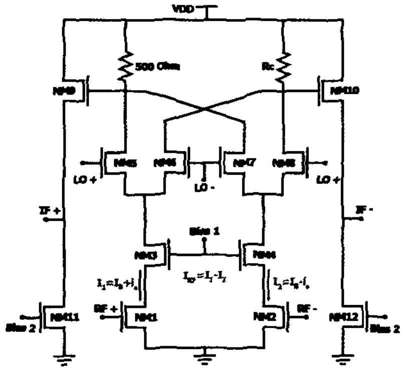

Figure 1. Down-mixer Schematic

The grounded-source pair in RF input stage has less IM products, compared to a differential pair with a constant tail current. Using the MOSFET I-V characteristics including short channel effects [2], the Kirchhoff's voltage law, and Volterra series technique [3, 4], we can calculate the differential current I_{RF} as a function of the signal source voltage V_{in}:

$$I_{RF} = \alpha_1 V_{in} + \alpha_3 V_{in}^3 \dots$$

$$\alpha_1 = K\left[\frac{V_{od}(2+\theta V_{od})}{F(1+\theta V_{od})^2}\right] \qquad (1)$$

$$\alpha_3 \approx \frac{K\theta}{4F^3(1+\theta V_{od})^4}\left[K\frac{XV_{od}(2+\theta V_{od})}{F(1+\theta V_{od})^2} - 1\right]$$

where

$$F = X\left[\frac{KV_{od}(2+\theta V_{od})}{(1+\theta V_{od})^2}\right] + sC_{gs}(Z_S + Z_G) + Y$$

$$X = \frac{Z_S g_{ds} + Z_G sC_{gs}}{g_{ds} + sC_{gs}}$$

$$Y = 1 + (Z_S + Z_G)\left(\frac{g_m sC_{gs} + g_{ds} sC_{gd}}{g_{ds} + sC_{gs}}\right)$$

and $K=(\mu C_{OX}/2)*(W/L)$. μ is the carrier mobility, C_{OX} the gate-oxide capacitance per area, $V_{od}=V_{GS}-V_{th}$(V_{GS} is the gate-source dc voltage, and V_{th} the threshold voltage of MOS transistor), $s(=j\omega)$ the Laplace variable, and θ the mobility degradation factor [2]. Z_G is the impedance at gate of NM1, which composed of the source resistance R_{source}, gate poly resistance, the impedance of bias T, and the impedance of matching network, and Z_S is the impedance at source-node of NM1 due to interconnection metal, bonding wire, and pad parasitic components. Also, the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, the output conductance g_{ds}, and the transconductance g_m, which are MOSFET intrinsic parameters [2], are used to derive (1).

Assuming the complete switching of LO driven transistors, the output voltage at a differential load resistance R_C can be expressed as:

$$V_{out} = \frac{4R_C}{\pi}\left[\frac{KV_{od}(2+\theta V_{od})}{F(1+\theta V_{od})^2} V_{in}\right]\cos(\omega_{LO} \cdot t) \qquad (2)$$

For a narrowband RF input $V_{in}=V_{RF}\cos(\omega_{RF}t)$, we can obtain the desired IF by multiplying ω_{RF} and ω_{LO} together. So the voltage conversion gain A_V and the power conversion gain A_P are given by [5]:

$$A_V = \frac{2}{\pi}G_m R_C,\ A_P = A_V^2\frac{R_{source}}{R_C} \qquad (3)$$

$$G_m = \left|\frac{KV_{od}(2+\theta V_{od})}{F(1+\theta V_{od})^2}\right|$$

So the conversion gain is controlled by the overall transconductance G_m and R_C.

The next analysis, nonlinearity is mainly affected by the RF input stage if the LO switching pair stage guarantees the complete switching [6]. From (1), we can find the first, third Volterra series coefficients. Using those, the non linearity equation is derived as [5] :

$$A_{IIP3} = \sqrt{\frac{16}{3} \cdot \frac{\left|F^3 V_{od}(1+\theta V_{od})^4 (2+\theta V_{od})\right|}{\left|(K \cdot X - F \cdot \theta)(1+\theta V_{od})^2 - K \cdot X\right|}} \quad (4)$$

The main noise soureces of the Gilbert mixer type are noise of the RF input stage and that of the LO-driven transistors. The SSB noise figure [5] of the presented down conversion mixer can be approximated as the following analytical expression [7] :

$$NF_{SSB} \approx \frac{(G_m R_{source} + 2\gamma)G_m + 4\gamma \frac{2 I_B}{\pi V_{LO}} + 1/R_C}{(2G_m/\pi)^2 R_{source}} \quad (5)$$

Where γ is the channel noise factor, which is 2/3 for long channel MOSFET's but can be higher in short channel device [8], and V_{LO} is LO amplitude.

According to (3), (4) and (5), the circuit performance can be improved by increasing V_{od}, but due to voltage head room problem and increasing power consumption [4], the trade-off is needed to low power application. The theoretical performance of mixer is summarized in Table 1.

Table 1. The theoretical performance

Parameters	Theory
A_V / A_P	14 dB/4 dB
Input P_{-1dB}	−6 dBm
IIP3	3.6 dB
NF_{SSB}	8.3 dB
Power	3.06 mW

3. Simulation Result

The power conversion gain is illustrated in Figure 2. According to the Figure, the power conversion gain is -2 dB upto the RF power of −18 dBm. It is lower than the analytical result, because of the -3 dB insertion loss of balun at RF and LO input. The IIP3 versus RF input power is shown in Figure 3. The IIP3 is about 9 dBm lower than the analytical result, due to nonlinear shunt capacitances C_{gs} and C_{gd} in LO-driven MOS transistors mainly. The noise figure is plotted on Figure 4. The NF_{SSB} is 8.1 dB at a 2.45GHz RF input, which is contributed by 2~3 dB at RF input stage, about 5 dB at LO switching stage and NF at the other noise sources [7].

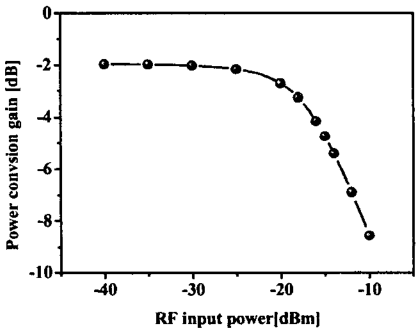

Figure 2. A_P versus RF input power

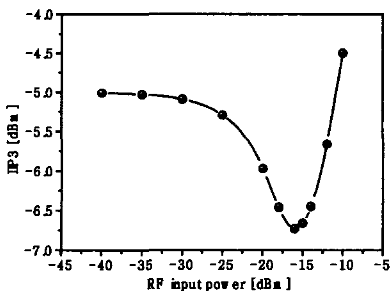

Figure 3. IIP3 versus RF input power

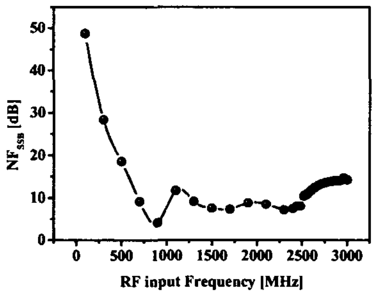

Figure 4. NF_{SSB} versus RF input Frequency

4. Measurement Results

The fabricated chip was attached to FR4 board and wire-bonded for testing. Discrete RF baluns were used for differential signal of RF and LO input. Figure 5 shows test jig for measurement. Setting RF input power to -30 dBm at 2.45GHz and LO input power to 0 dBm at 2.5GHz, the IF spectrum of the single tone test is shown in Figure 6. The power conversions gain versus RF input power is illustrated Figure 7. After sweeping the LO input power from -5 dBm to +3 dBm, the measured power conversion gain is shown in Figure 8. When a two-tones RF input power -30dBm at 2.45GHz±200KHz are mixed the LO input frequency, the output IF spectrum is displayed in Figure 9.

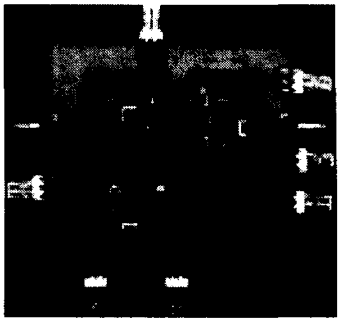

Figure 5. Test jig for measurement

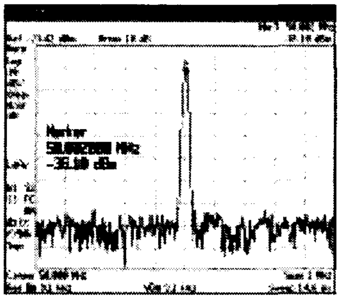

Figure 6. IF spectrum of the single tone test

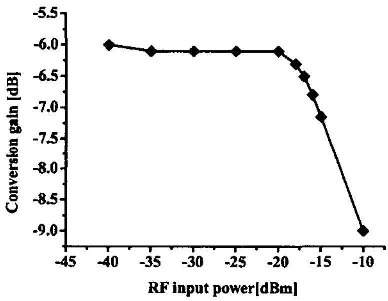

Figure 7. A_P versus RF input power

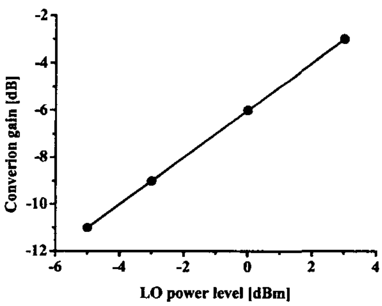

Figure 8. A_P versus LO power level

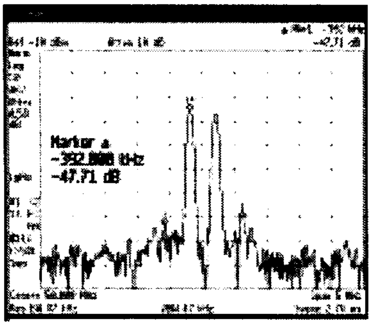

Figure 9. IF spectrum of the two tone test

5. Conclusion

The RF downconverison mixer for 2.4GHz ISM band applications, has been fabricated using 0.18um CMOS process, and measured to validate the theory and simulation results. The performance of the presented circuit are summarized in Table 2. The measured results do not match the theory and simulation results due to the loss of SMA connector, the access insertion loss of balun, the switching efficiency of LO−driven transistors, and parasitic capacitances in the signal path. The measurement of noise figure and port−to−port isolation is under progress.

Table 2. Down−mixer performance summary

Parameters	Theory	Sim.	Mear.
A_P	4dB	−2dB	−6.1dB
Input P_{-1dB}	−6dBm	−18dBm	−15dBm
IIP3	3.6dBm	−5dBm	−6dBm
NF_{SSB}	8.3dB	8.1dB	
Power	3.06mW	2.7mW	2.7mW

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