Low-Power Wide-Tuning Range Differential *LC*-tuned VCO Design in Standard CMOS

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Abstract

This paper presents a fully integrated, wide tuning range differential CMOS voltage-controlled oscillator, tuned by pMOS-varactors. VCO utilizing a novel tuning schme is reported. Both coarse digital tuning and fine analog tuning are achieved using pMOS-varactors.

The VCO were implemented in a 0.18-μm standard CMOS process. The VCO tuned from 1.8GHz to 2.55GHz through 2-bit digital and analog input. At 1.8V power supply voltage and a total power dissipation of 8mW, the VCO features a phase noise of -126dBc/Hz at 3MHz frequency offset.

Keywords — VCO, wide tuning range, pMOS varactor, digital tuning

Ⅰ. Introduction

The explosive growth of today's telecommunication market has brought an increasing demand for high-performance radio-frequency circuits in low-cost technologies. The implementation of monolithic VCO in standard CMOS technologies is one of the major challenges that must be overcome in the design of integrated radio-frequency CMOS transceivers. The phase noise of the VCO is one of the most critical parameters for the quality and reliability of the information transfer. To achieve the low-phase-noise specifications with low power consumption, integrated passive *LC*-VCO's tend to be the best choice. It is generally believed that the *LC* oscillator, even with a low-Q inductor, displays a lower phase noise than the ring oscillator. However, due to the absence of good varactors compatible with CMOS technology, the integrated *LC* oscillator suffers from very limited tuning range. This work aims at the design of VCO that has a wider tuning range than the previous works, without extra processing steps and increase of the power supply voltage.

This work presents the theoretical and experimental results of the use of three identical pMOS-varactors as digital and analog tuning components for RF VCO. It is shown that varactors allow wide tuning performance for multimode, multiband applications.

Ⅱ. CMOS *LC* VCO Design

A general integrated CMOS *LC* tuned voltage-controlled oscillator (VCO) consists of an inductor and a capacitor, building a parallel resonance tank, and active parts, compensating the losses of the inductor and capacitor. As the range of capacitance is proportional to a tuning input voltage, the circuit results in a VCO with center frequency

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \qquad (1)$$

It can be symbolized as in Fig.1.

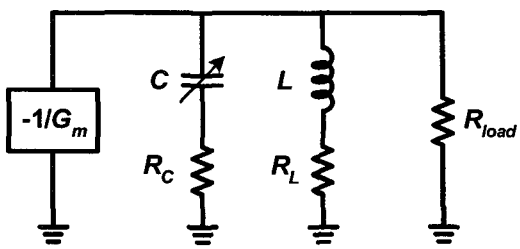

Figure 1. *LC*-VCO equivalent circuit

The differential CMOS VCO under investigation is shown in Fig.2. This is a standard symmetric CMOS VCO architecture, where *LC* tank consists of two rectangular spiral inductors and three pMOS varactors. A cross-coupled differential transistor pair provides a negative resistance which is essential to compensate the loss of *LC*-tank. A simple active-loaded common-source nMOS transistor was used as an output buffer to drive the 50-Ω measurement system. In [1], the authors just use MOS varactors to provide coarse digital tuning. In this paper, the pMOS varactor has been used not only for coarse digital tuning but also for fine analog tuning to achieve wide tuning ranges.

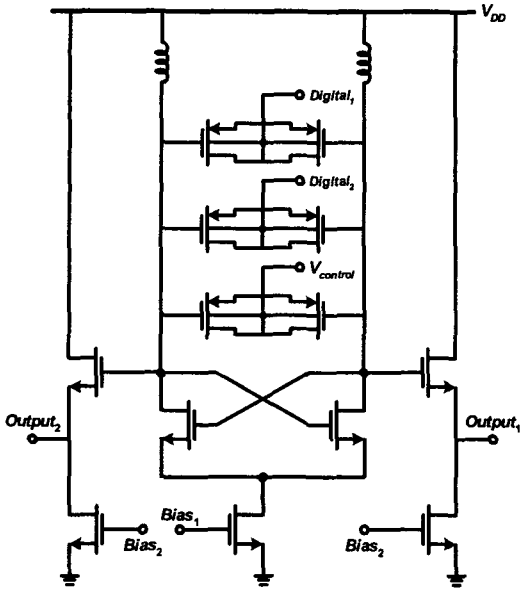

Figure 2. CMOS VCO under investigation

III. *LC* tank Design

A. MOS Varactor

It is well known that an MOS transistor with drain, source and bulk (D,S,B) connected together realizes an MOS capacitor with capacitance value dependent on the voltage V_{BG} between bulk and gate. In the case of a pMOS capacitor, an inversion channel with mobile holes builds up for $V_{BG} > |V_T|$, where $|V_T|$ is the threshold voltage of the transistor. The condition V_{BG} $|V_T|$ guarantees that the MOS capacitor works in the strong inversion region, the region where the MOS device shows a transistors behavior. On the other hand, for some voltage $V_G > V_B$, the MOS device enter the accumulation region, where the voltage at the interface between gate oxide and semiconductor is positive and high enough to allow electrons to move freely. Thus, in both strong inversion and accumulation region the value of the MOS capacitance C_{mos} is equal to $C_{ox} = \varepsilon_{ox}S/t_{ox}$, where S and t_{ox} are the transistor channel area and the oxide thickness, respectively [3].

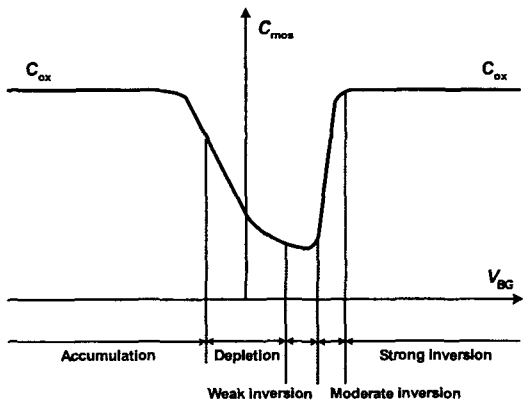

Figure 3. Tuning characteristics for the pMOS

Three more regions can be distinguished for intermediate values of V_{BG} ; moderate inversion, weak inversion, and depletion [4]. In these regions there are few mobile charge carries at the gate oxide interface, which causes a decrease of the capacitance C_{mos} of the MOS device. The behavior of C_{mos} versus V_{BG} is reproduced qualitatively in Fig.3.

In this work, a combination of two pMOS capacitors is used varactor for digital tuning. Thus, the capacitance of varactors increases from 4 pF to 8.5pF as the 2-bit digital and analog input voltage varies from 0.8V to 1.8V. The variation covers 750MHz of tuning range. Also, tuning range of the VCO increases as bits of digital input are increased. The simulation results of the varactor are shown in Fig.4. In Fig.5, the tuning frequencies are displayed.

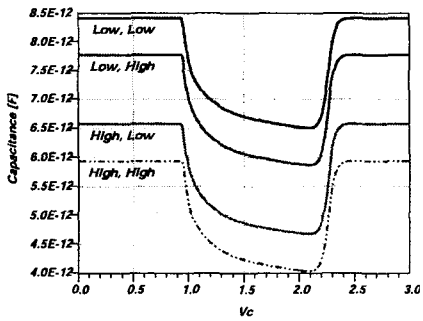

Figure 4. Capacitance of varactor vs. $V_{control}$

This allows the varactor to be used in low-voltage VCO. So wide tuning range VCO can be achieved without extra processing steps and increase of the power supply voltage.

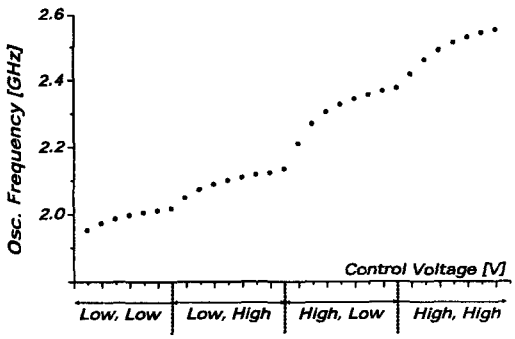

Figure 5. Osc.Frequency vs. $V_{control}$

B. Integrated Spiral Inductor

The key factor in the design of low-phase-noise *LC* oscillators is the design of a high-quality inductor. This is reflected in the equations for the phase noise and the power consumption.

$$P_{loss} = RC^2\omega_c^2V_{peak}^2 = \frac{R}{L^2\omega_c^2}V_{peak}^2 \qquad (2)$$

where V_{peak}^2 is the peak amplitude voltage across the capacitor, L is inductance of tank, R is the loss of spiral inductor, C is capacitance of tank.

Already in 1966, Leeson published the following heuristic expression for the phase noise of a LC-VCO:

$$S_{SSB} = F\frac{kT}{2P_{sig}}\frac{\omega_c^2}{Q^2\Delta\omega^2} = F\frac{kT}{2P_{sig}}\frac{R^2}{L^2\Delta\omega^2} \qquad (3)$$

where Q is the loaded quality factor of the tank, $\Delta\omega=2\pi\Delta f$ is the angular frequency offset, and F is called the device noise excess factor or simply noise factor. [6]

As shown in equation (2) and (3), the inductor's series resistance must be low so as to lower the phase noise as well as the power consumption.

The EM simulation has been used to find an optimal inductor solution for a low-phase noise, low-power specification. Based on the simulations, a two-turn rectangular inductor is implemented in a 0.18μm CMOS process. The simulation results of spiral inductor characteristics are shown in Fig.6.

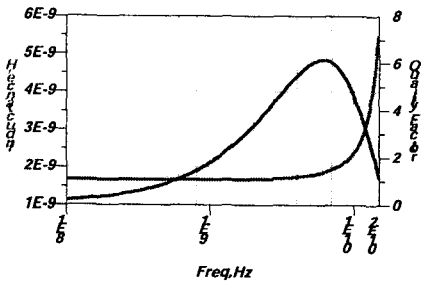

Figure 6. Designed inductor characteristics

IV. Simulation Results

A wide tuning range fully integrated CMOS VCO was designed and fabricated with 0.18μm CMOS process. In Table1 the simulation results is displayed

Table 1. Performance of VCO (based on simulation)

	Simulated Data
Osc. Frequency	*1.8 ~ 2.55 GHz*
Tuning Range	*750 MHz*
Phase Noise	*-126dBc/Hz @3MHz*
Power	*7.2 mW*

A tuning range of 750MHz was obtained through the use of three pMOS varactors. Simulated worst case phase noise is -126dBc/Hz @ 3MHz. This VCO fulfills Bluetooth phase noise requirements at a power consumption of only 7.2mW.

V. Fabrication and Measurement Results

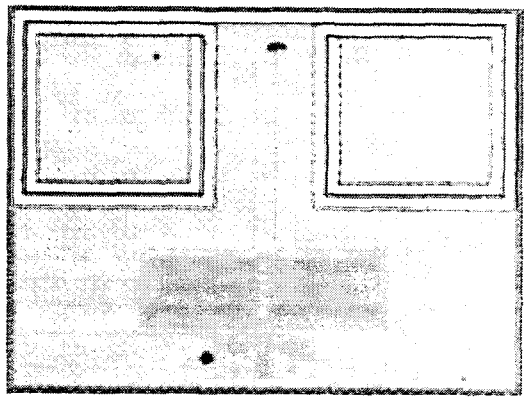

Figure 7. Chip Photo of fabricated VCO

The CMOS VCO using a combination of three pMOS capacitors for wide tuning range applications as shown Fig.2 were designed and fabricated with Anam 0.18μm CMOS. The chip photo in Fig.7 shows the perfectly symmetrical layout. Testchip size is 650μm by 500μm.

The fabricated die was mounted on a FR-4 PCB board with wire bonding for measurement and artwork is shown in Fig.8. And a bonding wire microphotograph is shown Fig. 9. The measurements have been carried out with HP Spectrum Analyzer.

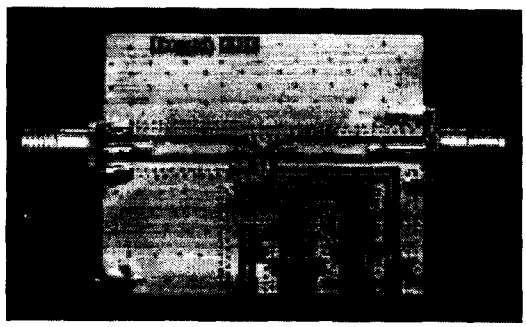

Figure 8. FR-4 PCB Test Board for measurement

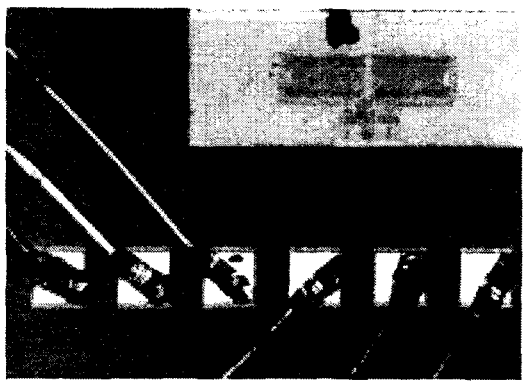

Figure 9. A bonding wire microphotograph

Table 2. Measured data summary

	Simulated Data	Measured Data
Osc. Frequency	1.8 ~ 2.55 GHz	1.08 ~ 1.15 GHz
Tuning Range	750 MHz	70 MHz
Phase Noise	-126dBc/Hz @3MHz	-119dBc/Hz @3MHz
Power	7.2 mW	7.2 mW

Table2 gives a summary of the measured performance. The deviation of measured data from simulated data is due to absence of pMOS varactor model and the conventional effect of PCB board. The measured oscillation frequency is even lower by the effect of the fixed overlap gate-source, gate-drain and substrate capacitances. And decrease of tuning ranges is due to parasitics of PCB board, such as parasitic capacitances by PCB interconnection, and losses of board, coupling effect of bias line. Especially bias line of connected varactor input effected a change of *LC* tank impedance.

A bonding wire connects a pad of the IC to a pad of the PCB board. A rule of thumb for the inductance associated with this connection is 1nH per mm length. This is a serious problem for high frequency input or output, since the combination of this inductance with the parasitic capacitance of bonding pad. It must be considered that suitable buffer circuits are inserted to drive the MOS varactors. The phase noise degradation is probably caused by increasing losses in the varactor, or by the increase in upconverted baseband noise due to the larger nonlinearities. Such are the problems that disturb a precise measurement.

VI. Conclusion.

In this paper, we presented a wide tuning range fully integrated *LC*-VCO that requires no extra processing steps. A 2-bit digital tuning scheme gives wider tuning bandwidth.

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