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비이상 불순물 분포 상태가 $CoSi_2$와 STI 공정에 의해서 제작된 CMOS 소자의 누설전류에 미치는 영향에 관한 연구

(Effect of abnormal dopant profiles on the junction leakage current in submicron CMOS devices with Co-silicidation and shallow trench isolation (STI) processes)

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A cobalt self-aligned-silicide (Co-salicide) process has become an essential technology for high performance ultra-large-scale integrated (ULSI) circuits. However, as the design rule continues to scale down, a junction leakage problemcaused by a Co-silicidation process can be a key issue for next generation integrated circuits. Efforts to find out leakage mechanisms in ULSI devices made with silicide processes have become a critical challenge for a decade. However, the precise leakage model remains still unclear due to the complex characteristics of the junction leakage.

In this work, two dimensional dopant profiling using transmission electron microscopy (TEM) combined with selective chemical etching is employed to investigate the leakage mechanism in p+/n shallow junctions that are fabricated using Co silicidation and STI processes. The TEM (Fig. 1) and TSUPREM-4 simulation (Fig. 2) results show that the junction profiles abnormally bend upward near the edge of the active region due to transient enhanced diffusion (TED), resulting in the formation of the shallower junctions. It is proposed that the shallower junctions are responsible for the leakage current in the shallow silicided p+/n junction.

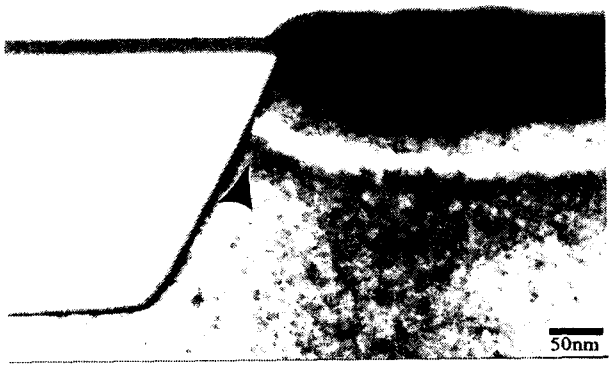

Fig. 1. A TEM image obtained from selective-chemical-etched silicided sample, showing two-dimensional dopant profiles. It is worth noting that the junction profile bends upward, as indicated by the arrow.

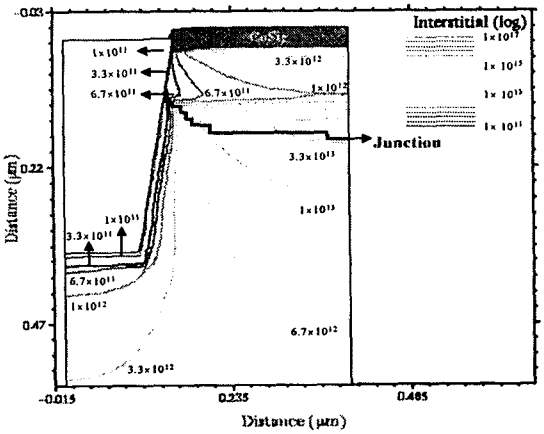

Fig. 2. Profiles of two-dimensional Si interstitials and junction simulated by TSUPREM-4 using transient enhanced diffusion model after the silicidation process.