A Single-Chip CMOS Digitally Synthesized 0-35 MHz Agile Function Generator

C. Meenakarn[1,2] and A. Thanachayanont[1]

[1] Research Center of Communications and Information Technology, and Faculty of Engineering,
King Mongkut's Institute of Technology Ladkrabang,
3 Chalongkrung Rd, Bangkok 10520, THAILAND
Phone: +66-2-7373000 ext 3309, Fax: +66-2-7392429, E-mail: s3061316@kmitl.ac.th, ktapinun@kmitl.ac.th
[2] Thailand IC Design Incubator (TIDI), National Electronics and Computer Technology Center (NECTEC)
99/25, 10th floor, Software Park Bldg, Chaengwattana Rd, Nonthaburi 11120, THAILAND
Phone: +66-2-5822560 ext 213, Fax: +66-2-5822562, E-mail: charan@nectec.or.th

Abstract: This paper describes the design and implementation of a single-chip digitally synthesized 0-35 MHz agile function generator. The chip comprises an integrated direct digital synthesizer (DDS) with a 10-bit on-chip digital-to-analog converter (DAC) using an n-well single-poly triple-metal 0.5-μm CMOS technology. The main features of the chip include maximum clock frequency of 100 MHz at 3.3-V supply voltage, 32-bit frequency tuning word resolution, 12-bit phase tuning word resolution, and an on-chip 10-bit DAC. The chip provides sinusoidal, ramp, saw-tooth, and random waveforms with phase and frequency modulation, and power-down function. At 100-MHz clock frequency, the chip covers a bandwidth from dc to 35 MHz in 0.0233-Hz frequency steps with 190-ns frequency switching speed. The complete chip occupies 12-mm^2 die area and dissipates 0.4 W at 100-MHz clock frequency.

1. Introduction

There are many significant advantages of direct digital synthesizer (DDS) over the traditional frequency-agile phase-locked loop (PLL)-based synthesizer, including fast settling time, digitally-controlled sub-hertz frequency and sub-degree phase resolutions, continuous-phase switching response, and low phase noise [1]. Due to advances in digital logic and digital-to-analog converter (DAC) IC technologies, DDS is now enjoying an increasingly significant role in wideband frequency generation. The integration of a high-speed, high-performance DAC and DDS circuitry onto a single chip enables low-cost, high-performance, functionally-integrated, and small package-sized DDS products, which target a wide range of applications such as time division multiple access/code division multiple access (TDMA/CDMA) digital cellular systems and spread-spectrum wireless LANs.

A number of high-speed DDSs with on-chip DAC have been reported. In [2], a CMOS DDS implemented in a 1.0-μm process was reported with 50-MHz maximum operating clock frequency. In [3], a BiCMOS DDS implemented in 0.8-μm double-metal double-poly process was reported with the maximum operating clock frequency of 170 MHz. The gap in the maximum operating clock frequency of the two designs mainly arises from the difficulty in the design of high-speed DAC in CMOS technology. Therefore the design of a high-speed DDS with an on-chip DAC in standard CMOS process still poses a real challenge. This paper describes the design and implementation of a single-chip digitally synthesized 0-35 MHz agile function generator using an n-well single-poly triple-metal (1P3M) 0.5-μm CMOS technology. The objective of the chip reported in this paper is to generate various types of waveforms for general video, wireless applications such as digital radios/modems, test and measurement equipment, digital video/audio, baseband transceivers, and PC-based instrumentation cards.

2. Chip Architecture

The architecture of the chip, shown in Figure 1, is employed. The phase accumulator word length is chosen to be 32 bits to achieve a frequency tuning resolution of 0.0233 Hz at the clock rate of 100 MHz. Only 14 of the most significant bits (MSBs) are used to calculate the sine wave samples in order to reduce size and power dissipation of the table look-up ROM. Two MSBs of these 14 bits are used to decode the quadrant of the sine wave samples in the ROM. This achieves a 12-bit phase tuning resolution that yields a spurious performance due to the phase accumulator truncation of –72 dBc [4], which is well below the spur level of the on-chip 10-bit DAC at 100 MHz.

Phase modulation of the chip is achieved by adding 12-bit phase tuning word to the phase accumulator output before entering the phase-to-amplitude converter. The 10-bit digital output data is also available for applications that do not require the conversion to analog, such as tuneable digital band-pass filter, mixers for digital receivers, and real-time digital spectrum analysis. The design of the chip, described in the following sections, is divided into two main parts: (1) the DDS circuitry (digital part) and (2) the analog part. The layout considerations and the experimental results are described after the design of digital and analog parts.

3. Design of DDS Circuitry

3.1 DDS Circuitry Architecture

The DDS circuitry is designed and implemented by using hardware description language (HDL). In this design, VHDL language is chosen. The VHDL code is first simulated at the functional level. Then the functionally verified VHDL code is synthesized into the gate-level

circuitry. The gate-level circuitry is re-simulated in order to verify the timing constraints. The main building blocks of the DDS circuitry are a 32-bit phase accumulator, coarse and fine ROMs, a 14-bit phase-to-amplitude converter and a clock generator. In order to achieve maximum conversion speed, the 19-stage pipeline is employed. The modified Sunderland algorithm [5] is chosen for phase-to-amplitude conversion. Latches are implemented to strobe the digital samples of the waveform before entering the 10-bit DAC in order to eliminate signal skews and reduce output glitches.

The frequency and pattern of the output waveform can be controlled by an external micro-controller via an 8-bit parallel interface. The maximum update rate, determined by the speed of the control interface and the 19-stage pipeline, is 38 MS/s. The DDS circuitry can provide 4 waveforms including sinusoidal, ramp, saw-tooth and random. The 10-bit amplitude of ramp and saw-tooth waveforms is generated directly from the phase register, while a linear feedback shift register is used to generate random values for random waveform. The 10-bit amplitude of sinusoidal waveform is generated from a sine look-up table.

3.2 Memory Compression

Using the well-known quarter-wave symmetry technique, the sine wave samples for the full range of 2π are generated from 0 to $\pi/2$ rads of sine information stored in the ROM [5]. The two MSBs of the phase accumulator are used to decode the quadrant of the sine function. Thus the MSB is used as the sign bit, while the next MSB controls whether the phase between 0 to $\pi/2$ should be increased or decreased. This reduces the capacity of the look-up table with the penalty of additional logic circuits required to generate the complements of the accumulator and the look-up table outputs. The width of the one-quadrant look-up table is reduced by compression of the quarter-wave sine information using the Modified Sunderland algorithm [5]. The use of Modified Sunderland algorithm gives the total ROMS compression ratio of 64:1.

4. Design of 10-Bit DAC

4.1 DAC Architecture

The integrated high-speed 10-bit DAC is implemented by using the 6/4 segmented current-steering architecture, in which the 6 MSBs of the digital binary inputs are thermometer-decoded to control 63 identical current sources, each having 16-LSB current weighting, and the remaining 4 LSBs control 4 binary-weighted current sources. The output currents of all current sources, which are either switched ON or OFF according to the digital input codes, are summed and driven into any resistive load in order to generate the required analog output voltage. The DAC comprises an array of current-steering cells, a bias generator, a segment decoder, and code latches as shown in Figure 2.

4.2 Current-Steering Cell

The schematic diagram of the current-steering cell of the 10-bit DAC is shown in Figure 3. The cascode current source (M_{p1} and M_{p2}) and the differential current-steering switches (M_{p3} and M_{p4}) are implemented by using p-channel MOSFETs in order to obtain the output voltage referred to ground. The cascode configuration suppresses the voltage fluctuation at the drain of the transistor M_{p1} thereby enhancing the output impedance of the current source. Long channel length is required for the transistor M_{p1} in order to achieve good accuracy and matching of the output current. The cascode transistor M_{p2} should have a short channel length in order to minimize the parasitic capacitance at the coupled sources of the differential switches, thus improving the switching speed during the output transition. The current from the cascode circuit is steered by the differential switches into two resistive loads, according to the true and complementary digital control signals, D1 and D1B. The differential switches employ the minimum channel length, and the width is optimized toward the switching speed while maintaining the accuracy of the output currents.

The two complementary digital control signals, D1 and D1B, are generated by the asymmetrical switch driver [6], M_{n1}-M_{n4}, in order to withdraw any possibility that both switches are turned OFF simultaneously due to inevitable delay in both control signals. The switch driver is simply a differential drive circuit with n-channel transistors for both pull-up and pull-down. The dimension of M_{n1}-M_{n4} must be chosen properly such that the fall-time of D1 and D1B (turning ON) will be faster than the rise-time (turning OFF). This ensures that both switches are never turned off simultaneously, but allowing a simultaneous turn-on for a short period of time. Turning-on both switches simultaneously will degrade the switching speed a little, but reducing glitches substantially. Furthermore, the HIGH level output is V_{TH} lower than V_{DD}, minimizing the switching swing thus reducing the switching feedthrough to the output current. This intentional asymmetrical switching circuit guarantees that one switch is ON, even for a small skew. HSPICE simulation using the process parameters from the Alcatel's 0.5-μm CMOS technology suggests an extra delay of 0.2 ns due to the switch driver circuit.

The two complementary DAC output currents are uni-polar. Thus the voltages developed across the load resistors range from 0 V to a positive full-scale value. In practice, a center-tapped RF transformer is used to combine these two complementary currents and produce a bi-polar, zero DC-offset symmetrical output current. Additionally the transformer is beneficial in both providing the DAC outputs a suitable load resistance (via an impedance transformation) in order not to violate the DAC output voltage compliance, and coupling the DAC output currents to the reactive input of the subsequent LC low-pass filter. This also maintains a constant current flowing in each current source during switching, thus allowing fast settling time and reducing output glitches.

Linearity of the DAC is determined by the matching of current sources. In practice, the total current error is due to

the variation in threshold voltage and process geometry [7]. The dominant source of error is likely to be the threshold voltage variation provided that the devices are well above the minimum geometry. Thus large gate-source voltage and large LSB current weighting are required to reduce the mismatch. Measured mismatch data from the 0.5-μm CMOS technology suggest that the channel length of the p-channel MOSFET current source should be no shorter than 4 μm in order to satisfy the current matching requirements of the 10-bit DAC. Other circuit parameters are then calculated accordingly to meet the DAC specifications.

5. Layout Considerations

The performance of the complete chip is largely determined by the on-chip DAC. Thus much attention were paid to the layout and routing of the DAC including the bias generator which were done by hand, while all digital circuits were implemented by using automatic place-and-route with standard library cells. The total chip area about is 12 mm^2.

To obtain the optimum performance, the DAC cascode current sources are drawn in an array, isolating from their associated current-steering switches and asymmetrical switch drivers that are placed together in a separate block. This allows a compact and uniform layout of the array, reducing mismatches between the current sources. Isolation of sensitive analog circuits from digital switching noise is very important in mixed signal IC. Therefore analog and digital power supplies are separated, and double guard rings surround both the current source array and the switches and drivers block in order to prevent digital switching noise coupling to the DAC output currents.

6. Experimental Results

A test system, shown in Figure 4, was developed in order to evaluate the chip. The software on a personal computer is used to load the frequency control word into the test board. The micro-controller on the test board generates controlling data and signal for the chip according to the frequency control word received from the computer. A 7^{th}-order 40-MHz low-pass filter is used to filter high-frequency components from the output of the chip.

The chip was tested at 3.3-V supply voltage and 100-MHz clock frequency. The chip can generate an output from dc to 35 MHz in 0.0233-Hz frequency steps with 190-ns frequency switching speed. The spurious free dynamic range (SFDR) is better than 45 dBc. A spectrum shown in Figure 5 is the spectrum of 2-MHz sinusoidal output. Figure 6 shows the relation between SFDR and output frequencies at 100-MHz clock frequency. The phase noise is below −115 dBc/Hz at 100-kHz offset. The closed-in spectrum of the 25-MHz sinusoidal output at 100-MHz clock frequency is shown in Figure 7.

7. Conclusions

The design and implementation of a single-chip CMOS digitally synthesized agile function generator is described in this paper. The chip covers a bandwidth from dc to 35 MHz with 0.0233-Hz resolution. At 100-MHz clock frequency, the SFDR is better than 45 dBc. Table 1 summarizes the specifications of the chip. The photomicrograph of the chip is shown in Figure 8.

Acknowledgements: Financial support of the Tri-Partite research grant from National Electronics and Computer Technology Center (NECTEC), Thailand, is gratefully acknowledged.

References

[1] B. Goldberg, Digital techniques in frequency synthesis, McGraw Hill, 1996, New York.

[2] G. Chang, A. Rofougaran, M. Ku, A. A. Abidi, and H. Samueli, "A low-power CMOS digitally synthesised 0-13 MHz agile sinewave generator," in *Proc. Int. Solid-State Circuits Conf.*, 1994, pp. 32-33.

[3] J. Vankka, M. Waltari, M. Kosunen, and K. Halonen, "A direct digital synthesizer with an on-chip D/A-converter," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 218-227, Feb. 1998.

[4] H. T. Nicholas, III, H. Samueli, and B. Kim, "The optimization of direct digital synthesizer performance in the presence of finite word length effects," *in Proc. 42nd Annu. Frequency Control Symp.*, 1988, pp. 357-363.

[5] J. Vankka, "Methods of mapping from phase to sine amplitude in direct digital synthesis," in *Proc. 1996 IEEE Int. Frequency Control Symp.*, pp. 942-950.

[6] T.-Y. Wu, C.-T. Jih, J.-C. Chen, and C.-Y. Wu, "A low glitch 10-bit 75-MHz CMOS video D/A converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 68-72, Jan. 1995.

[7] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1440, Oct. 1989.

Table 1. Chip specifications

Technology		Single-poly, triple-metal 0.5-μm CMOS
Power supply voltage		3.3 V
Max. clock frequency		100 MHz
Max. output frequency		35 MHz at 100-MHz clock rate
Frequency resolution		32 bits (0.0233 Hz at 100 MHz)
Phase tuning resolution		12 bits (0.0879 degrees)
Amplitude resolution		10 bits (0.846 mV at R_L = 25 Ω)
f_{out} = 25MHz	Worst-case spurious	-45 dBc
	Phase noise	*-115 dBc/Hz at 100-kHz offset*
Max. frequency switching speed		190 ns (19 x 1/100MHz)
Die area (including pads)		3240x3830 μm^2
Power dissipation	Digital	270 mW at 100-MHz clock rate
	Analog	126 mW at full-scale output level

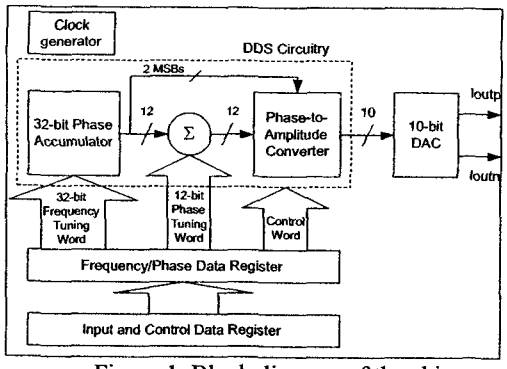

Figure 1. Block diagram of the chip

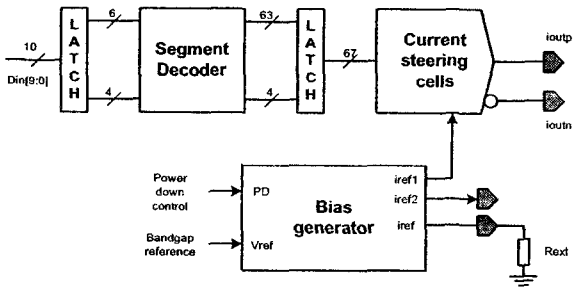

Figure 2. Block diagram of the 10-bit DAC

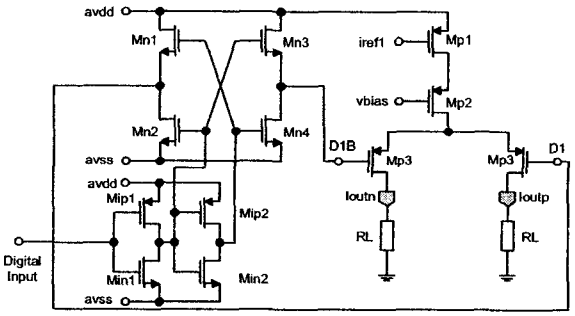

Figure 3. DAC's current-steering cell

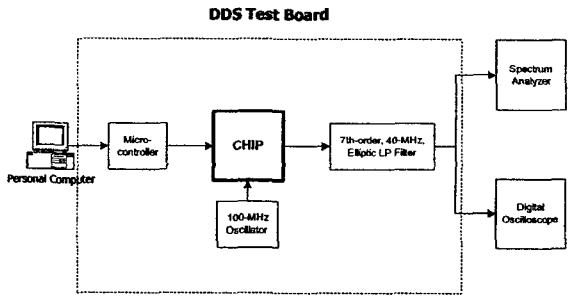

Figure 4. Test system

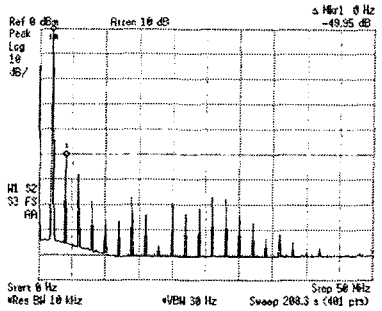

Figure 5. Spectrum of 2-MHz sinusoidal output @ 100-MHz clock frequency

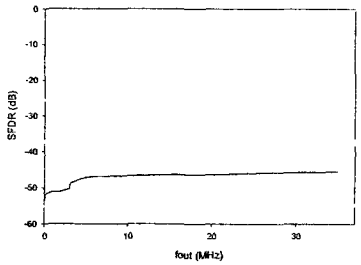

Figure 6. SFDR as a function of output frequency @ 100-MHz clock frequency

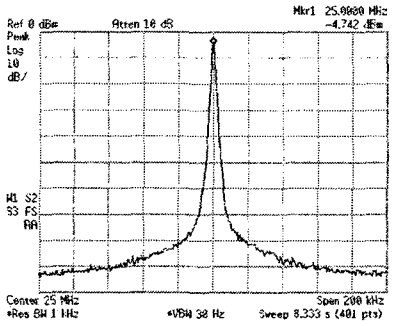

Figure 7. The close-in spectrum of 25-MHz sinusoidal output @ 100-MHz clock frequency

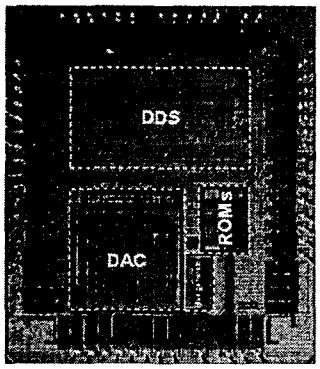

Figure 8. The photomicrograph of the chip