

# Chip Timing Recovery Algorithm Robust to Frequency Offset and Time Variant Fading

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**Abstract:** In this paper, we propose a chip timing recovery algorithm that is robust to frequency offset and time variant fading environments for DS/CDMA. The proposed structure is a modified non-coherent Delay Locked Loop (DLL) that employs a decimator. Analytical expression for the proposed non-coherent DLL S-curve and steady-state timing jitter is derived and confirmed by computer simulation. The results show that the proposed structure can reduce a steady-state timing jitter of the regenerated spreading code replica to frequency offset and time-variant fading in mobile radio channel, especially in very low SNR.

are described in section 3. In section 4, the performance of the proposed structure is compared to the conventional non-coherent DLL. Finally, we draw a conclusion in section V.

## 1. Introduction

In WCDMA system, which has higher chip rate than IS-95, rapid and fine chip timing error tracking is essential for synchronization technique. There are two chip timing error tracking algorithms in DS/CDMA: Delay Locked Loop (DLL) and Tau Dither Loop (TDL). It is well known that DLL gives a 3dB increase in the signal to noise ratio (SNR) of the chip timing error signal compared to TDL. DLL is classified into non-coherent DLL and coherent DLL. The non-coherent DLL is the most popular and well-developed technique, but it suffers from increased tracking jitter due to noise enhancement arising from square-law detector, which is called squaring loss [1]. It turned out analytically that coherent DLL overcomes this problem of non-coherent DLL and has a slightly better performance than non-coherent DLL in AWGN. But, its performance is degraded by data decision error, mobile channel estimation uncertainty and frequency uncertainty [2].

In this paper, we propose a modified non-coherent DLL, which has some little tracking jitter in very low SNR and is robust to frequency offset and time variant mobile radio channel. Sum of early gate output and late gate output is used to prevent performance degradation by amplitude variation due to time variant fading, which is traditionally a problem of Early-Late synchronization architecture. We prove by analysis and extensive computer simulation that the tracking jitter and stability of the proposed tracking structure are superior to the conventional structure, especially in very low SNR and fading.

This paper consists of as follows. The proposed chip timing error tracking structure is introduced briefly in section 2. Analysis with respect to S-curve and timing jitter

## 2. Proposed Chip Timing Error Detector

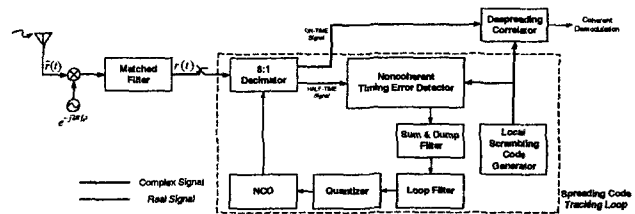


Figure 1. DLL structure for DS/CDMA receiver

The DLL structure for DS/CDMA receiver is shown in Figure 1. The received bandpass signal is first down-converted to baseband by the receiver local oscillator, filtered by a matched filter and sampled by a free-running Analog-to-Digital converter (ADC) operating at some multiple of the chip rate,  $1/T_c$  Hz. The output of the ADC is then down-sampled to the chip rate by a decimator and fed into the Timing Error Detector (TED). The error signal generated by the TED is filtered by the loop filter, and is quantized and used to control the sampling phase of the decimator by Numerical Controlled Oscillator (NCO) [3].

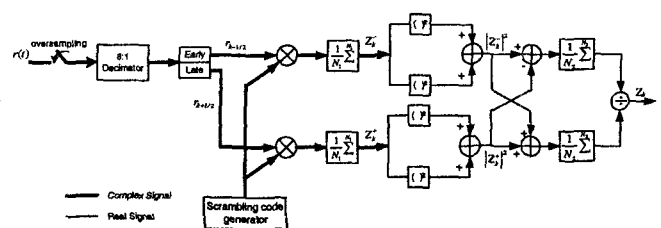


Figure 2. Proposed Non-coherent TED

Figure 2 shows the proposed TED structure in this paper. To reduce the effect of random magnitude and phase, the error signal that is a difference between early gate output and late gate output is normalized by the summation value of early gate output and late gate output. In this procedure, the attenuation factor due to frequency offset and fading is removed.

### 3. S-Curve and Steady-State Timing Jitter Analysis

It is assumed that the chip pulse shaping filter is matched to the transmitter's. The baseband equivalent signal model adopted in this paper follows the air interface specification of the WCDMA reverse link [4]. The filtered complex baseband signal  $r(t)$  with a propagation delay  $\tau$  can then be written as follows:

$$r(t) = \sum_{i=-\infty}^{\infty} \left[ \frac{\sqrt{E_c}}{2} \alpha(t) (d_{(i)_N}^I C_{|i|_M}^d + j d_{(i)_{256}}^Q C_{|i|_{256}}^Q) (S_{|i|_M}^I + j S_{|i|_M}^Q) \right] \cdot \exp(2\pi\Delta f t + \theta_d(t)) g(t - iT_c - \tau) + n_R(t) \quad (1)$$

where  $E_c$  is the received chip energy,  $d_{(i)_N}^I + j d_{(i)_{256}}^Q$  is the  $i$ -th quadrature data symbol,  $g(t) \triangleq g_T(t) * g_R(t)$  is the impulse response of the overall chip pulse shaping filter satisfying the Nyquist criterion,  $g_T(t)$  and  $g_R(t)$  are Square Root Raised Cosine (SRRC) filter of transmitter and receiver respectively.  $\Delta f$  is the frequency offset generated by residual frequency offset and oscillator mismatch,  $\theta_d(t)$  is the residual carrier phase offset generated by Doppler effect.  $\alpha(t)$  is the random amplitude of a chip. Since the chip rate of WCDMA system is so high, most of the fading is slow time-varying. Therefore,  $\alpha(t)$  has almost the same value during the symbol interval.  $N \triangleq T/T_c$  is spread factor (SF) of DPCCCH,  $T$  is the symbol duration,  $T_c$  is the chip duration.  $C_{|i|_M}^d$  and  $C_{|i|_{256}}^Q$  are the channelization code of DPDCH and DPCCCH respectively.  $S_{|i|_M}^I + j S_{|i|_M}^Q$  is complex scrambling code,  $M$  is the scrambling code length,  $(i)_N$  is the integer quotient of  $i/N$ , and  $|i|_M$  is  $i$  modulus  $M$ .  $n_R(t) \triangleq n(t) * g_R(t)$  is the filtered noise process where  $n(t)$  is a complex AWGN with a double-sided power spectral density of  $N_o/2$ . Assuming that noise effect is ignored, the  $k$ -th sampled version of the early/late signal at time  $t_k = (k + \tau \pm 1/2)T_c$  is

$$r_{k \pm 1/2} = \sum_{i=-\infty}^{\infty} \left[ \frac{\sqrt{E_c}}{2} \alpha(k) (d_{(i)_N}^I C_{|i|_M}^d + j d_{(i)_{256}}^Q C_{|i|_{256}}^Q) (S_{|i|_M}^I + j S_{|i|_M}^Q) \right] \cdot \exp(2\pi\Delta f k T_c + \theta_d(k)) g[(k + \tau \pm 1/2 - i)T_c] \quad (2)$$

After descrambling, the sampled chip signal is transformed into a symbol by the sum and dump filter. In this procedure, DPDCH signal component is removed by the OVSF code orthogonal property [4]. The square-law-detector output of the early/late gate for given code timing error  $\tau$  has the following characteristics [5]:

$$E\{|Z_k^\pm|^2\} = E_c \left[ \frac{\sin(\pi N_1 \Delta f T_c)}{\pi N_1 \Delta f T_c} \right]^2 g^2[(\tau \pm 1/2)T_c] \quad (3)$$

S-curve derivation assumes that the instantaneous fading is averaged out over the observation time so that the average output of the conventional TED can be written as follows:

$$E\{Z_{k, \text{conventional}}\} = E_c \left[ \frac{\sin(\pi N_1 \Delta f T_c)}{\pi N_1 \Delta f T_c} \right]^2 \cdot \{g^2[(\tau - 1/2)T_c] - g^2[(\tau + 1/2)T_c]\} \quad (4)$$

In (4), we can see that the signal component by frequency offset attenuates the TED output [5]. In addition, we suppose that the TED output is attenuated by instantaneous fading. S-curve of the proposed TED can be derived as follows.

$$E\{Z_{k, \text{proposed}}\} \triangleq \frac{|Z_k^-|^2 - |Z_k^+|^2}{|Z_k^-|^2 + |Z_k^+|^2} = \frac{g^2[(\tau - 1/2)T_c] - g^2[(\tau + 1/2)T_c]}{g^2[(\tau - 1/2)T_c] + g^2[(\tau + 1/2)T_c]} \quad (5)$$

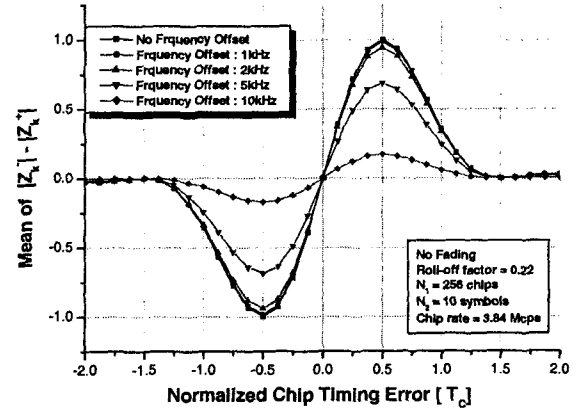


Figure 3. Normalized S-curve of the Conventional Non-coherent TED for given frequency offset

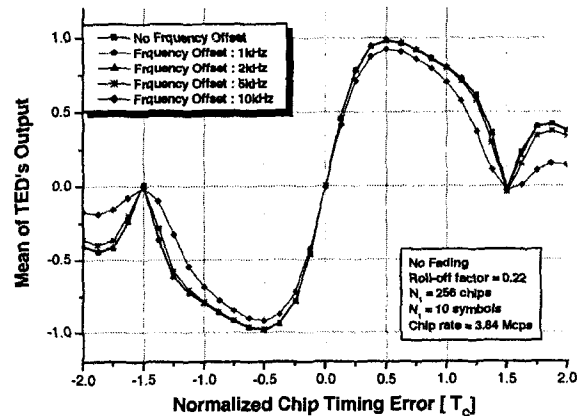


Figure 4. Normalized S-curve of the Proposed Non-coherent TED for given frequency offset

Plots of the normalized ( $E_c = 1$ ) S-curves are shown in Figure 3 and Figure 4 for a raised-cosine chip pulse with a roll-off factor of 0.22. Figure 3 is S-curve of the conventional non-coherent TED and Figure 4 is S-curve of the proposed non-coherent TED for given code timing error.

The square-law-detector outputs  $|Z_k^\pm|^2$  of early/late gate can be divided into I-component and Q-component. It is clear that I-component follows the central chi-square distribution and Q-component follows the non-central chi-square distribution. Thus  $|Z_k^\pm|^2$  has joint probability density function (pdf) of two components. Therefore, the mathematical analysis with respect to the pdfs of  $|Z_k^-|^2 - |Z_k^+|^2$  and  $|Z_k^-|^2 + |Z_k^+|^2$  is too difficult. So we provide the pdfs of two TEDs by computer simulation.

#### 4. Simulation Results

In this section, we compare the pdfs of the TED output, steady-state RMS jitter performances, and code tracking performance for the conventional and the proposed DLL by computer simulation. We adopt the first-order non-coherent DLL. Carrier frequency is 2 GHz.  $N_1$  is 256 and  $N_2$  is 150. Thus the decimator update rate  $N_s (\triangleq N_1 \times N_2)$  is 1 frame. For the first-order DLL, the TED output is scaled by the gain factor  $G$  of the loop filter and then quantized. The threshold  $\theta$  of the quantizer is adopted as  $|\text{TED}(T_c/16) \times K_D \times G|$ , where  $K_D$  is the TED gain. For the first-order DLL, the relationship between the equivalent loop noise bandwidth  $B_L$  and the loop gain  $G$  is given by [7] and is as follows:

$$2B_L T = \frac{G}{2-G} \quad T = \frac{38400 \text{ chip}}{3.84 \text{ Mcps}} \times N_s \quad (6)$$

In computer simulation, the same  $B_L$  is applied to the conventional and the proposed non-coherent DLL, where  $B_L$  is 0.0045 Hz. Figure 5 and Figure 6 show the pdfs of the conventional and the proposed TED output respectively. In very low SNR environment especially, the variance of the proposed TED output is less than that of the conventional TED output and the value of the proposed TED output is almost uniformly distributed in  $[-1, 1]$ . This phenomenon reveals that the steady-state RMS jitter of the proposed TED output is less than that of the conventional TED output. The comparison results of the conventional and the proposed TED output's RMS jitter for given frequency offset and Doppler spread are shown in Figure 7 and Figure 8. From these figures, we can see that the proposed structure is quite robust to frequency offset and Doppler spread. Figure 9 and Figure 10 show that the tracking performance of the conventional and the proposed DLL. Doppler frequency is 222.22 Hz and initial chip timing error is  $T_c/2$  in this simulation. From these results,

we can find out that the proposed structure is more stable than the conventional structure.

#### 5. Conclusions

In this paper, an alternative structure of the non-coherent DLL for bandlimited DS/CDMA signals is proposed. The steady-state RMS jitter and tracking performance achievable by the proposed non-coherent DLL are evaluated by computer simulation for the WCDMA reverse link. Simulation results showed that the proposed non-coherent scheme outperforms the conventional scheme thanks to its insensitivity to frequency offset and time-variant phase in mobile radio channel, especially in very low SNR.

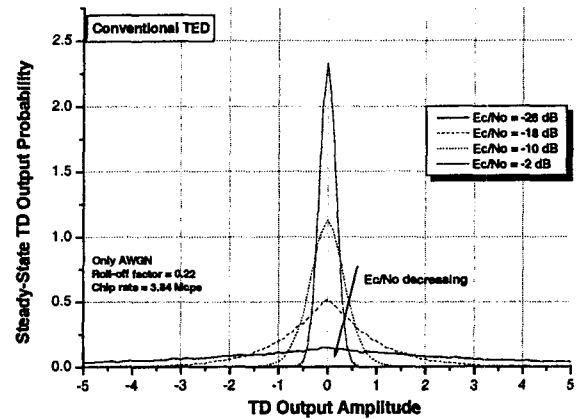


Figure 5. Probability Density Function of the Conventional TED output

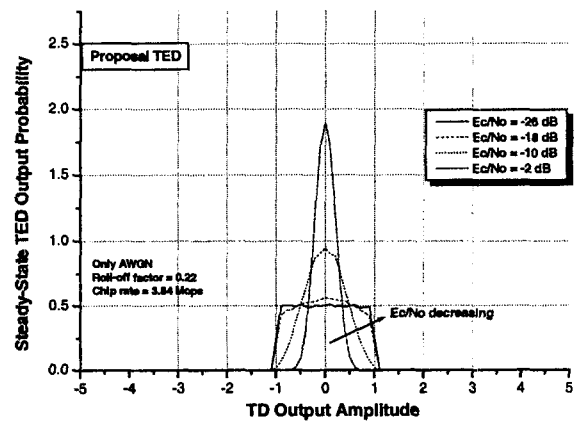


Figure 6. Probability Density Function of the Proposed TED output

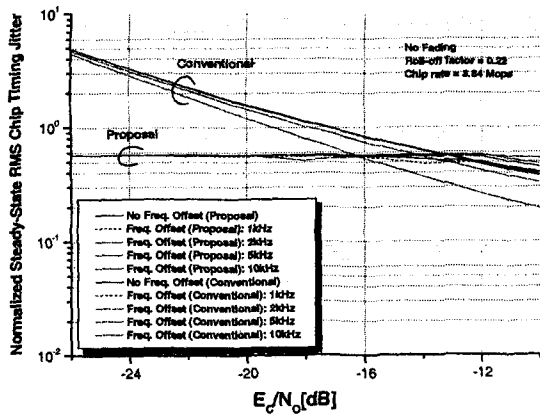


Figure 7. Steady-State RMS Jitter of the TED output for given Frequency Offset

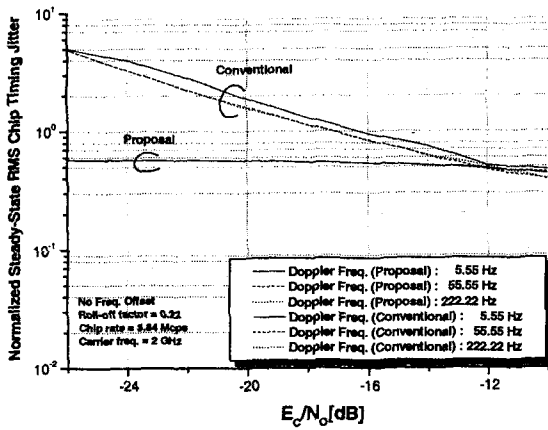


Figure 8. Steady-State RMS Jitter of the TED output for given Doppler Frequency

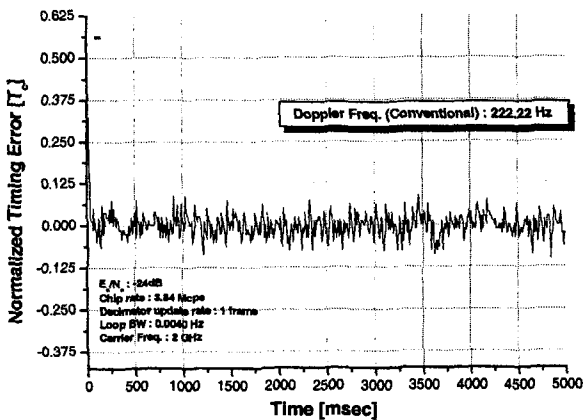


Figure 9. Tracking Performance of the Conventional DLL

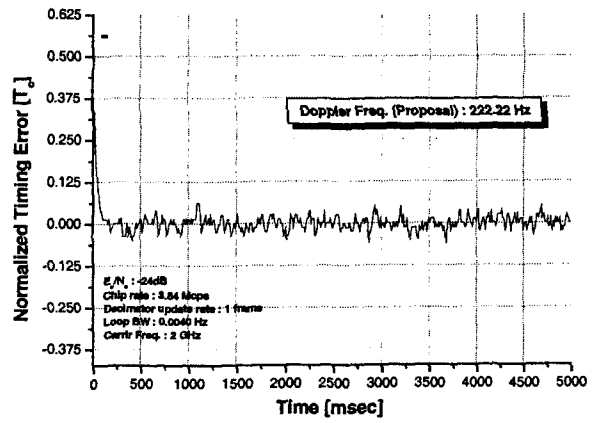


Figure 10. Tracking Performance of the Proposed DLL

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