Implementation of outgoing packet processor for ATM based MPLS LER System

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Abstract: The Internet with conventional routing scheme cannot meet user demands driven from drastic growth in the Internet user and various service and traffic type. MPLS(Multi Protocol Label Switching) was introduced to the Internet for solution to resolve this problem. MPLS is a paradigm to integrate higher layer's software routing functions including layer-3 routing with layer-2 switching. But, the exponential growth of Internet traffic brings out of label space. One scalable solution to cope with this problem is to introduce flow merge technique, i.e. a group of flows is forwarded using the same label. Specially, IETF(Internet Engineering Task Force) recommends that ATM based MPLS system may include VC merge function, so it is scalable to increase of internet traffic. We implemented the MPLS LER system that includes the look-up and forwarding function in incoming path and VC merging function and limited traffic management function in outgoing path. This paper describes the implementation of the LER's outgoing parts.

1. Introduction

In these days, there is increasing dramatically in user traffic of the Internet due to user demands for various service types and enormous growth of Internet user. Thus it makes impossible to meet user demands with conventional router based Internet. MPLS(Multi Protocol Label Switching) is a solution to resolve this problem. MPLS is a paradigm to integrate higher layer's software routing functions including layer-3 routing with layer-2 switching.[1][2][3]

But, the exponential growth of Internet traffic brings out of label space of MPLS. One scalable solution to cope with this problem is to introduce flow merging technique, i.e. a group of flows is forwarded using the same label.[4] Therefore, IETF(Internet Engineering Task Force) recommends that ATM based MPLS system may include VC merge function, so it is scalable to increase of internet traffic.[4][5][6]

MPLS is emerged to provide required Internet QoS(Quality of Service) to Internet users. But, normal user traffic is influenced by any spiteful user traffic with burstness, if MPLS router does not have appropriate traffic management solution. Therefore, it is required to implement traffic management function into MPLS LER(Label Edge Router). Especially, ATM based MPLS system is required to involve conventional ATM traffic management functions.

This paper is about a outgoing packet processor applicable to LER of ATM switch based MPLS system. We implemented the MPLS LER system that includes the look-up and forwarding function in incoming path and VC merging function. Additionally, a limited traffic management was appended to support ATM like QoS service.

This paper describes the implementation of the LER's outgoing parts.

2. ATM switch based MPLS System

We have developed ATM based MPLS system based on ACE2000 ATM switching system. The system is called ACE2000 MPLS system. The ACE2000 MPLS system has a modular architecture that can be easily extended by additional MIM(MPLS Interface Module). The MIM provides high performance packet forwarding capability and traffic management functions in incoming side and VC merge and traffic management functions in outgoing side. We can see the conceptual deployment of the MPLS network in Fig. 1.

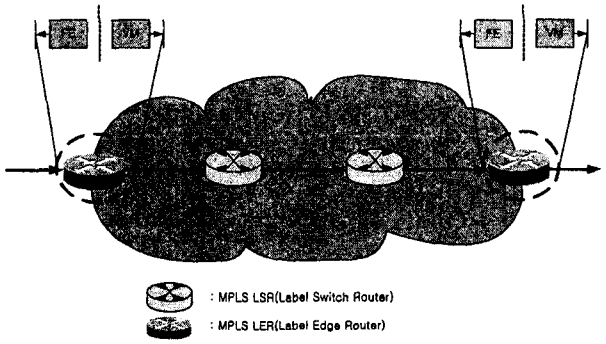

Fig. 1. MPLS network configuration with with ACE200 MPLS LER

As shown in Fig. 1, when an IP packet goes into MPLS domain, the IP packet arrives at FE(Forwarding Engine) part of the ingress LER. In the FE of ingress LER, the IP packet is classified based on service type and forwarded with VPI/VCI(Virtual Path Identifier/Virtual Circuit Identifier) used for MPLS label through look-up procedure. The forwarded packet is transferred to VM(VC Merge) part of corresponding HFMA(High performance packet Forwarding and VC Merge board Assembly) of ingress LER through ATM switch. The transferred packet

is processed by VM(VC Merge) of ingress LER and sent to next node operating for MPLS LSR(Label Switch Router). The IP packet traverses MPLS domain and arrives at egress LER through label swapping at each LSR node. The packet arrived at egress LER pass on processing in FE and VM of egress LER in turns and leaves from the MPLS domain.

MPLS LERs(ingress and egress) consist of MIMs(MPLS Interface Module) and ATM switch system. And, the MIM consists of four HFMA hardware boards with 622Mbps packet processing capability each. The HFMA is controlled by MSC(MPLS Service Controller) through the FE & VM manager(PowerPC MPC860). Fig. 2 shows the architecture of the HFMA.

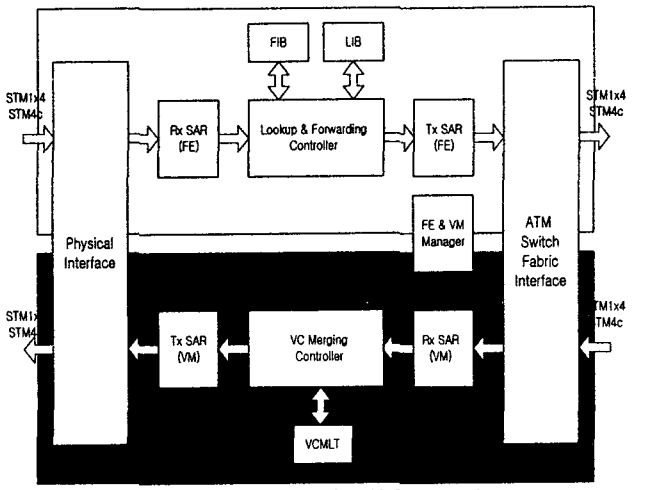

Fig. 2 Architecture of HFMA Hardware

HFMA supports four STM-1 or one STM-4C line interface. HFMA is subdivided with FE module and VM module. 'FE & VM manager' controls the FE and VC modules.

In the FE module, incoming ATM cells are reassembled to AAL-5 packet in Rx SAR(Receive Segmentation and Reassembly) block. The reassembled are classified and forwarded through 'Lookup & Forwarding Controller' based on FIB(Forwarding Information Base) and LIB(Lookup Information Base). And, segmentation to ATM cells by Tx SAR(Transmit Segmentation and Reassembly) block is followed. The segmented ATM cells goes into ATM switch fabric through STM-1 or STM-4C interface.

In the VM module, incoming ATM cell from ATM switch fabric are reassembled to AAL-5 packet in Rx SAR block. The reassembled AAL-5 packet is processed for VC merge through 'VC Merging Controller' based on VCMLT(VC Merge Lookup Table). And, the processed packet goes out through STM-1 or STM-4C after segmentation in Tx SAT block.

This paper deals with principally VC merge module shaded area in figure, which is referred to LER's outgoing packet processor in ACE2000 MPLS system.

3. Implementation of VC Merge Hardware

The outgoing packet processor of LER is capable of providing VC merge, VP merge and non-VC merge function at the same time. To do these functions, outgoing packet processor consists of Rx SAR, Tx SAR, VC merge Controller and VCMLT as shown in above Fig. 2.

3.1 Considerations in Packet types

There are three type of packets in ATM based MPLS system, i.e. AAL-5 type normal data packet, AAL-5 type EFC(Extended Forwarding Control) packet, and raw ATM cell. AAL-5 type normal data packet is transferred from one node attached to one of ingress MPLS LERs to another node attached to one of egress MPLS LERs. That packet is used for normal data transfer. AAL-5 type EFC packet is used to exchange any routing control information between a node attachd to any LER and MSC(MPLS service Controller). The AAL-5 type EFC packet is dedicated to our ATM based MPLS system.

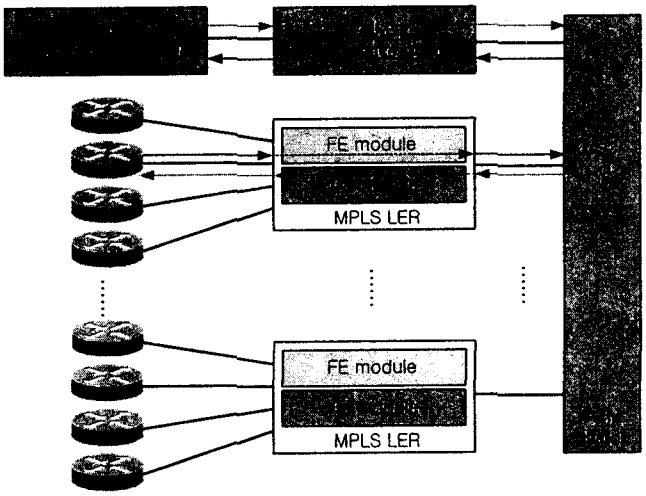

Fig. 3. Example of MPLS LER

Fig. 3 shows configuration of ATM based MPLS system and configuration of nodes attached ATM based LERs. As shown in Fig. 3, MSC exchange control informations including routing information and other control signalling information. So MSC has to communicate with nodes attached to LERs with point to multi-point communication. To do this communication of MSC to attached nodes, so many label reaources is required because ATM based MPLS system is connection oriented service. To cope with this label dissipation problem, we introduced the EFC packet dedicated to communication MSC to subscriber node. As EFC packet format shown in Fig. 4, the EFC packet use special header within AAL-5 PDU, which consist of three fields of 'Type(1B)', 'Cause(1B)' and 'Channel ID(2B)'. Channel ID field identifies outgoing channel to forward the corresponding packet.

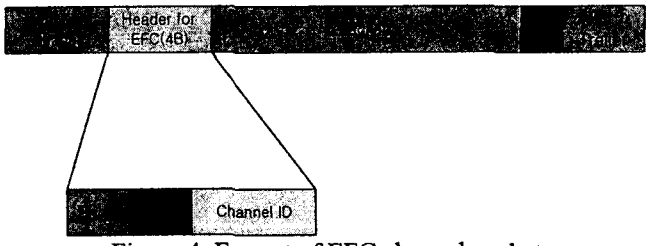

Figure 4. Format of EFC channel packet

ATM based MPLS system is able to operate in 'ships in the night' mode. To do in this mode, LER is capable to process raw ATM cell.

3.2 Implementation of VC merge Module

Label merge is that a group of flows is forwarded using the same label. In ATM based module, label merge refer to VC merge, in which several 'VPI/VCI's are consolidated single 'VPI/VCI' value. Therefore, SAR function is required because packets passed through VC merger may be interleaved. Fig. 5 shows proposed outgoing packet processor with VC mege for LER. As shown in Fig. 5, hardware for outgoing packet processor with VC merge consists of reassemble block(Receive Module), segmentation block(Transmit Module), VC merge controller(FPGA), merge table, PCI bus bridge and VC merge manager(CPU). PCI bus bridge and CPU are shared with incoming packet processor which operates as FE(Forwarding Engine).

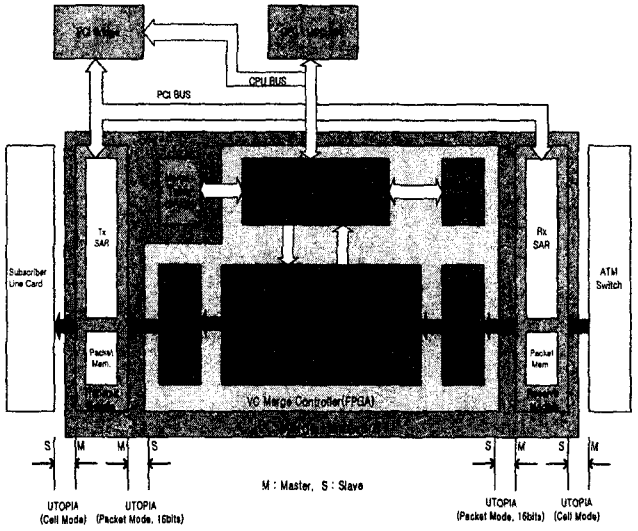

Fig. 5. Hardware architecture of outgoing packet processor including detailed VC merge controller

As shown in Fig. 5, that hardware board receive ATM cell from ATM switch fabric through UTOPIA-2(Universal Test & Operations PHY Interface for ATM Level 2) interface and reassemble the received cell in 'Receive Module' including SAR device and packet memory. The reassembled packets with AAL-5 type are transferred 'VC merge Controller' block for label merge based on merge table. That merged packets are sent to 'Transmit Module' and are segmented to ATM cell. Finally the segmented cells goes out phycal line interface card with 4xSTM-1 or 1xSTM4c through UTOPIA-2 interface. All hardware blocks are controlled by VC manager through CPU local bus or PCI bus.

3.3 Implementation of VC merge Controller

VC merge controller was implemented by FPGA. Fig. 5 shows the hardware architecture of whole outgoing packet processor including detailed internal architecture of VC merge controller. The proposed VC merge controller receives AAL5 type packet from Rx SAR through UTOPIA-2 packet extended mode. The packet contains a canonical header with RCH(Receive Channel Handle) of 16bits size which is used table address to lookup VC merge table. And the value is channel identifier related to ATM VPI/VCI value.

Fig. 6 shows the procedure that VC merge controller processes incoming packets for VC merge. During the packet processing, VC merge controller process with different mechanisms considering packet types ; Normal AAL5 packet, EFC(Extended Forwarding Control) packet and raw ATM cell. EFC packet is for MSC to exchange routing information with other router and raw ATM cell is to operate for ATM based MPLS system as ships in night mode. AAL-5 type packets are transferred to Tx SAR after processing by VC merge controller.

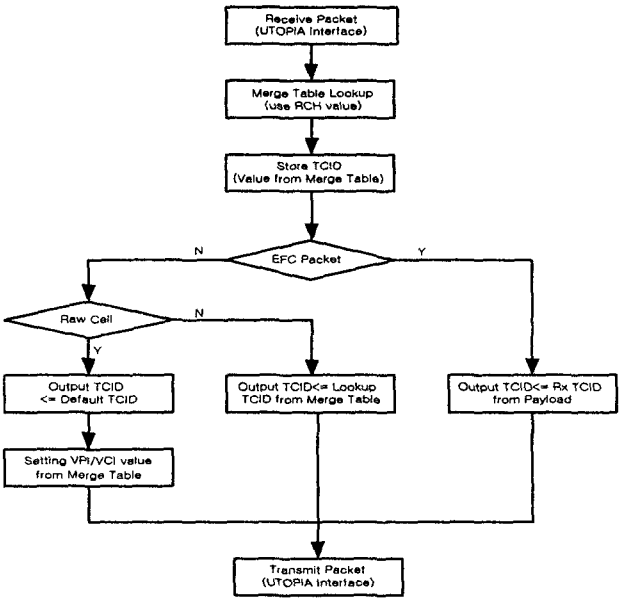

Fig. 6. Packet process mechanism in VC merge Controller

Fig. 7 shows hardware block diagram for VC merge controller implemented with FPGA.

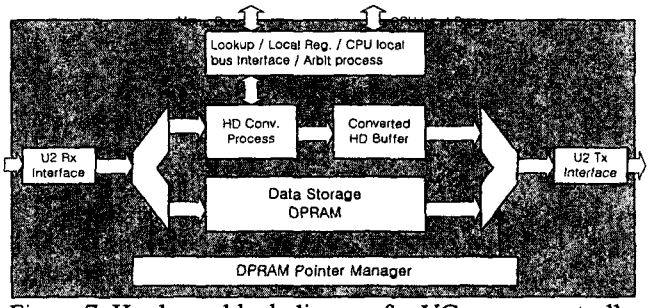

Figure 7. Hardware block diagram for VC merge controller

First, VC merge controller receives packets through 'U2 interface' and sends the header of packet to header conversion process(HD Conv. Process) and the body of packet to dual port RAM for data storage(Data Storege DPRAM). Second, 'HD Conv. Process' block does header conversion functions based on result of look-up operation of merge table and packet type information from

corresponding packet header as packet processing mechanism shown in Fig. 6. Third, the converted header and packet body from dual port memory are multiplexed under control of 'DPRAM Pointer Manager' and goes to phical line card through 'U2 Tx Interface'.

During the header conversion, VC merge controller access merge table for outgoing channel identifier with index value of RCH. Fig. 8 shows the corresponding result of this loo-up as regard to normal AAL-5 data packet, EFC packet and raw ATM cell.

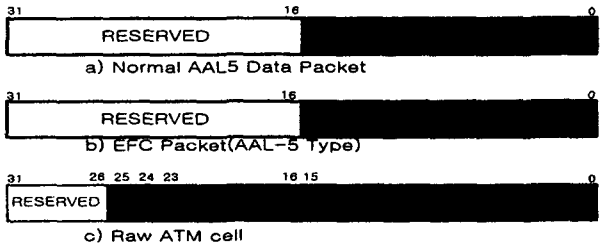

Fig. 8. Format of VC merge table

4. Traffic Management of MPLS LER

The proposed outgoing packet processor provides traffic management function for required QoS from Internet user and to enhance TCP/IP efficiency. In receive side(Rx SAR), the traffic management uses buffer classification method which uses separate buffer due to service class considering ATM service categories. Table 1 shows ATM service class supported in our outgoing packet processor

Table 1 ATM Service class support

Service Category	CBR	rt-VBR	nrt-VBR	UBR with PCR	UBR without PCR
Priority	0	1	2	3	none
TM Algorithm	PCR only	PCR/SCR	PCR/SCR	PCR only	UBR
PCR	x	x	x	x	
PCR Limit	x	x	x	x	
SCR		x	x		
SCR Limit		x	x		
MCR					
MCR Limit					

In transmit side(Tx SAR), the traffic management uses buffer classification method and appended MRED(Modified Random Early Discard), EPD and PPD algorithm. Especially, traffic shaping function was applied to transmit side based on ATM service categories.

5. Conclusions

It is impossible to meet user demands with conventional routing technologies under the circumstance of increasing dramatically user traffic in the Internet. MPLS has been proposed as a solution to resolve this problem. MPLS is a paradigm to integrate higher layer's software routing functions including layer-3 routing with layer-2 switching. But, the exponential growth of Internet traffic brings out of label space. One scalable solution to cope with this problem is to introduce flow merging technique, as referred to VC merge function in ATM based MPLS system.

We have implemented outgoing packet processor of LER for ACE2000 MPLS system based on ATM switching system. The proposed outgoing packet processor for LER includes VC merge and traffic management function. VC merger was implemented using FPGA for VC merge controller and was based on SAR function. And, we have verified that the outgoing packet processor works well with 622Mbps packet processing power per HFMA through simulation and real traffic test. The proposed outgoing packet processor provides the performance of 2.5Gbps in case of one module MIM configuration. This hardware based egress packet processor gives the expandability to the router as the ATM switch module size is large.

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