A Low Jitter on Multiple Frequency of Dividing Ratio Changeable Type ADPLL

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Abstract: In this paper, we proposed a new control system of the dividing ratio changeable type ADPLL (DCPLL). The DCPLL has been designed by us. However, in the DCPLL, there are some problems such as this curcuit is increased the output jitter on multiple frequency, and the output jitter is large on steady state. Then, the output jitter characteristic on multiple frequency is improved by using "rest-control" system. Also, output jitter decreases by using "W-edge (positive edge & negative edge)" system. We confirmed some characteristics of the DCPLL with the circuit simulator, PSpice.

1. Introduction

The technology of various high levels is demanded with development of digital information and a communication field such as portable telephones, digital broadcast, wireless LAN, and so on. Phase locked-loops (PLL) is one of the synchronous methods which is the important technology supporting these digital products. PLL is widely applied to various fields, such as timing recovery on digital communication systems, frequency synthesizers, a clock generator of various systems and so on. In recent years, system on a chip (SOC) which integrates various systems into one chip has been advanced. For this purpose, several All Digital PLL (ADPLL) have been proposed.

In the conventional basic ADPLL, the lock-in range is narrow. Because the fixed clock is divided by the fixed ratio, and the phase of the input signal and the output signal are controlled by adding pulses of the fixed clock or subtracting one. Also, in the conventional basic ADPLL, the pull-in characteristic (lock-in range, pull-in time) and the jitter suppression effect in the steady state are opposite relations. Therefore, when the lock-in range is made large and pull-in time is made high-speed, the jitter suppression effect is low. Conversely, when the jitter suppression effect is made improvement, the pull-in characteristic is bad.

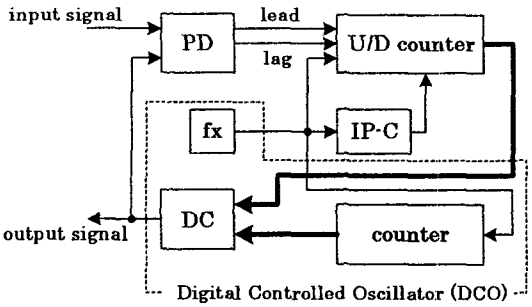
For improving the above problem, the dividing ratio changeable type ADPLL (DCPLL) which is able to adjust automatically for the fixed dividing ratio has been proposed by authers. In the DCPLL, extremely the wide lock-in range is obtained by setting up wide between a maximum value and a minimum value of the dividing ratio. Also, in the DCPLL, the multiple output signal with fixed pulse interval can be obtained.

In this paper, a new DCPLL is proposed that output signal of the low jitter is equivalent to the time of the basic operations (input frequency : output frequency = 1 : 1) on multiple frequency. An initial pull-in time on multiple frequency is 1 cycle of input signal, and it is shortest time. And, in the proposed DCPLL, the very large lock-in range is obtained in the maximum value of the dividing ratio by choosing a big value. Furthermore, the output jitter is reduced to 1/2 by counting both the positive edge of the fixed clock and the negative edge of one. Also, in the proposed DCPLL, when the frequency of the fixed clock is set to 1/2, the performances in the proposed DCPLL is equivalent to the performances in the basic DCPLL which is counted by only the positive edge.

2. Circuit organization and a principle operation

2.1 The basic dividing ratio changeable type ADPLL (DCPLL)

The basic dividing ratio changeable type ADPLL (DCPLL) is shown in Fig. 1. Circuit organization is the binary quantized phase detector (PD), the Up/Down counter (U/D counter), the counter (Counter), the digital comparator (DC), the fixed clock (fx), the initial pull-in counter (IP-C), and the digital controlled oscillator (DCO) which consists of the counter (Counter), the digital comparator (DC) and the fixed clock (fx).



PD : Phase Detector
U/D counter : Up/Down counter
IP-C : Initial Pull-in counter
DC : Digital Comparator
fx : fixed clock

Fig.1 Block diagram of the basic DCPLL

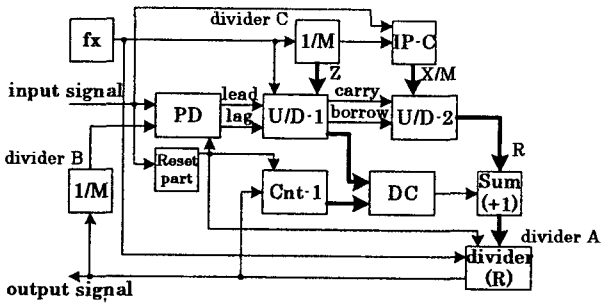
In the basic DCPLL, the frequency of the output signal is determined by carrying out changeable dividing ratio according to the frequency of the input signal, and the fixed

clock is divided by the changed dividing ratio. In the DCO, the dividing ratio is determined by the counted value of the fixed clock during 1 cycle of the input signal, and the frequency of the output signal is determined. In the PD, between the phase of the input signal and the phase of the output signal is compared. When the phase of the input signal is progressing compared with the phase of the output signal, the lead signal is outputted. Also, when it is behind the lag signal is outputted. In the U/D counter, the dividing ratio of the DCO is controlled. When the lead signal is outputted from the the PD, In the U/D counter, the positive edge of the fixed clock passed in the time is counted down. As against, In the U/D counter, when the lag signal is outputted, the positive edge of the fixed clock passed in the time is counted up. So, the phase error is detected. Therefore, when the phase error is less than 1 pulse of the fixed clock, this count operation is not performed and the error correction is not performed. Since this error influences the following loop, the output jitter of less than 3 pulses of the fixed clock arises.

Moreover, when the output signal is M multiple frequency, as shown in Fig. 4 (a) since the dividing ratio which controls the output signal becomes the quotient of X/M as the fixed clock is set to X during 1 cycle of the input signal, the rest Z is arised in X/M,and this becomes the output jitter. Here, since a maximum value of the rest Z is M-1, when multiple frequency is performed, there are problems that the output jitter increases in proportion to increase of the multiple ratio M.

2.2 The proposed dividing ratio changeable type ADPLL (DCPLL)

The proposed dividing ratio changeable type ADPLL (DCPLL) is shown in Fig. 2. Circuit organization is the binary quantized phase detector (PD), the Up/Down counter 1, the Up/Down counter 2 (U/D-1, U/D-2), the counter (Cnt), the digital comparator (DC), the fixed clock (fx), the initial pull-in counter (IP-C), the summer (Sum), the divider A (divider), the divider B (1/M) and the divider C (1/M).



PD : Phase Detector
U/D : Up/Down counter
Cnt : counter
IP-C : Initial Pull-in counter
DC : Digital Comparator
fx : fixed clock

Fig.2 Block diagram of the proposed DCPLL

Here, as shown in Fig. 3, In the U/D-1, the count value of the positive edge of the fixed clock and the count value of the negative edge of the fixed clock is outputted each other. When the phase error arises, both the positive edge and the negative edge (W-edge) of the fixed clock are counted, and error correction is performed. Therefore, since the errors will be rectified for every 1/2 circle of the fixed clock, the phase error which cannot make error correction becomes under 1/2 circle of the fixed clock, and can reduce the output jitter to 1/2. Moreover, in the proposed DCPLL, since it counts not only the positive edge but the negative edge when the frequency of the fixed clock is set to 1/2 , the performance which is equivalent to the basic DCPLL can be obtained.

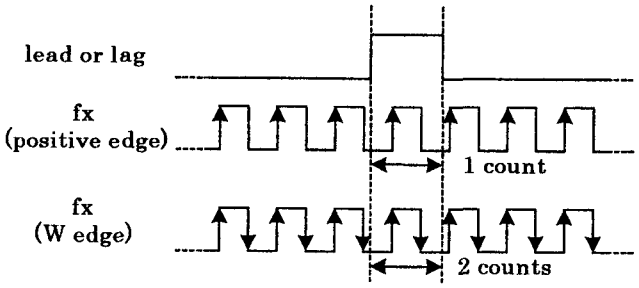


Fig.3 Waveforms of the W-edge

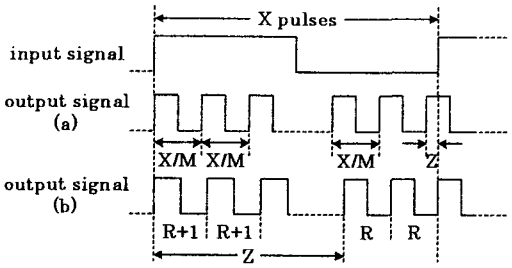


Fig.4 Waveforms of the rest-control on multiple frequency

As shown in Fig. 4 (b), the low jitter of the output signal is attained regardless its ratio on multiple frequency, by giving the method of removing the output jitter which corresponds to the rest considering as R+1 the dividing ratio of Z cycle for the output signal M cycle of the 1 cycle of the input signal. In the U/D-1 the W-edge of the fixed clock passed the phase difference between the input signal and the output signal is counted, and it is counted up or counted down by the lead signal and the lag signal from the PD. When their count-values are reached M, the U/D-2 which controls the dividing ratio is counted up (+1), and the value in the U/D-1 becomes to 0. Conversely, when the value becomes less than 0, the U/D-2 of the dividing ratio control is counted down (-1), and the value is set to M-1 in the U/D-1. Thereby, the output value of the U/D -1 turns into the value which always corresponds to the rest Z. The Cnt is M counter to count the cycle of the output signal. In the Sum, the output value of the Cnt and the output value of U/D-1 are compared in the DC, and the output value of the U/D-2 is carried out +1 until they are in agreement. The Sum is the summer. Consequently, the dividing ratio is set to R+1 for Z cycle during M cycle of the output signal. So,

the output jitter corresponding to the rest is negated, and the output signal of the low jitter can be acquired on multiple frequency.

2.3 An initial pull-in process

As the input signal is impressed, the counter will count the number of pulses of the fixed clock passed during 1 cycle of the input signal from the positive edge of the 1st input signal to the positive edge of the 2nd input signal. The initial setting of this value is carried out, and the frequency error of the input signal and the output signal is removed. And, the phase error is removed by resetting the dividing counter in the 2nd positive edge of the input signal. Therefore, the output signal locks in the 2nd positive edge of the input signal.

On the initial pull-in of the multiple frequency, when it is going to obtain the output frequency of M times for input frequency, the dividing ratio R chosen as 1/M in the basic operation. So, M counter is inserted in the preceding stage of the initial pull-in counter. The value of the initial pull-in counter is set to the U/D 2, and the value of M counter is set to the U/D -1. Therefore, the frequency error between the input signal and the output signal is removable. After frequency error removal, since the phase error is removed by resetting the dividing counter in the 2nd positive edge of the input signal, the initial pull-in time becomes the shortest time during 1 cycle of the input signal.

3. Characteristics

3.1 The output jitter on multiple frequency

In the proposed DCPLL, the 1/M counter is inserted in a feedback loop, and when the output signal of M multiple is acquired, the dividing ratio of the DC serves as an integer part of the value which divided M for the fixed clock X passed. Consequently, the number Z of the fixed clock which is equivalent to the rest as shown in Fig. 4 (a) exists in 1 ~ (M-1) the range, this influences a loop as the output jitter. Also, the value which is equivalent to this rest increases in proportion to the multiple ratio M from 1 ~ (M-1).

As shown in Fig. 4 (b), this increasing the output jitter can be controlled by adding +1 into the dividing ratio of the DCO during the Z cycles of the output signal. So, in the proposed DCPLL, the summer is inserted to add +1, and the comparator is inserted to control Z cycle. Therefore, in multiple frequency of the basic DCPLL, the more the multiple ratio is increased, the more the output jitter is increased. In the proposed DCPLL, the dividing ratio is set to R+1 for Z cycle during M cycle of the output signal. And, the output jitter corresponding to the rest is negated. So, the problem is improved, and the fixed output jitter can be kept regardless of the multiple ratio. The authers call this system "rest-control" system.

3.2 The output jitter on the W-edge

On the stationary state, when the ratio *fx/fin* (= *Tin/Tfx*) is not an integer, the phase error arises between *fin* of the input signal and the X of fixed clock. Here, *fin* is the input signal ,and *fx* is the fixed clock.

In order to detect the errors in the positive edge of the fixed clock, the phase error is less than 1 cycle, and the output jitter was 3 cycles. In the proposed DCPLL, in order to detect the errors on the W-edge of the fixed clock, the phase error is less than 0.5 cycles, and the output jitter is 1.5 cycles. In the DCPLL, the output jitter σ_{out} is shown as follows.

$$\sigma_{out}(basic) < \frac{2T_{fx}+T_{fx}}{T_{in}} 2\pi = \frac{f_{in}}{f_x} 6\pi \quad \cdots\cdot(1)$$

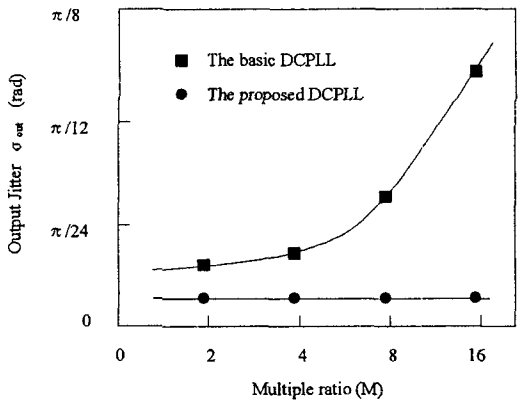
$$\sigma_{out}(propose) < \frac{f_{in}}{2f_x} 6\pi = \frac{f_{in}}{f_x} 3\pi \quad \cdots\cdot(2)$$

That is, the frequency of the fixed clock set to high-frequency, the output jitter can be low. The auters think that in the DCPLL, the output jitter can be controlled the low itter if the fixed clock is made more high-speed. So, we propose a new system which controls the phase error by the W-edge. Therefore, in the proposed DCPLL, the output jitter reduces 1/2 scale compared with the basic DCPLL. Also, in the proposed DCPLL, the output jitter characteristics are equivalent to the basic DCPLL, when the frequency of the fixed clock is set to 1/2 of the basic DCPLL.

4. Results

4.1 Simulation results of the output jitter on multiple frequency

Fig.5 shows the output jitter characteristics on multiple frequency. By Fig.5, the more the multiple ratio is increased, the more the output jitter is increased. Here, in the proposed DCPLL, the output jitter can be kept the fixed regardless of the multiple ratio. Therefore, the output jitter is the constant value on the large multiple ratio. So, in the proposed DCPLL, the frequency can be obtained high-frequency regardless of the multiple ratio.



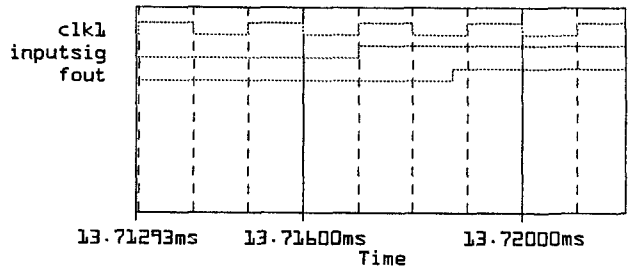
(fin=4.3[kHz], fx=2[MHz])

Fig.5 Output jitter characteristic on multiple frequency

4.2 Simulation results of the output jitter on the W-edge

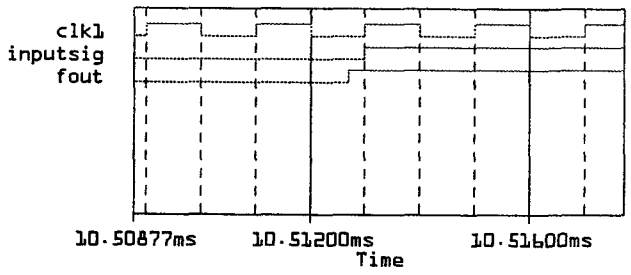
The input signal is earlier than output signal as shown in Fig.6. Also, the input signal is earlier than the output signal as shown as Fig.7. By Fig.6 and Fig.7, We can tell that the output jitter is 1.5 cycles. Here, this point is the output signal. In the DCPLL, since the output signal is controlled by the fixed clock, the output signal depends on the fixed clock. But, the output signal is late by sampling error. Therefore, as shown in Fig.7, the phase error is 0.5 cycles in the maximum, when the input signal is later than the output signal. And, as shown in Fig.6, the phase error is 1.0 cycle in the maximum, when the input signal is earlier than the output signal. So, as shown in Fig.8, the output jitter is 1.5 cycles.

Fig.9 shows the output jitter characteristics on the W-edge. By Fig.9, in the proposed DCPLL, the output jitter reduces 1/2 scale compared with the basic DCPLL. So, in the proposed DCPLL, the output jitter characteristics can be equivalent to the basic DCPLL, when the frequency of the fixed clock is set to 1/2 of the basic DCPLL. Also, in the proposed DCPLL, when the fixed clock is set to high-frequcncy, the output jitter is kept low.



clk1: fixed clock
inputsig: input signal
fout: output signal
(fx=2[MHz], fin=4.3[kHz], M=1)

Fig.6 Waveforms of output jitter simulation
(Input signal leads)



clk1: fixed clock
inputsig: input signal
fout: output signal
(fx=2[MHz], fin=4.3[kHz], M=1)

Fig.7 Waveforms of output jitter simulation
(Input signal lags)

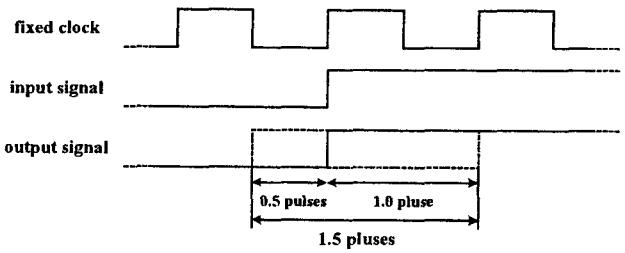
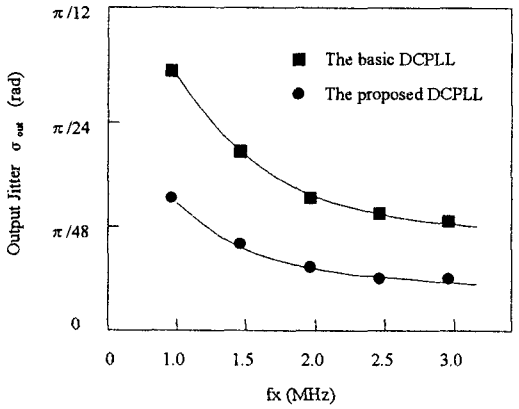


Fig.8 Waveforms of output jitter simulation
(Input signal leads and lags)



(fin=4.3[kHz], M=1)

Fig.9 Output jitter characteristic on the W-edge

5. Conclusions

In the proposed DCPLL, the output jitter is the constant value regardless of the multiple ratio by using "rest-control" system. Therefore, the output signal is obtained high-frequency on the large multiple ratio. Also, in the proposed DCPLL, the phase error is improved by using "W-edge (positive edge & negative edge)" system. Therefore, in the proposed DCPLL, the output jitter reduces 1/2 scale compared with the basic DCPLL. Also, the proposed DCPLL performs equivalent to the basic DCPLL, when the frequency of the fixed clock is set to 1/2 of the basic DCPLL.

References

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