Programmable Digital On-Chip Terminator

*Su-Chul Kim, Nam-Seog Kim, Tae-Hyung Kim, Uk-Rae Cho, Hyun-Guen Byun, *Suki Kim

SRAM Design, Memory Division, Samsung Electronics, Korea, 449-711
* Department of Electronics Engineering, Korea University, Anam-Dong, Sungbuk-Gu, Korea, 136-701

Abstract :
This paper describes a circuit and its operations of a programmable digital on-chip terminator designed with CMOS circuits which are used in high speed I/O interface. The on-chip terminator matches external reference resistor with the accuracy of ± 4.1% over process, voltage and temperature variation. The digital impedance codes are generated in programmable impedance controller (PIC), and the codes are sent to terminator transistor arrays at input pads serially to reduce the number of signal lines. The transistor array is thermometer-coded to reduce impedance glitches during code update and it is segmented to two different blocks of thermometer-coded transistor arrays to reduce the number of transistors. The terminator impedance is periodically updated during hold time to minimize inter-symbol interferences.

1. Introduction

Resistive terminations are required in high-performance signaling systems to absorb traveling waves for incident-wave switching: preventing reflections and their attendant inter-symbol interference [1]. In high speed signaling between CMOS chips, it is advantageous to build on-chip termination resistors rather than off-chip resistors because the off-chip termination always results in an un-terminated stub consisting of the package parasitic and the internal circuitry and introducing large reflections into the signal line. There are two methods of adjusting a CMOS resistor to an external reference resistor: analog control and digital control. The analog control [2] is usually not preferred because it is desirable to make 'V_{GS}-V_{th}' as large as possible to allow the largest swing in V_{DS} while remaining in the linear part of the resistive characteristic, where V_{GS} is the voltage between gate and source of MOSFET, V_{th} is the threshold voltage, and V_{DS} is the voltage between drain and source. Also since several terminators usually share the controller and the signals must travel long distance, the analog control voltage is susceptible to noise. Hence digital adjustment is preferable in CMOS chips [3]. This paper describes a CMOS circuit which can be adjusted digitally to generate controlled impedance of on-chip terminators for use in high-performance circuits.

2. Automatically adjustable digital on-chip terminator

In Figure 1, automatically adjustable digital on-chip terminator consists of following blocks:

(1) Programmable impedance controller (PIC): detects resistance of external reference resistor and generates digital impedance codes.
(2) CODE transmitter: transmits the digital codes, which are conveyed serially to all terminators at input pads to reduce the number of signal lines.
(3) CODE receiver: receives the serial codes and transmits the codes parallel to TERMINATOR.
(4) TERMINATOR: The pass gate CMOS resistor is used for good linearity, which is shown in Figure 2.

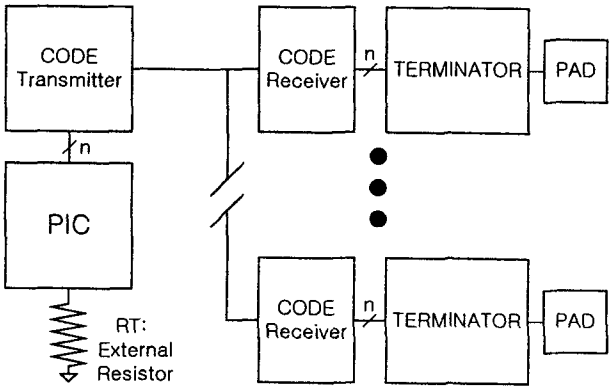

Figure 1. The block diagram of a automatically adjustable digital on-chip terminator

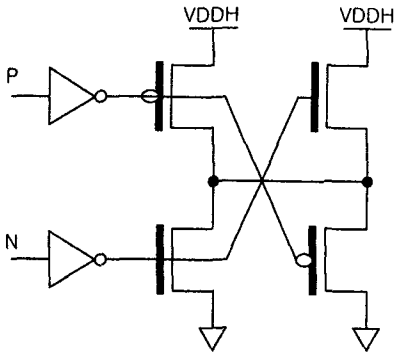

Figure 2. The pass gate CMOS resistor for TERMINATOR

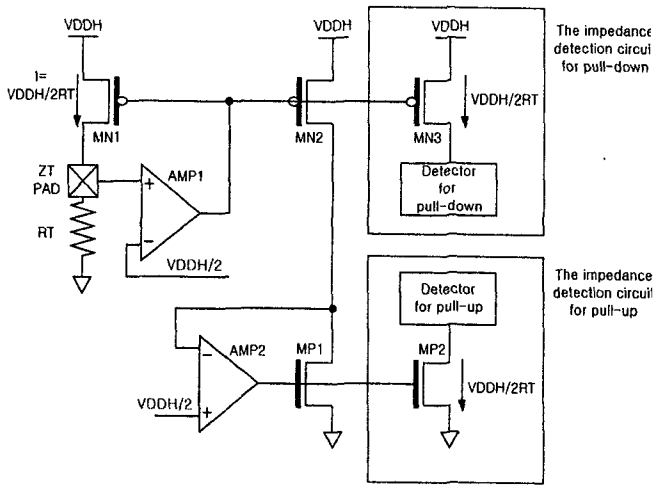

Figure 3. The schematic diagram of programmable impedance controller (PIC)

3. Programmable Impedance Controller (PIC)

The scheme of PIC is illustrated in Figure 3. An external off-chip resistor, RT, serves as the reference impedance. The resistance of RT is detected by measuring the current and voltage across RT. In Figure 3, all transistors operate in the saturation region acting as a current source. AMP1, an amplifier, makes ZT pad voltage level VDDH/2, where VDDH is interface voltage. Then the current through the external resistor is VDDH/2RT. And the current through MN1, MN2 and MN3 are equal to VDDH/2RT because they have the same bias condition. The current through MN3 is used to generate pull-down impedance codes. The current through MN2 flows into MP1 and AMP2 makes the drain voltage of MP1 VDDH/2. Then the currents through MP1 and MP2 are also VDDH/2RT. The current through MP2 is used to generate pull-up impedance code. The current generation method is so convenient as to make two or more impedance values, which are required in a chip.

An impedance detection circuit for pull-down is shown in Figure 4. The pull-down transistor array is simple nMOS array and coded in a segmented thermometer type. Because impedance code is updated while terminator is not turned off, an input signal distortion may happen. So a segmented thermometer code is used to minimize impedance glitch with a relatively small number of transistors. The pull down transistor array is shown in Figure 5.

The comparator generates a signal, UD, which is applied to an n-bit binary up-down counter. When the voltage at V_{MID} is higher than 1/2VDDQ, the comparator generates a high signal. This signal is applied to the up-down counter, and it will increment the control signal, BC, by one. This binary control signal is converted into segmented thermometer code, TCH and TCL. Then the total width of the array increases, causing the voltage at V_{MID} to decrease. Alternatively when the voltage at V_{MID} is lower than 1/2VDDQ, the comparator generates a low signal. Then the total width of the array decreases, causing the voltage at V_{MID} to increase. This process will continue until the waveform of V_{MID} alternates about 1/2VDDQ due to dithering of the transistor array.

A selector is used to detect whether a dithering condition occurs and to generate 'enable signal'. Once the dithering condition occurs, the control bit pattern BC alters between two codes 1-bit apart. It means that the impedance of transistor array alters between two values which are the nearest to the reference impedance. One value is lower than reference impedance and the other value is not. A meta-stability of comparator may cause another type of dithering pattern, which alternates between three codes. Once it is detected, the selector chooses center code, which generates the impedance nearest to the reference impedance. Figure 6 shows the selector circuit.

If the 'enable signal' is issued, a hold register stores one of the control bit patterns. This final bit pattern, called BCDA, is sent to the pull-down transistor array of all terminators, which are around the frame of the chip. If the power supply voltage and temperature remain constant, the bit pattern is stable due to the selector and the hold register. However, if either of these two external conditions varies, the data in the register is updated.

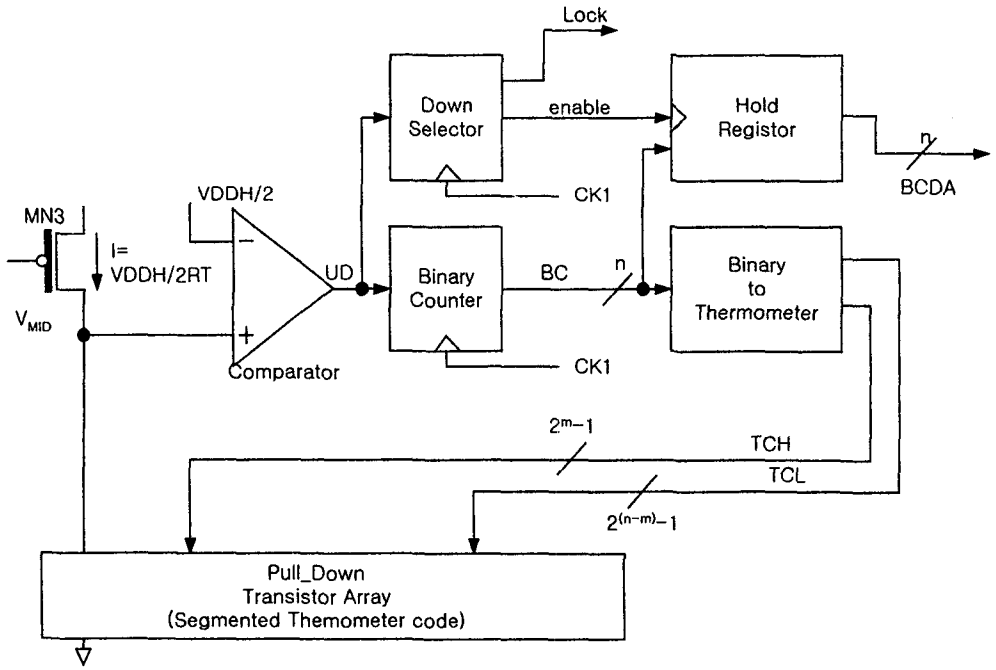

Figure 4. The block diagram of impedance detection circuit for pull-down

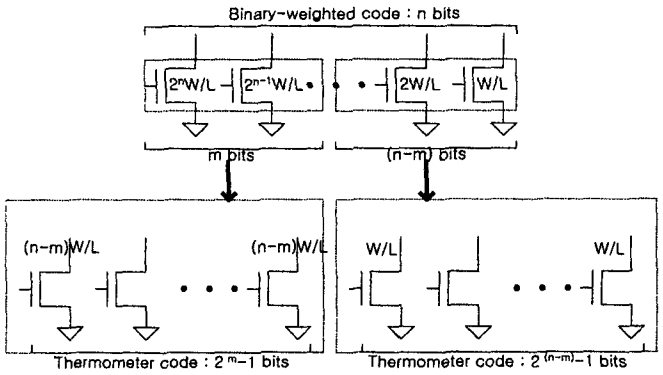

Figure 5. n bits binary-weight transistor array and m bits and (n-m) bits segmented thermometer transistor array for pull down transistor array.

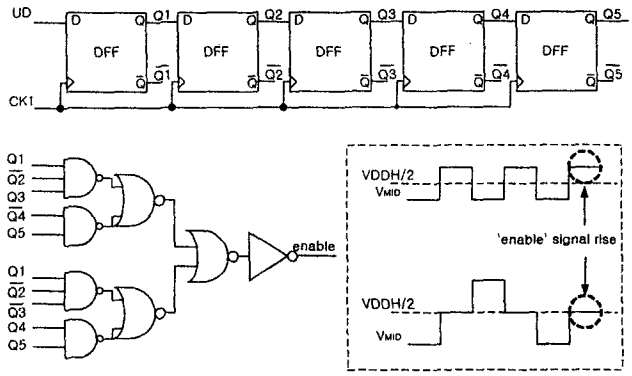

Figure 6. Digital code selector in impedance detection circuit

4. Digital impedance code update scheme

Figure 7 shows a timing diagram of the digital codes transmission. The codes are serially transmitted through only one line to reduce the number of data lines. The binary codes of pull-up and pull-down are 5-bits each. When UPDATE_CK is high, CODE_CK toggles 5-times. The codes for pull-down are transferred at the rising edge of CODE_CK. The shift register receives digital codes at the falling edge of CODE_CK. And then the series-to-parallel register accepts the codes in accordance with CK3U. The codes are converted into segmented thermometer codes. The codes for pull-up are transferred when UPDATE_CK is low.

Impedance updating at hold time of input signal makes input signal distortion minimal. The CK3U pulse occurs at every 64 cycles in accordance with SAM_CK, which is synchronous with data sampling clock and divided into 8 times. The circuit, in Figure 8, makes the CK3U pulse. An initial condition is that PREC is charged to VDD, LAT to ground (GND), and STBY keeps the gate of NN2 at GND previously. When rising edge of UPDATE_CK is applied to Short Pulse Generator (SPG), SPG generates low pulse, which is UPDATE_CK2. The low pulse makes STBY charged to VDD. Consequently when the rising edge of SAM_CK is applied, CK3U pulse is generated. Because CK3U pulse discharges the STBY to GND subsequently, this pulse occurs at every 64cycles.

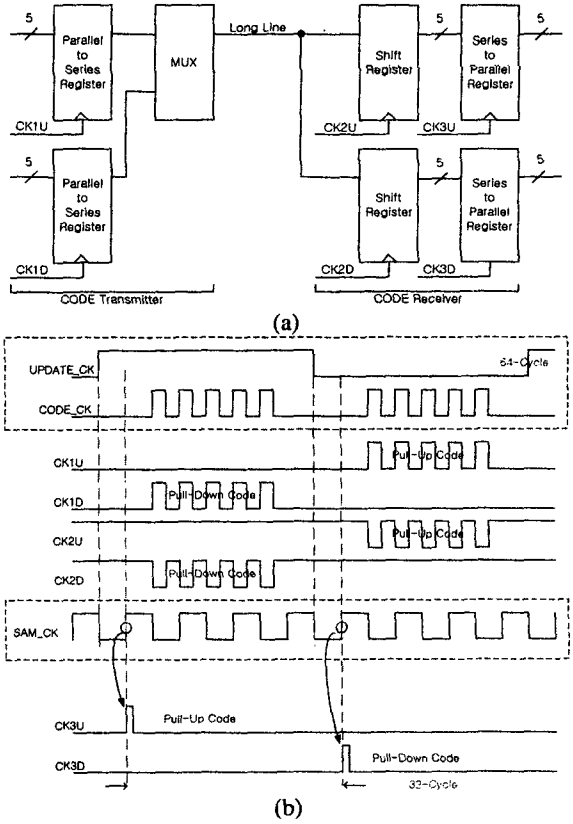

Figure 7. Block diagram (a) and clock timing diagram (b) for 5 bits digital impedance codes update scheme

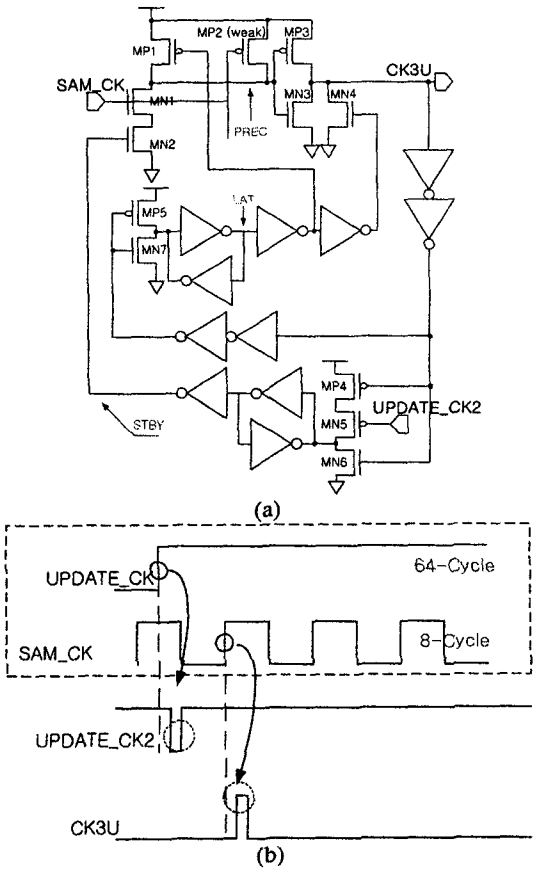

Figure 8. Circuit for generating CK3U in Figure 7 (a) and its timing diagram (b)

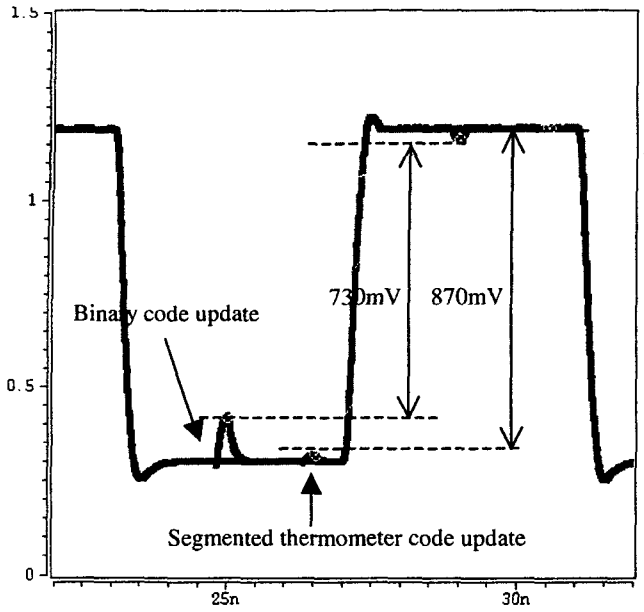

Figure 9. Spice simulation of signal noise, which is induced by the impedance digital code update

5. Simulation results

Figure 9 shows the Spice simulation result for the impedance glitch when impedance code is updated. In worst-case binary-weighted code update causes the signal distortion of about 170mV. But in case of segmented thermometer code update, the amount of distortion is reduced to about 30mV. The distortion occurs after data transition. This small amount of noise merely hurt the input signal.

The eye diagram at 1Gbps is shown in Figure 10. In this simulation, the impedance of driver is 25Ω and the equivalent impedance of Thevenin termination is 100Ω ±15%. The diagram shows data valid window of about 800pS at 400mV.

A worst-case analysis is performed. Simulation conditions are following; temperature varies from 0℃ to 110℃, voltage level varies from 1.45V to 1.55V, and Vth, which is threshold voltage of MOSFET, varies by ± 20mV. The simulation results are summarized at table 1 and maximum variation is ± 4.1%. The impedance of the pass gate type Thevenin terminator with digital codes traces well the resistance of external resistor. In Figure 11, the I-V curves show good linear characteristics across from 20% to 80% of VDDH.

Table 1. Simulation results for terminator in Figure 2.

Simulation Conditions	Variation of impedance
Temperature: 0°C~110°C	± 1.6 %
VDDH: 1.45~1.55V	± 1.3 %
Vth±20mV	± 1.2 %

References

[1] Gabara, T.J., Thompson, D.W., "A 200MHz 100K ECL output buffer for CMOS ASIC's," ASIC Seminar and Exhibit, 1990 Proceedings, Third Annual IEEE, 1990, Page(s): P8/5.1 -P8/5.4

[2] Knight, T.F. Jr., Krymm, A., "A self-terminating low-voltage swing CMOS output driver," Solid-State Circuits, IEEE Journal of, Volume: 23 Issue: 2, April 1988, Page(s): 457 -464

[3] Gabara, T.J., Knauer, S.C., "Digitally Adjustable Resistors in CMOS for High-Performance Applications," Solid-State Circuits, IEEE Journal of, Volume: 27 Issue: 8, Aug. 1992, Page(s): 1176 – 1185

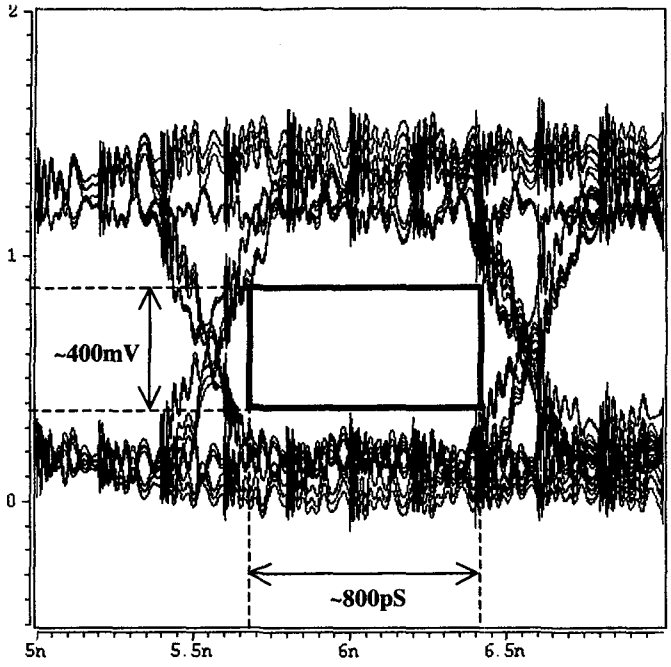

Figure 10. Simulated eye diagram with ± 15% variation of termination resistance

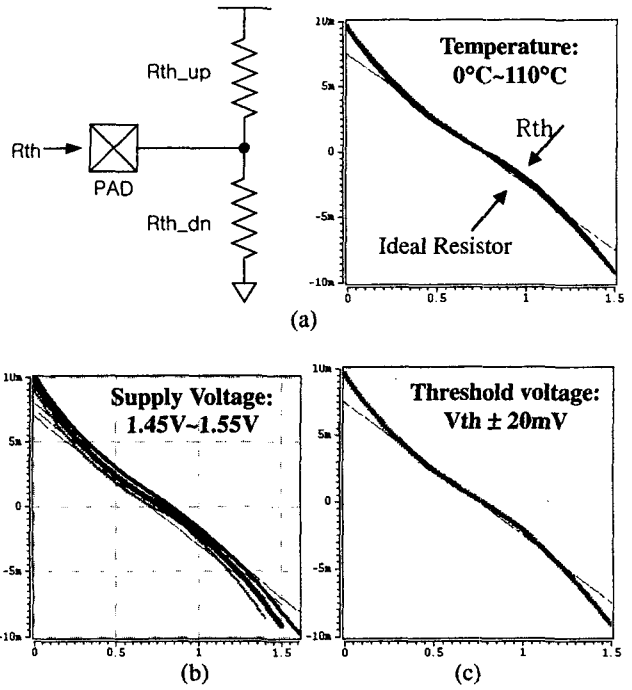

Figure 11. The simulated I-V curves for temperature variation (a), supply voltage variation (b), and threshold voltage variation (c)