Design on MPEC2 AAC Decoder

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Abstract

This paper deals with FPGA(Field Programmable Gate Array) implementation of the AAC(Advanced Audio Coding) decoder.

On modern computer culture, according to the high quality data is required in multimedia systems area such as CD, DAT(Digital Audio Tape) and modem. So, the technology of data compression for data transmission is necessity now. MPEG(Moving Picture Experts Group) would be a standard of those technology.

MPEG-2 AAC is the availableness and most advanced coding scheme for high quality audio coding. This MPEG-2 AAC audio standard allows ITU-R 'indistinguishable' quality according to at data rates of 320 Kbit/sec for five full-bandwidth channel audio signals. The compression ratio is around a factor of 1.4 better compared to MPEG Layer-III, it gets the same quality at 70% of the bitrate.

In this paper, for a real time processing MPEG2 AAC decoding, it is implemented on FPGA chip.

The architecture designed is composed of general DSP(Digital Signal Processor). And the Processor designed is coded using VHDL and C language. The verification is operated with the simulator of C language programmed and ECAD tool.

1. Introduction

New digital standard is exact to the technology that is the electrical communication, entertainment and the information industry. MPEG-2 standard is developed by ISO and IEC WG11 and ITU-T is also admitted to standard.

The famous specification of MPEG audio is MPEG-1 Layer-III(MP3) which technology is very useful in Internet area based on PC users. MPEG-2 AAC(Advanced Audio Coding) is not compatible with MPEG-1 but it has a high compression(about 1/20) and accepts a high quality, so to be excellent at the perceptual audio coding now.

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Also, afterwards MPEG-4, the audio specification able to compare with AAC. Perhaps MPEG-1 would disappear from the advanced technology of multimedia area. AAC is able to accept into the future audio technology. Thus, it tries to satisfy the completely standard. But AAC has a difficult problem of the technology that have to use a high performance DSP

In this paper, for the design of the exclusive use AAC decoder, the author implemented MPEG-2 AAC 2-channel main profile decoder(M2.0.0.0) on FPGA chip.

In this scheme, the author performed the optimizations of the algorithm and hardware architecture of AAC decoding using the DSP core part designed. And according to the given standard, the evaluation of the audio quality is performed. The organization of this paper is as follows: Sec. 2 illustrates the theoretical background for MPEG-2 AAC Layer-III and related to H/W architecture. Sec. 3 addresses the proposed algorithm and designs AAC decoder and it is experimented for the performance evaluation in sec. 4. Lastly, the conclusion is drawn in Sec. 5.

2. Theoretical background

ISO13818-7 MPEG-2 audio NBC(Non-Backwards Compatible) is standard that is called AAC. According to the using purpose of the system, MPEG-2 has several profiles that could be controlled by the specifications of the encoding and decoding. There are several types in MPEG like as Main profile could be supported max. 8.1 channels and LC(Low Complexity) profile is composed of 2 channels that is fitted portable audio system. These 2 kind of the profiles is using 8KHz ~96KHz sampling frequency.

It is detailed to represent A.L.I.D based on the profile. A means that is number of channels, L means that is number of LFE(Low Frequency Enhancement) channels, I means

that is number of coupling channels which is independently converted and lastly, D means that is number of coupling channels which is dependently converted. Ability of AAC decoder of each profile is represented in Table 1.

Table. 1. Ability of AAC decoder of each profile.

# of main audio channel	Main profile	LC profile	SSR Profile
1	1.0.0.0	1.0.0.0	1.0.0.0
2	2.0.0.0	2.0.0.0	2.0.0.0
3	3.0.0.0	3.0.0.1	3.0.0.0
4	4.0.1.0	4.0.0.1	4.0.0.0
5	5.1.1.1	5.1.0.1	5.1.0.0
7	7.1.1.2	7.1.0.2	7.1.0.0

AAC decoder is composed of the several tools as like Bitstream formatter, Noiseless decoding, Inverse quantizer, Scale factors, M/S, Prediction, Intensity/coupling, TNS, Filter bank, and Gain control.

Main profile must have a high compression rate and audio quality at the environment of the unlimited computing source. LC profile is not use Prediction and Gain control tools and limits the order of TNS filter in the case of the limited computing source. SSR profile uses minimum bitrate at the low bitrate communication environment and the audio bandwidth is constrainedly limited using Gain control tool. In this scheme, M2.0.0.0 means that 2 main audio channels of Main profile, 0 LEF channel, 0 Independent coupling channel and 0 independent coupling channel. In the Table 2, the use of each tool is represented that require or optional.

Table. 2. The contents of AAC decoder tool.

Tool name	Required/Optional
Bitstream formatter	Required
Noiseless decoding	Required
Inverse quantizer	Required
Scale factors	Required
M/S	Optional
Prediction	Optional
Intensity/coupling	Optional
TNS	Optional
Filter bank	Required
Gain control	Optional

The decoder architecture of AAC main profile is shown in Fig. 1. AAC is using ISO13818-7 std. audio bitstream that has two parts, the one is ADIF(Audio Data Interchange Format) and the other one is ADTS(Audio Data Transport Stream). The type of each audio format is shown in Fig. 2 and 3.

ADIF is not used at the network environment of on-line because that is the storage mass, so playing is impossible at some point of bitstream but ADTS is possible playing at the network environment because that has sync-word, CRC and frame length also stored into mass.

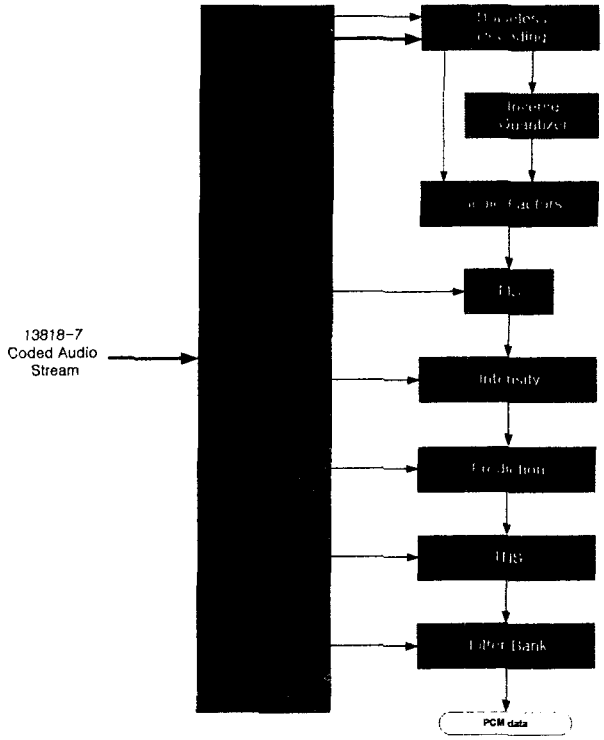

Fig. 1. The decoder architecture of AAC main profile.

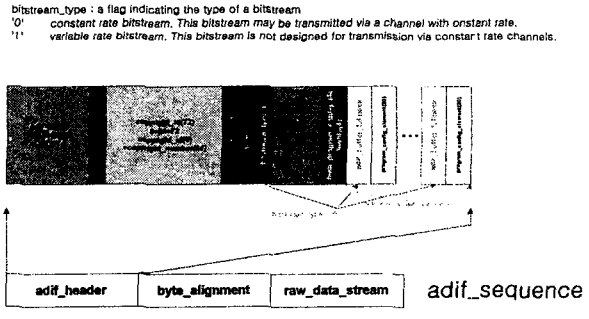

Fig. 2. ADIF bitstream.

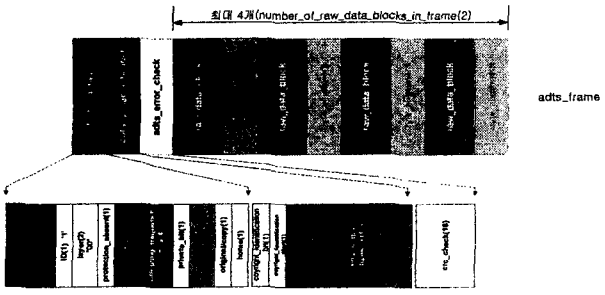

Fig. 3 ADTS bitstream

3. AAC decoder chip design

3.1 DSP core

In this scheme, while AAC decoding, each tool requires the dynamic range about 96dB. For the satisfied precision with 96dB, 8bits exponents and 24bits mantissas is used for the compatible IEEE single-precision(32bits) format also accepted pipeline architecture for the increasing of processor speed.

The processor H/W architecture of AAC decoding proposed is entirely hardwired, and composed of FPU(32bits floating and 24bits fixed for point unit), SEU(Shifter Exponent Unit), ACU(Address Controller Unit) and ALU(Arithmetic Logic Unit). External dada bus is two(A and B) and has 32bits data width. ACU memory pointer is composed of APL, BPL and CPL. The entire block diagram of DSP core proposed is shown in Fig. 4.

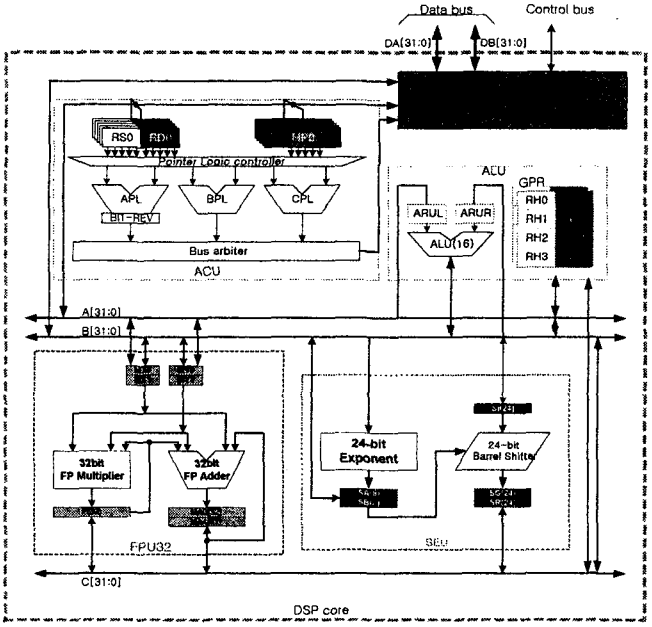

Fig. 4. The entire block diagram of DSP core proposed.

3.2 IMDCT performer

IMDCT which process the operation of many complex number so must be processed high speed while decoding and it requires many linear buffer memory. The flow diagram for complex number with butterfly operation is shown in Fig. 5 and the order for the effective operation of data streaming is rearranged in this figure.

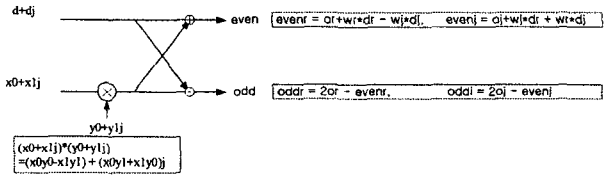

Fig. 5. The flow diagram of complex number by butterfly operation.

The memory arrangement method of complex number is shown in Fig. 6. The real and imaginary part of input data is each assigned into the independent linear memory. At complex number coefficient, real part is assigned into even position and vice versa.

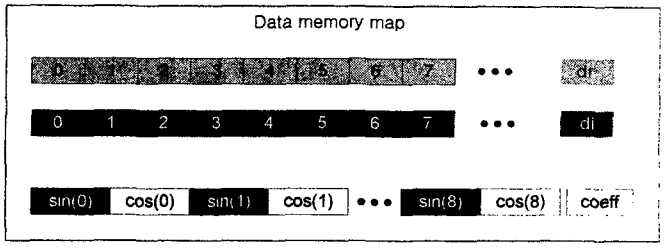

Fig. 6. The arrangement of IMDCT data-stream on memory map proposed.

In LONG_BLOCK case of IMDCT, it requires 2048 linear memory so the author composed the process of memory overlap for the effective memory management of the transform processing. It is shown in Fig. 7.

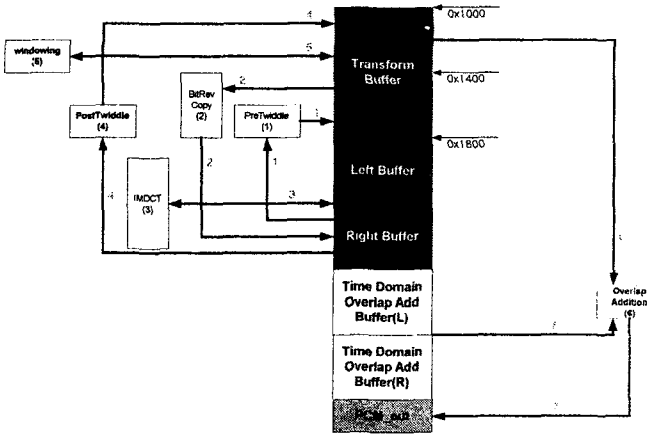

Fig. 7. The memory map of transformation proposed.

4. Design synthesis and implementation

In the progress of the chip implementation, Synopsys V9905, XILINX foundation V1.5, Verilog-XL(CADENCE V9905), and Active-VHDL V3.0 which are supported from IDEC(IC Design Education Center, KAIST, in KOREA) are used and to verify the algorithm of this scheme, Visual-C V6.0 and Matlab V5.3 are used. FPGA is used with XILINX(Virtex XCV300 300K Gate). Also the author programmed the application programs, which are AAC decoder player(PC window98/NT), ISO13818-7 verification software, and ROM Table generator for cosine account.

FPU functional simulation of DSP core proposed is shown Fig. 8. and the PCM output of AAC decoding by Verilog timing simulation is shown in Fig. 9. Through the this implementation, the author confirms that the stable operational frequency is 19MHz, 64 3-state buffers, 137

ports, 1,273 CLBs and 288,125 Gates. According to the decoding time of 1 frame, about 1.7*10^6 clock cycle is required so it is satisfied that the realtime decoding is possible at 20MHz. As a result, the AAC decoder designed is completely compatibility with ISO13818-7.

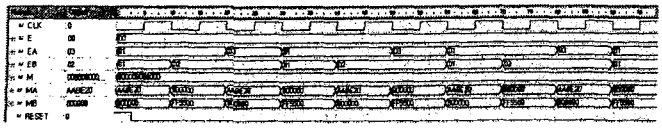

Fig. 8. FPU functional simulation.

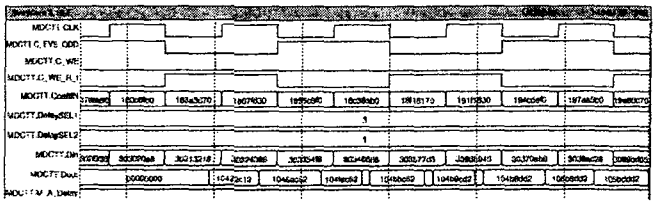

Fig. 9. PCM output of AAC decoding by Verilog timing simulation

And, the final PCM output of AAC decoding by DSP core proposed is shown in Fig. 10 and we could be saw 1,724,625 clock cycles per 1 frame decoding in here.

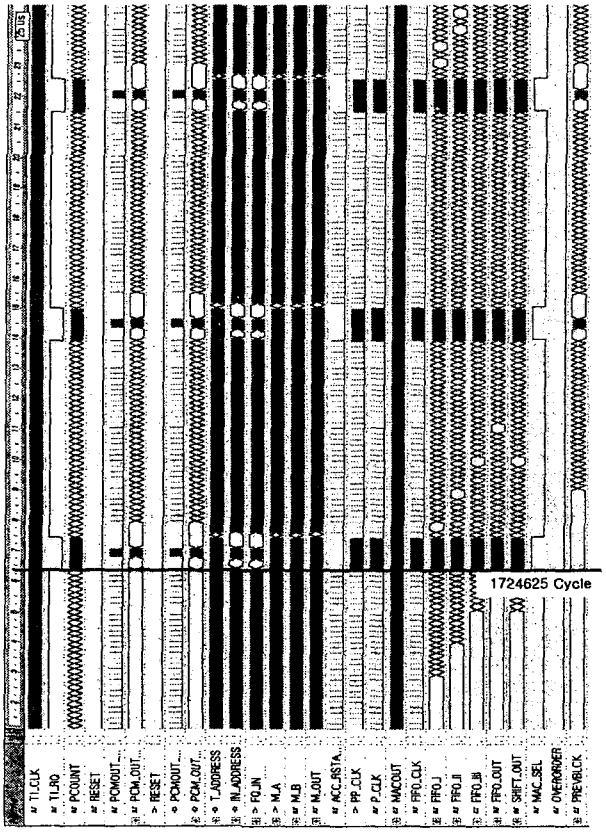

Fig. 10. The final PCM output of AAC decoding by DSP core proposed.

5. Conclusion

In this paper, the author optimized the calculation algorithm of AAC decoder for small H/W system size. It was reduced the number of table to 512 and has the low error with 0.02%

It is reduced that the number of table and operation quantity in filter bank thus, realtime decoding could be performed.

And in this scheme, the appearance of the neck of a bottle is conquested in the calculation of DSP core. For the access to memory, ACU is used, and the data is processed by pipeline and has the compatible format with IEEE single precision in FPU. In here, 37KB RAM and 27K ROM is used in AAC decoder.

For the low overhead of the instructions, the DSP core proposed is designed on the operational clock 20MHz(20MIPS) and AAC M2.0.0.0 could be played in the realtime.

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