Sub-One volt DC Power Supply Expandable 4-bit Adder/Subtracter System using Adiabatic Dynamic CMOS Logic Circuit Technology

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Abstract: The expandable 4 bit adder/subtracter IC was designed using the adiabatic and dynamic CMOS logic (ADCL) circuit as the ultra-low power consumption basic logic circuit, and the IC was fabricated using a standard 1.2 μ CMOS process. As the result, the steady operation of 4 bit addition and subtraction has been confirmed even if the frequency of the sinusoidal supply voltage is higher than 10MHz. Additionally, by the simulation, at the frequency of 10MHz, energy consumption per operation is obtained as 93.67pJ for addition and as 118.67pJ for subtraction, respectively. Each energy is about 1/10 in comparison with the case in which the conventional CMOS logic circuit is used. A simple and low power oscillation circuit is also proposed as the power supply circuit for the ADCL circuit. The oscillator operates with a less one volt of DC supply voltage and around one milli-watts power dissipation.

1. Introduction

With the stream of refinement and high integration of LSI, the power reduction technology in which the grade is higher than the conventional CMOS circuit is desired by the advance on portable type equipment assuming the battery drive in which the market is expanding.

Under such background, the circuit technology called 'adiabatic circuit technology' has been studied, in which power reduction is more possible than the conventional CMOS circuit, and several papers on it were reported. The adiabatic and dynamic CMOS logic (ADCL) circuit has been also proposed [1]. Generally speaking, features of basic logic circuit using the 'adiabatic circuit technology' are as follows:

(1) Discharge and charge is done in the constant current in respect of the load capacity, using supply voltage which repeats increase and decrease at the fixed gradient. Then, the thermal loss of the energy at the channel resistance of the transistor is held low. The thermal loss of the energy decreases here and more, as it is longer, if the time spent for discharge and charge is long.

(2) By recovering the energy for the charging in the power supply, the energy is recycled.

In addition, following features are added in the ADCL circuit:

(1) The output voltage, the high level and low level of which are fixed without following supply voltage, can be retained.

(2) For the power supply, the ADCL can operate only in a sine wave voltage generator or a triangular wave voltage generator of the single phase. In case of ADL, it needs 4 phase periodical trapezoidal voltage sources.

(3) It is possible to constitute the logic-system by the simple connection that is similar to the conventional CMOS logic circuit.

In this paper, design, fabrication and evaluation of an ultra-low power expandable 4-bit adder /subtracter IC using ADCL basic circuit will be described.

Additionally, a simple and low power consumption oscillation circuit which outputs sine wave voltage which drives this IC, will be also presented.

2. Basic ADCL Circuit

Figure 1(a) shows the basic ADCL inverter circuit,which is composed of 2 MOS FETs, 2 diodes and a capacitor. To the terminal Φ, the triangular or sinusoidal voltage source is connected as the power source.

If the low level voltage is input to the terminal IN, then transistor M_1 comes into the 'cut-off' state and transistor M2 comes into 'on' state. In this case, the capacitor C_L is charged up to the voltage of V_P-Φ_D which is the high level of output voltage, where V_P is the maximum value of the supply voltage and Φ_D is the barrier potential of the diode(D_1, D_2). In the next, if the high voltage is input to the terminal IN, then transistor M_1 comes into the 'on' state and transistor M_2 comes into the 'cut-off' state. Thus, the capacitor C_L is discharged and the output voltage becomes Φ_D which is the low level of the output. The relationship among the supply voltage V_Φ, the input voltage V_{IN} and the output voltage V_{OUT} are shown in Fig.1(b). From Fig.1(b), it is known that the stable output signals of high level V_P-Φ_D and low level Φ_D are obtained.

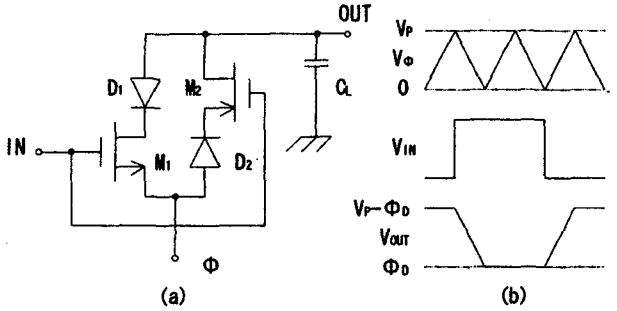

Fig.1. (a) The basic ADCL inverter circuit and (b) the relationship among V_Φ, V_{IN} and V_{OUT}.

Here, the adiabatic operation is carried out if the rising and falling edges of the output signal follow the supply voltage and do not change stepped. In order that such operation is

put on, it is important that the input signal voltage is made to rise in maximum value vicinity of the supply voltage, and again, that it is made to fall in the minimum value vicinity, as in Fig.1(b). Then, discharge and charge of load capacitor C_L would be done in the constant current, while potential difference between source and drain of the MOSFET (M_1 , M_2) is kept low. As the result, the energy thermally consumed at channel resistance of M_1 and M_2 is minimized. In actual circuit, diodes D_1 and D_2 in Fig.1(a) can be replaced by diode-connected MOS FET(MOS diode) for CMOS process compatibility. Thus, the actual ADCL inverter circuit as shown in Fig.2 is obtained. In this circuit, MOS diodes M_1 and M_2 are used. For another basic logic circuits, 2-input NAND circuit, 2-input NOR, XOR and other logic circuits using ADCL circuit technology can be easily constructed. Among such logic circuits, the 2-input NAND circuit is specially shown in Fig.3 for an example.

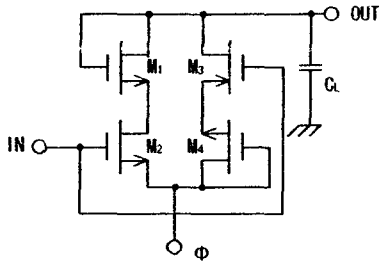

Fig.2. The actual ADCL inverter circuit.

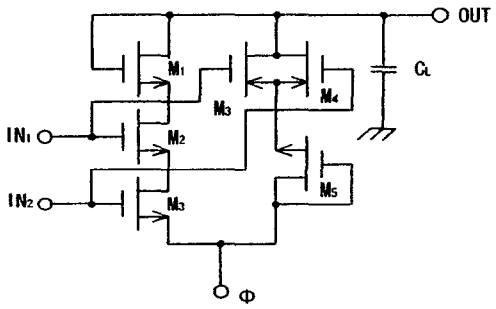

Fig.3. The 2-input NAND circuit by ADCL technology.

3. Expandable 4-bit Adder/Subtracter

3.1 Circuit Structure

The 4-bit adder / subtracter is easily realized using Full Adder (FA) and Exclusive OR (XOR), when the 2's complement is used. In Fig.4, the expandable 4-bit adder/subtracter circuit is shown. It is designed as a practical circuit. Therefore input and output buffers, and input and output registers by D type Flip-Flop (D-FF) are also equipped. FA, XOR and D-FF circuits used in the 4-bit adder/subtracter are composed with NAND and NOT circuits. These circuits are shown in Fig.5, Fig.6 and Fig.7, respectively.

3.2 Operation

In Fig.4, data A (a_1, a_2, a_3, a_4) and data B (b_1, b_2, b_3, b_4) are input to buffer circuit and stored by clock signal CLK in the input register which is composed of 8 D-FFs.

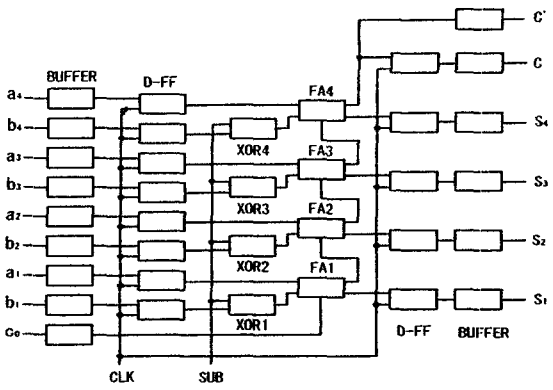

Fig.4. The expandable 4-bit adder/subtracter circuit.

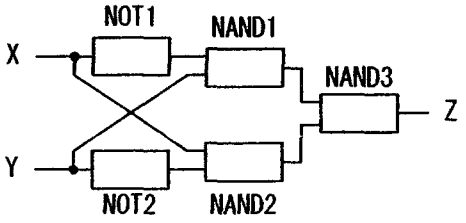

Fig.5. Full Adder (FA) circuit.

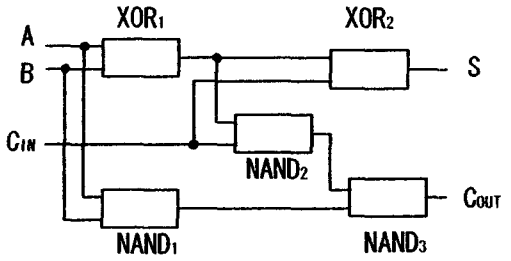

Fig.6. Exclusive OR (XOR) circuit.

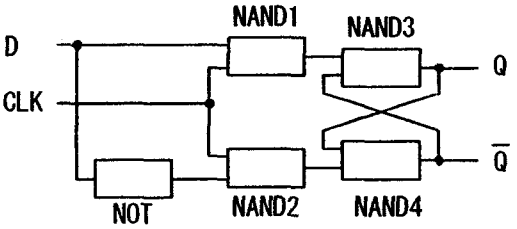

Fig.7. D type Flip-Flop circuit.

The data stored in the input register are operated in the XORs and FAs. Carry-in bit C_0 is directly fed to FA_1 circuit The resulted 4bit data plus one carry-out bit are output as S_1 S_2, S_3, S_4 and c through output register composed of 5 D-FF circuits and output buffer circuits. For expanding 4-bit addition and subtraction, extra carry bit C' is output without passing through output register and output buffer circuit.

In Fig.4, if SUB=0, then XOR circuit becomes only a buffer circuit and thus the addition as $a_i+b_i+C_0$ ($i = 1, 4$) is carried out. On the contrary, if SUB=1 and C_0=1 then the data b_i ($i =1,4$) are input in the form of the 2's complement since XOR gate operates as a inverter circuit, and the operation of subtraction a_i-b_i ($i =1,4$) is realized.

3. 3 Operation Speed

Output voltage V_{OUT} of the ADCL circuit delays at least by 0.5 periods of the source voltage V_Φ from the input voltage V_{IN}, because the rising and falling edges of V_{OUT} waveform synchronize with the source voltage V_Φ. Also in case of 2-input NAND and NOR circuit, the delay is 0.5 periods of V_Φ. Thus, the maximum delays of the circuits in Fig.5, Fig.6 and Fig.7 are as shown in Table.1.

Table. 1

Circuit	Signal Pass	Delay(periods)
FA	A, B to S	3.0
	A, B to C_{OUT}	2.5
XOR	X, Y to Z	1.5
D-FF	D to Q, $\bar{Q}$	1.5

From Table.1, the critical pass delay of the ADCL 4-bit adder/subtracter circuit in Fig.4 can be calculated as Eq.(1) using the period of source voltage V_Φ.

Critical Pass Delay = Delay [D-FF]+Delay [XOR_1]+Delay [FA_1 (A, B to C_{OUT})]+Delay [FA_2 (C_{IN} to C_{OUT})]+Delay[FA_3(C_{IN} to C_{OUT})]+Delay[FA_4(C_{IN} to S)]+Delay[D-FF].

=1.5+1.5+2.5+1+1+1.5+1.5 periods.

=10.5 periods. (1)

Here, time delays of input and output buffers are neglected, because the conventional CMOS circuit which works non-synchronously is used for them.

If the frequency of source voltage V_Φ is set at 10 MHz, then the latency time of the ADCL 4-bit adder/subtracter circuit can be calculated using Eq.(1) and becomes about 1.05 μ sec.

3.4 Energy Consumption

By the circuit simulation, energy consumption between 4 bit addition and subtracter using usual CMOS circuit and 4 bit addition and subtracter using the ADCL circuit was compared. The program used for simulation is PSPICE. The simulation result is as follows:

(1) In case of addition operation at the supply voltage frequency of 10MHz, consumed energy is 919.56 pJ/operation for conventional CMOS and 93.67pJ/operation for ADCL circuit.

(2) In case of subtraction operation at the supply voltage frequency of 10MHz, consumed energy is 1010 pJ/operation for conventional CMOS and 118.67pJ/operation for ADCL circuit.

From above comparison, it is known that energy consumtion in ADCL 4-bit adder/subtracter is 90% less than that in conventional CMOS 4-bit adder/subtracter.

4. Fabrication and Evaluation of the IC

The ADCL 4-bit adder/subtracter IC was fabricated using a standard 1.2 μ CMOS process. The fabricated IC chip includes several TEG circuits also. The microphotograph of the chip is shown in Fig.8. The chip size is 2.3mm×2.3mm. In order to evaluate the fabricated IC, several experiments were carried out. Measurement conditions for experiments are as follows:

- DC supply voltage (V_{DD})for substrate biasing : 5V.
- Sinusoidal voltage (V_Φ) for power supply : Maximum (V_P) and minimum values are 5V and 0, respectively. Frequency is 10MHz.
- Rectangular pulse voltage for input (V_{IN}) : $5V_{P\text{-}P}$.
- For interfaces of input and output, buffer circuits by conventional CMOS are employed.

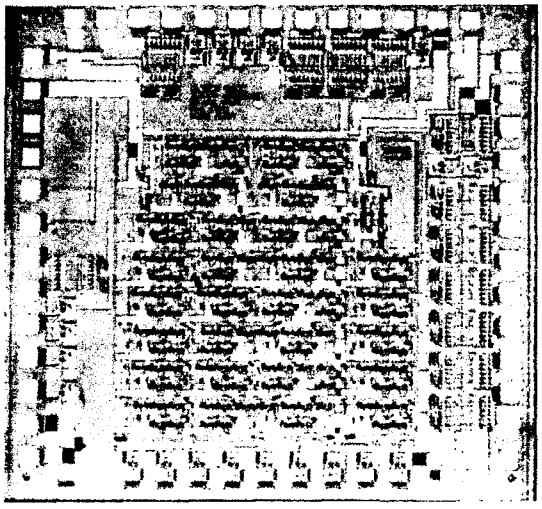

Fig.8. Expandable 4-bit adder/subtracter IC chip using the ADCL circuit technology.

5. ADCL 4-bit Adder/Subtracter Circuit

In order to evaluate the ADCL 4-bit adder/subtracter IC, experiments on addition, subtraction and addition for C' which is the carry-out bit terminal for extending function were carried out.

5.1 Addition Operation

For testing the addition operation of the IC, the input data pattern a_n and b_n are set as follows:

Operation (SUB=0, C_0=0)

	a_4	a_3	a_2	a_1	+	b_4	b_3	b_2	b_1	C_0
	1	1	1	1		0	0	0	0	0
										1
=	C'	C	S_4	S_3	S_2	S_1				
	0	0	1	1	1	1				
	1	1	0	0	0	0				

Here, b_1 is changed from '0' to '1' surrounded in the dotted line. Then the output data (C' C S_4 S_3 S_2 S_1) are changed from (0 0 1 1 1 1) to (1 1 0 0 0 0). In Fig.9, waveforms of input and output voltage related to b_1 and C'are shown. From Fig.9, it is also known that the signal delay from the lowest significant bit (LSB) b1 of the input to C' is 6 periods of V_Φ in the rising edge and 7 periods of V_Φ in the falling edge of the rectangular pulse input signal.

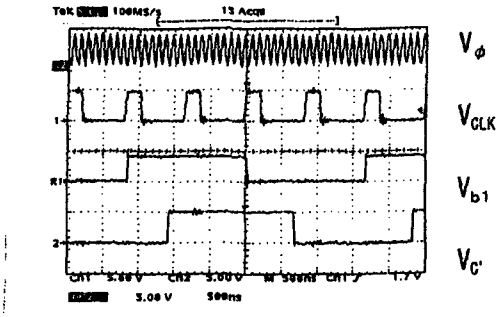

Fig.9. Waveforms of input and output voltage related to b1 and C'(for addition).

5.2 Subtraction Operation

For testing the addition operation of the IC, the input data pattern a_n and b_n are set as follows:

Operation (SUB=1, C_0=1)

Subtraction operation is executed using the 2's complement method.

$a_4\ a_3\ a_2\ a_1\ -\ b_4\ b_3\ b_2\ b_1\ C_0$

1 1 1 0 1 1 1 1 1

1

$= C'\ C\ S_4\ S_3\ S_2\ S_1$

0 0 1 1 1 1

1 1 0 0 0 0

Here, a_1 is changed from '0' to '1' surrounded in the dotted line. Then the output data (C' C S_4 S_3 S_2 S_1) are changed from (0 0 1 1 1 1) to (1 1 0 0 0 0). In Fig.10, waveforms of input and output voltage related to a_1 and C'are shown. From Fig.10, steady subtraction operation is confirmed. In the subtraction operation, the output signal at C'delays 7 periods of V_ϕ from the input, both in the rising and falling edges of pulse voltage. Thus, like the case of addition, the clock pulse interval must be longer than the delay time of 7 periods of V_ϕ for latching the data steadly.

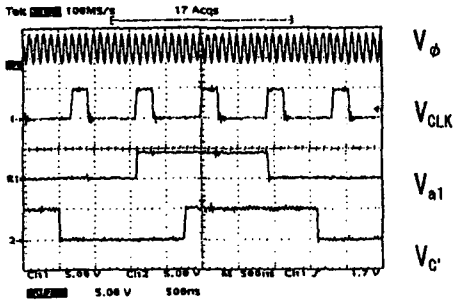

Fig.10. Waveforms of input and output voltage related to a_1 and C'(for subtraction).

6. Charge Recovery Power Supply Circuit

In order to supply the power to the expandable 4-bit adder /subtracter circuit, sinusoidal voltage source is used in this case.The Clapp oscillator circuit is used to generate the sinusoidal voltage. The oscillator circuit is shown in Fig.11. The circuit is constructed using discreet components. In the circuit, the normally-on transistor is used. Therefore, DC power source voltage is reduced until effectively low. This time, the oscillator has operated with lower supply voltage

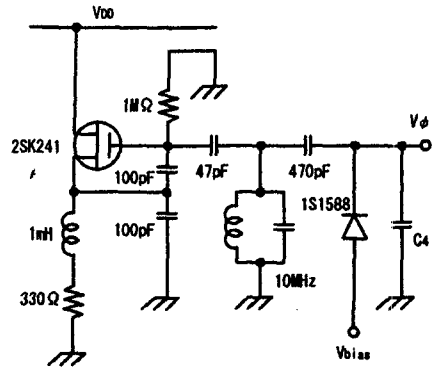

Fig.11. Clapp oscillator circuit for supplying the power to the ADCL expandable 4-bitadder/subtracter circuit.

than one volt DC. The current to the circuit was set by adjusting the value of source resistance (shown as 330Ω in the circuit), in order to generate the sinusoidal voltage of 5Vp-p at the output terminal (V_ϕ). Frequency of the oscillated sinusoidal voltage was controlled to be near 10MHz by LC value.

The oscillator circuit was connected to the ADCL expandable 4-bit adder/subtracter circuit for supplying the power and thus, the ADCL system was constructed. The ADCL system was experimentally confirmed to operate perfectly. Dependency of the ADCL system power dissipation on the DC supply voltage is shown in Fig.12. From the figure, it is known that the system can operate under sub-one volt DC power supply and shows the minimum power dissipation of 0.95 mW at the supply voltage of 1.3V DC.

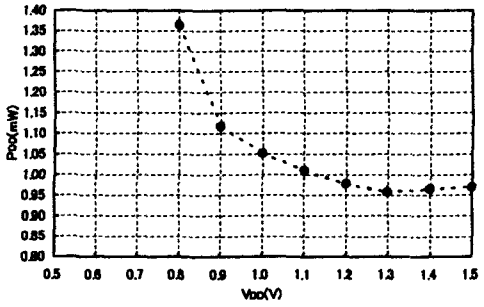

Fig.12. Dependency of the ADCL system power dissipation the DC supply voltage.

7. Conclusion

In conclusion, it is known that by using the Clapp oscillator circuit which uses normally-on transistor as a active device to generate sinusoidal voltage for ADCL logic circuit, external DC power supply voltage can be reduced to sub-one volt. It means that a 1.5 volt single battery can be used for ADCL system. From the viewpoint of very low power dissipation and low level supply voltage, it is also known that ADCL circuit is hopeful in the field of portable electronic system or very large system such as super array computer.

Reference

[1] K. Takahashi, M. Mizunuma, "Adiabatic Dynamic CMOS Logic circuit", IEICE Trans.C-II, vol.J81-C-II, pp.810-817,Oct.1998 (in Japanese).