The Design of Error Detection Auto Correction for Conversion of Graphics to DTV Signal

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Abstract: In the integrated systems, that is integrated digital TV(DTV) internet and home automation, like home server, is needed integration of digital TV video signal and computer graphic signal. The graphic signal is operating at the high speed and has time-divide-stream. So the re-request of data is not easy at the time of error detection. therefore EDAC algorithm is efficient.

This paper presents the efficiency error detection auto . correction(EDAC) for conversion of graphics signal to DTV video signal. A presented EDAC algorithms use the modified Hamming code for enhancing video quality and reliability. A EDAC algorithm of this paper can detect single error, double error, triple error and more error for preventing from incorrect correction. And it is not necessary an additional memory. In this paper The comparison between digital TV video signal and graphic signal, a EDAC algorithm and a design of conversion graphic signal to DTV signal with EDAC function is described.

1. Introduction

In times past, the systems such as home automation and home multimedia served their services separately.[1]
But at the present time, the services are trending toward integrating system. Because of the internet was spreaded among the public rapidly, and the high speed internet networks. So In the integrated systems, that is integrated digital TV internet and home automation, like home server, is needed integration of digital TV video signal and computer graphic signal. The graphic signal is operating at the high speed and has time-divide-stream. So the re-request of data is not easy at the time of error detection. therefore EDAC algorithm is efficient.

In this paper the efficiency error detection auto correction presented for conversion of graphics signal to DTV video signal. A presented EDAC algorithms use the modified Hamming code for enhancing video quality and reliability. A EDAC algorithm of this paper can detect single error, double error, triple error and more error for preventing from incorrect correction. And It use 32bits, data 24bits and 8 parity bits, for EDAC in general 32bits width memory. So it is not necessary an additional memory.

The comparison between digital TV video signal and graphic signal is described in chapter2. A EDAC algorithm using modified Hamming code is described in chapter 3. A design of conversion graphic signal to DTV signal with EDAC function is described in chapter 4. It is designed using HDL for FPGA.

2. Graphics/DTV Signals

In general there are the difference between graphic signal and DTV video signal such as aspect ratio, scan mode, frame rate and data format. The comparison is as follows.

1) Digital TV Output Format
- Aspect ratio: 16:9
- Scan mode: Interlace(1920*1080I)
  Progressive(1280*720P)
- Frame Rate: 30Hz (SMPTE274M:1080I),
  60Hz(SMPTE296M:720P) 74.25Mhz
- Data Fromat: Y Pb Pr, Tri state sync

2)Graphic Data Output Format
- Aspect ratio: 4:3
- Scan mode: Progressive
  (SVGA 800*600, XGA 1024*768)
- Frame Rate: 60Hz(SVGA:40Mhz, XGA:65Mhz)
- Data Fromat: R G B and VHSync(2)

A color in the RGB color space is converted to the

YPbPr color space using the following equation(1) and (2).

$$\begin{bmatrix} Y \\ Pb \\ \Pr \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.168 & -0.331 & 0.5 \\ 0.5 & -0.418 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad (1)$$

$$Y = 0.299R + 0.587G + 0.114B \quad (2)$$
$$Pb = 0.71327(R - Y)$$
$$\Pr = 0.56433(B - Y)$$

This paper intend to conversion graphic data to DTV signal.

3. EDAC Algorithm for Graphics to DTV Signal

A EDAC algorithm using modified Hamming code and conversion module are described in this chapter.

In general a mechanism of error detection and correction between signal processor and memory module is needed for reliability.

The video and graphic signal are operating at the high speed and has time-divide-stream. So the re-request of data is not easy at the time of error detection. therefore auto correction algorithm is efficient. A error detection can correct single error using general Hamming code[2]. But In the case doble error, triple error, or more error, it incorrectly correct by Hamming code.

This EDAC algorithm can detect single error, double error, triple error and more error for preventing from incorrect correction. Furthermore that use 8 bits except for data 24bits among 32bits memory bank width. So not needed to attach additional memory.

A modified hamming code for enhanced image quality consists of video data 24 bits, parity 5bits and error information 3 bits.

The relation k and P for error detection auto correction can be written as[3]

$$P \le 2^k - 1 - k \quad (3)$$

k: parity check bit

P: protect P bit

where k is 5, P is 24, and error information bit N is 3. The position and error information of N bits are described in table 1- table 3.

A conversion block module of digital TV/graphic signal with EDAC for enhanced quality is shown in Fig 1.

This consist of input module from graphic signal, EDAC coding module, interpolation module, signal format converter, address generator, and digital TV sync generation module, etc.

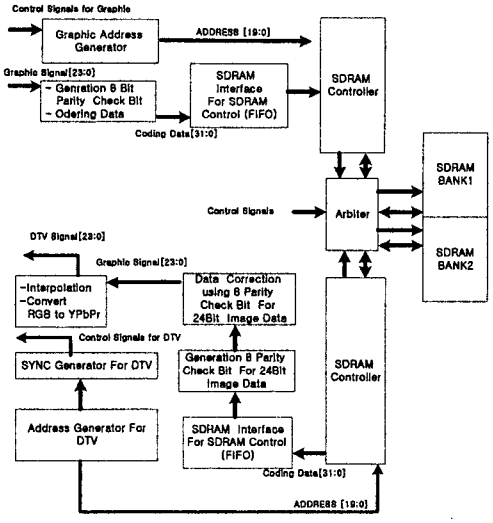


Fig. 1. Block diagram of conversion graphics to DTV with EDAC.

A Input data 24 bits from graphic is converted to 32 bits by EDAC, and stored in memory then a data from memory is processed to 24 bits data by EDAC then it is changed digital TV signals.

For input data aquisition of graphic signal, the digital graphic output from graphic chip for DVI interface is connected with input module of Fig 1. A output module for a converted digital TV signal is connected digital/analogue converter with tri-state.

A converted digital TV signal and digital TV signal from DTV decode chip are multiplexed in the case of application like a DTV settop.

The parity bits(P0-P4), parity value and error bit are shown in table 1.

Table. 1. Configuration of 24bit data and 8bit parity as modified EDAC for 32bit memory bank

Error bit	P0	P1	P2	P3	P4	Parity Value #(S3-S0)
0	1	1	0	0	0	3
1	1	0	1	0	0	5
2	0	1	1	0	0	6
3	1	1	1	0	0	7
4	1	0	0	1	0	9
5	0	1	0	1	0	10
6	1	1	0	1	0	11
7	0	0	1	1	0	12
8	1	0	1	1	0	13
9	0	1	1	1	0	14
10	1	1	1	1	0	15
11	1	0	0	0	1	17
12	0	1	0	0	1	18
13	1	1	0	0	1	19
14	0	0	1	0	1	20
15	1	0	1	0	1	21

Error Bit	P0	P1	P2	P3	P4	Parity Value
16	0	1	1	0	1	22
17	1	1	1	0	1	23
18	0	0	0	1	1	24
19	1	0	0	1	1	25
20	0	1	0	1	1	26
21	1	1	0	1	1	27
22	0	0	1	1	1	28
23	1	0	1	1	1	29
P0	1	0	0	0	0	1
P1	0	1	0	0	0	2
P2	0	0	1	0	0	4
P3	0	0	0	1	0	8
P4	0	0	0	0	1	16
No Error	0	0	0	0	0	0

Table. 2. Position of 24bit data and 8bit parity as modified EDAC for 32bit memory bank

Bit Position	Data /Parity	Parity Value	Bit Position	Data /Parity	Parity Value
0	P0	1	16	D11/G3	17
1	P1	2	17	D12/G4	18
2	D0/B0	3	18	D13/G5	19
3	P2	4	19	D14/G6	20
4	D1/B1	5	20	D15/G7	21
5	D2/B2	6	21	D16/R0	22
6	D3/B3	7	22	D17/R1	23
7	P3	8	23	D18/R2	24
8	D4/B4	9	24	D19/R3	25
9	D5/B5	10	25	D20/R4	26
10	D6/B6	11	26	D21/R5	27
11	D7/B7	12	27	D22/G6	228
12	D8/G0	13	28	D23/R7	29
13	D9/G1	14	29	N0	30
14	D10/G2	15	30	N1	31
15	P4/16	16	31	N2	32

The position of N0-N2, parity bits(P0-P4), and data bits(D0-D23) are shown in table2.

Where R0-R7 are red bits, G0-G7 are green bits, B0-B7 are blue bits. The parity 5 bits(P0-P4) for EDAC are generated as follows.

P0 = XOR of data bit
(0, 1, 3, 4, 6, 8, 10, 11, 13, 15, 17, 19, 21, 23)
P1 = XOR of data bit
(0, 2, 3, 5, 6, 9, 10, 12, 13, 16, 17, 20, 21)
P2 = XOR of data bit
(1, 2, 3, 7, 8, 9, 10, 14, 15, 16, 17, 22, 23)
P3 = XOR of data bit
(4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23)
P4 = XOR of data bit
(11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23)

And a additional 3 parity bits(N0-N2) are used for preventing from correction incorrectly in the case of doble error and triple error and more error. N0-N2 are generated as follows.

N0 = XOR of data bit
(R7, R6, G7, G6, B7, B6)
N1 = XOR of data bit
(R5, R4, R3, G5, G4, G3, B5, B4, B3)
N2 = XOR of data bit
(R2, R1, R0, G2, G1, G0, B2, B1, B0, P4, P3, P2, P1, P0)

The parity bits P0 is parity for writing input image data. and P0' is parity for reading input image data. P1, P2, P3 and P4 are the same. The parity value(S3-S0) is calculated by S0=XOR(P0, P0'), S1=XOR(P1, P1'), S2=XOR(P2, P2'), S3=XOR(P3, P3'), S4=XOR(P4, P4'). The error can be corrected by parity value. The parity values(SS2-SS0) for error information are the same. SS0=XOR(N0, N0'), SS1=XOR(N1, N1'), SS2=XOR(N2, N2'). The even error and odd error can be detected by using additional only one bit. But if three bits(N0-N2) are used, an even error, odd error, 3 bits error, 5 bits error and more error can be detected. The high bits of graphic data has high affects at image, so N0 has high resolution. The error type(error information) with respect to N0-N2 are shown in Table 3.

Table. 3. Error Information with respect to N0-N2

Parity Value	SS2	SS1	SS0	Error Inform
0	0	0	0	No Error
Not 0	0	0	0	Not Single error
Not 0	0	0	1	Single error : Correctable
Not 0	0	1	0	Single error : Correctable
Not 0	0	1	1	Not Single error (2,...)
Not 0	1	0	0	Single error : Correctable
Not 0	1	0	1	Not Single error (2,...)
Not 0	1	1	0	Not Single error (2,...)
Not 0	1	1	1	Not Single error (3,...)
0	0	0	1	N0 error : Correctable
0	0	1	0	N1 error : Correctable
0	0	1	1	N1, N0 error : Correctable
0	1	0	0	N2 error : Correctable
0	1	0	1	N2, N0 error : Correctable
0	1	1	0	N2, N1 error : Correctable
0	1	1	1	N2, N1, N0 error : Correctable

4. Design of Signal Converter with EDAC

The design of signal converter with EDAC function for enhanced reliability is described in this chapter. The module is designed by using HLD. The designed signal converter module for FPGA is shown in Fig 2.

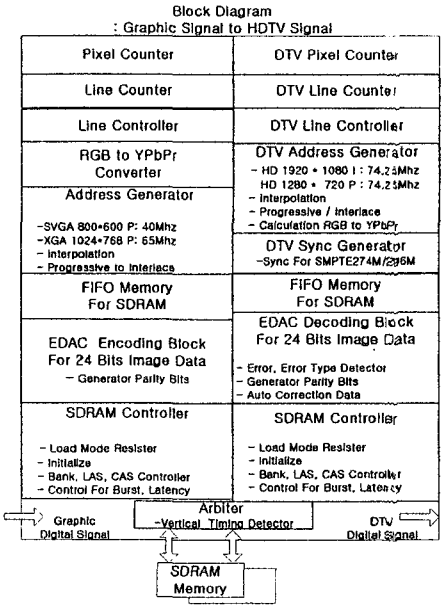
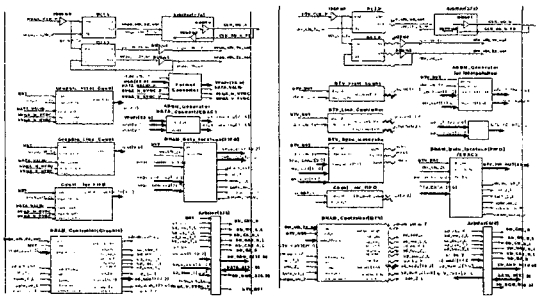
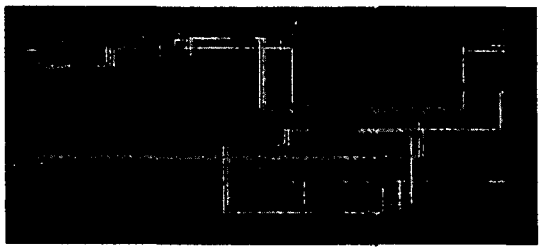


Fig. 2. Block module for conversion graphics to DTV with EDAC.

A design of graphic input part with EDAC is shown in Fig 3(a), and a design of digital TV output part with EDAC function is shown in Fig 3(b). The synthesis Schematic of top level is shown in Fig3(c). In Fig 4, the waveform of top level is shown.



(a) (b)



(c)

Fig. 3.(a) Block diagram of graphics signal part.
(b) Block diagram of DTV signal part
(c) The synthesis Schematic of top level

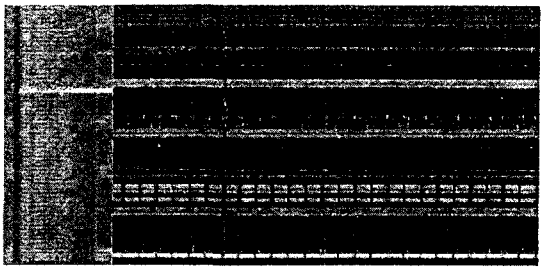


Fig. 4. Top level wave of conversion graphics to DTV with EDAC.

5. Conclusion

At the present time, the services are trending toward integrating system. In the integrated systems, that is integrated digital TV internet and home automation, like home server, is needed integration of digital TV video signal and computer graphic signal. The graphic signal is operating at the high speed so the re-request of data is not easy at the time of error detection. therefore EDAC algorithm is efficient. In this paper presents a EDAC for conversion of graphics signal to DTV video signal. A presented EDAC algorithms use the modified Hamming code for enhancing video quality and reliability. A EDAC algorithm of this paper can detect single error, double error, triple error and more error for preventing from incorrect correction. It is not necessary an additional memory. In this paper The comparison between digital TV video signal and graphic signal is described and a algorithm using modified Hamming code is described and a design of conversion graphic signal

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