Ultra CSP
(Wafer Level Packaging)

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Ultra CSP

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- Process Overview
- Process Characterization
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- Design Rule
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- Capacity & Cycle Time
- Competitive Advantage
- Summary

Introduction

- What is Ultra CSP?

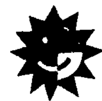
- **Wafer-level Packaging**

Wafer-level packaging has sets of area array bonding pads on the wafer or forms the sets of area array bonding pads by means of redistribution of the peripheral bonding pads of each die in the wafer fabrication process. Moreover, the interconnect medium on the pad is built via various ways to enable direct chip attach.

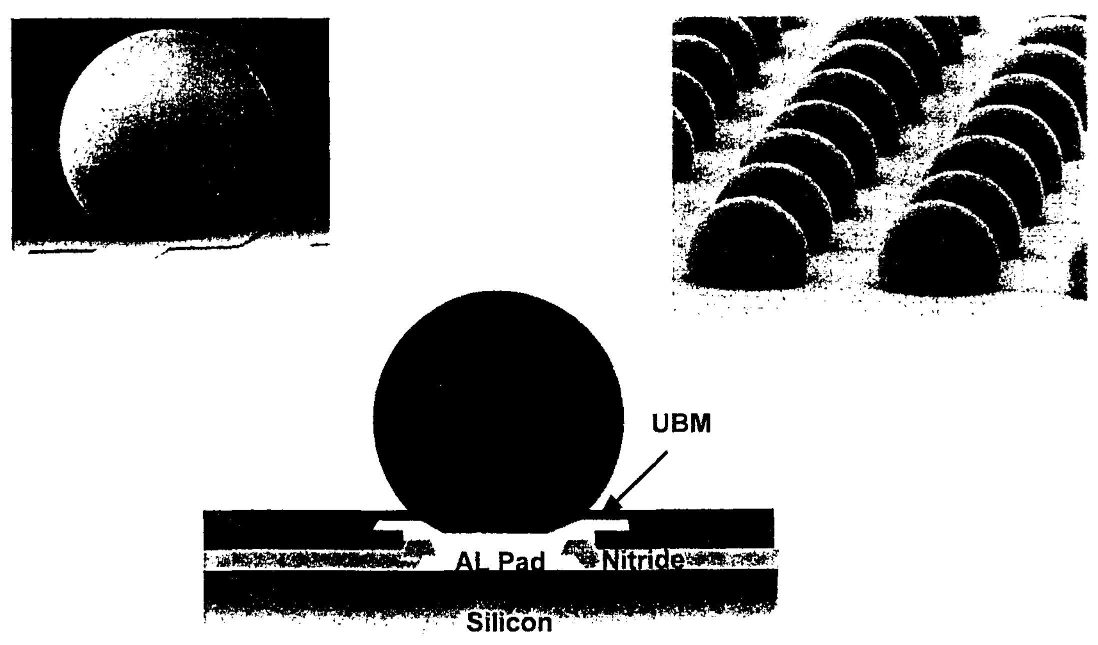
- **Ultra CSP**

Ultra CSP is one of wafer-level packaging, which allow direct ball drop process in wafer form to establish its interconnection medium for direct board assembly. It is a patented process by *Flip Chip Technologies*.

Introduction

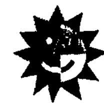


- Illustration of Ultra CSP



Introduction

- Features



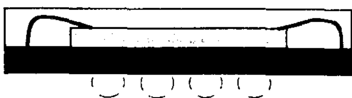
- Real chip size (smallest, thinnest and lightest)
- High density interconnection
- High-speed data processing
- Batch process- assembly processed in wafer form (cost competitive, even better for 12 inch wafer)
- Limitation of higher pin-count
- Lack of package standardization

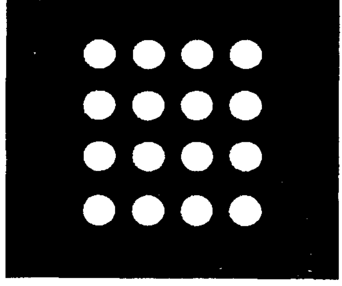
Ideal package for low pin-count application!

Introduction

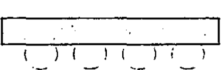
- Ultra CSP v.s. WB CSP

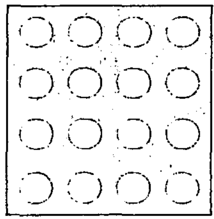
WB CSP





Ultra CSP ™





"Package size" & "Electrical path" shrink.

Introduction

- Ultra CSP v.s. Flip Chip CSP

Flip Chip (solder bumps)		Ultra CSP ™ (solder balls)
4 ~ 3600	I/O count	4 ~ 100
>150 μm	Min. I/O pitch	0.5 mm
100 μm typical	Solder diameter	300-500 μm
100 μm typical	Solder Height	220 ~ 400 μm
High accuracy	SMT Equipment	Standard
0.4 ~ 0.75 mm	Package Height	0.6 ~ 1.1 mm
Yes	Underfill	No

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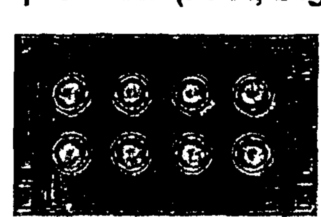
Introduction

- Applications

- Application
  - Memory (EEPROM, Flash, DRAM & SRAM)
  - Integrated Passives
  - Analog Device (RF)
  - Digital Signal Processor (DSP)
  - Power & Voltage Regulator
  - Power Amplifier
- Products
  - Cell phone
  - Portable consumer products (PDA, Digital camera...)
  - System boards

Casio Camera Watch



Atmel EEPROM

Photos provided by Pristmark

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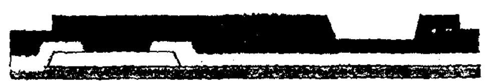
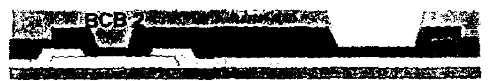
Process Overview

- Process Flow

Apply first-layer polymer onto wafer



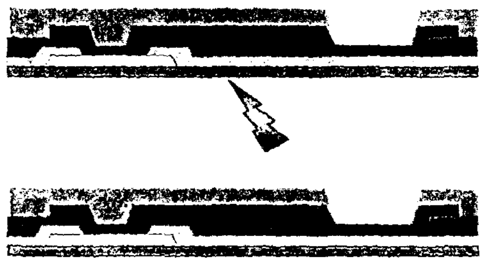
Sputter UBM and form trace and pad



Apply second-layer polymer onto wafer

Process Overview

- Process Flow (Cont'd)



Backside Grinding

Backside Laser Marking

Solder Ball Attach

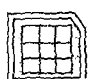
Reflow

Cleaning

Wafer Mount

Wafer Saw (Singulation)

or



Pick & Place

FVI

Packing (Tape & Reel / Waffle pack
Wafer box)

Process Characterization

- Process Capability and Limitation

• Redistribution	Standard pitch 50um (Line/Space=38/12um) Fine Pitch 37um (Line/Space=25/12um)
• Laser Marking	0.3mm (Font Height) x 0.2mm (Font Pitch)
• Wafer Grinding	12mil min.
• Ball Mounting	Sn/Pb=63/37 0.3 / 0.5mm Ball Pitch
• Wafer Sawing	80um min. Scribe Line
• Packing	0.5x0.5mm min. for Waffle Pack 1.0x1.0mm min. for Tape and Reel

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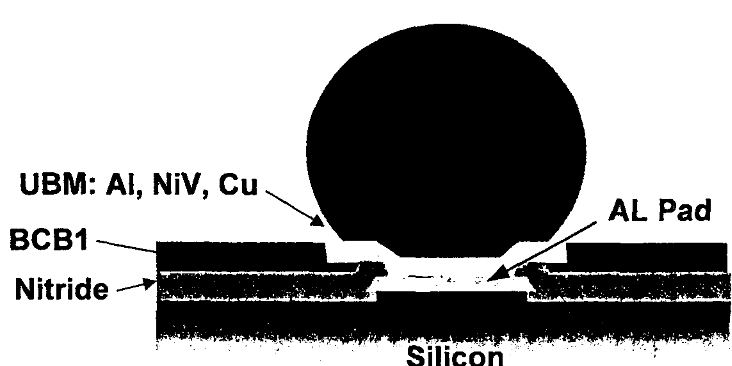
Package Menu

- Structure 1: Re-passivation



Note:
1. Not in scale
2. Nitride 1um, UBM 2um, BCB 3um
3. BCB: Benzocyclobutene
4. BCB: dielectric, planarizing & stress buffer

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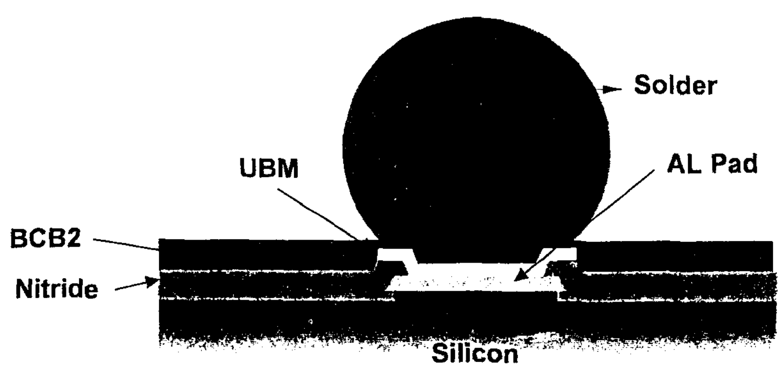
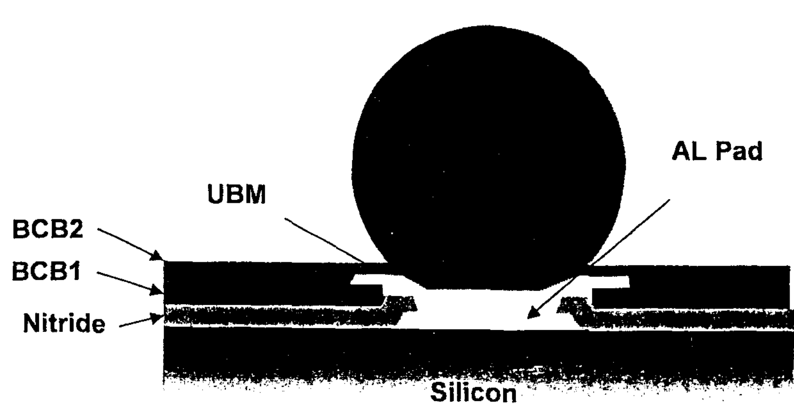
Package Menu

- Structure 2: One-layer BCB



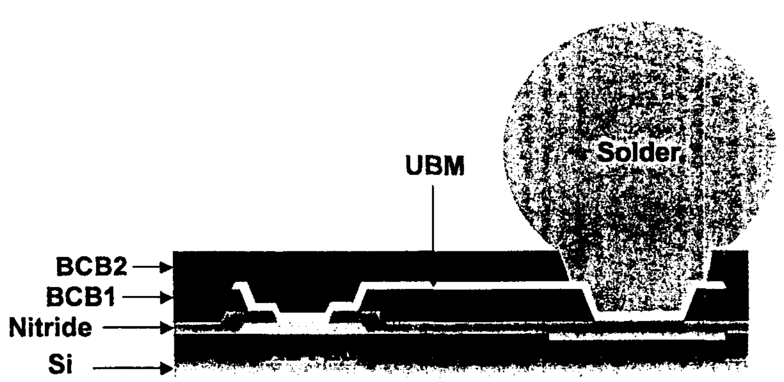
Package Menu

- Structure 3: Two-layer BCB



Package Menu

-Structure 4: Redistribution



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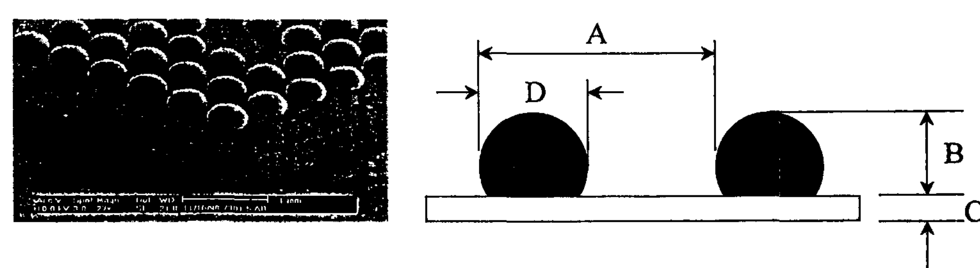
Package Menu

- Critical Geometric Dimensions



Pitch (mm)	Ball Size (mm)	Ball Height (mm)	Die Thick. (mm)	Ball Diameter (mm)
A		**B**	**C**	**D**
0.50	0.30	0.22	0.33 ~ 0.73	0.32
0.50	0.35	0.28	0.33 ~ 0.73	0.38
0.65	0.35	0.28	0.33 ~ 0.73	0.38
0.75	0.50	0.38	0.33 ~ 0.73	0.54
0.80	0.50	0.38	0.33 ~ 0.73	0.54

*Total Height: 0.6~1.1mm

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Package Menu

- Experience (Processed Devices)

Wafer size (inch)	6 ~ 8
Die size (mm)	1.45x1.45 ~ 6.9x6.45
Ball pitch (mm)	0.5, 0.75 and 0.8
Ball size (mm)	0.3 and 0.5
Ball count	8~ 98

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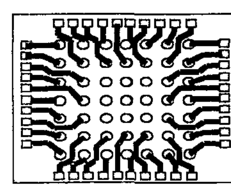
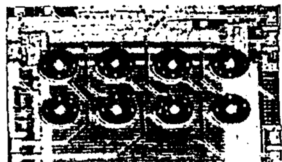
Design Rule

- Basic Wafer Request

- **Passivation type** Nitride or Oxynitride, but not Polyimide.
- **Scribe Line Width** BCB inside die passivation step is preferable.
  (Min. scribe line for die saw ability is 80 um)
- **Inking** No inked wafer is required
- **Min. thickness** 6 inches wafer : 18~40 mils
  8 inches wafer : 22~40 mils





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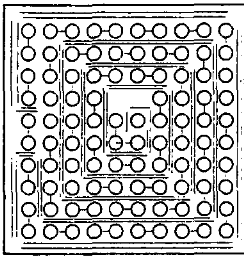
Qualification Plan

- Test Vehicles

***Ultra* CSP™ 50**

0.50 mm pitch
0.30 mm ball
10 x 10 array
Die Size : 6.9x6.45mm
Max. DMP = 3.18
No. I/O = 98



***Ultra* CSP™ 80**

0.80 mm pitch
0.50 mm ball
7 x 15 array
Die Size : 13.0x6.50mm
Max. DMP = 6.10
No. I/O = 90

Qualification Plan

- Package Level Tests

Tests Methods	S.S.	Test Conditions	
MSL test			
- MSL 1	270	85 ℃ /85%RH/168hrs + IRx3 (240'C)	
- MSL 2	270	85 ℃ /60%RH /168hrs+ IRx3 (240'C)	
- MSL 3	270	30 ℃ /60%RH /192hrs+ IRx3 (240'C)	
Reliability test			
- TCT	45	-55 ~ 125 ℃	1000 cycles
- HAST	45	130℃ /85%RH /33.6 psia	100 hrs
- THT	45	85 ℃ /85%RH	1000 hrs
- HTST	45	150 ℃	1000 hrs

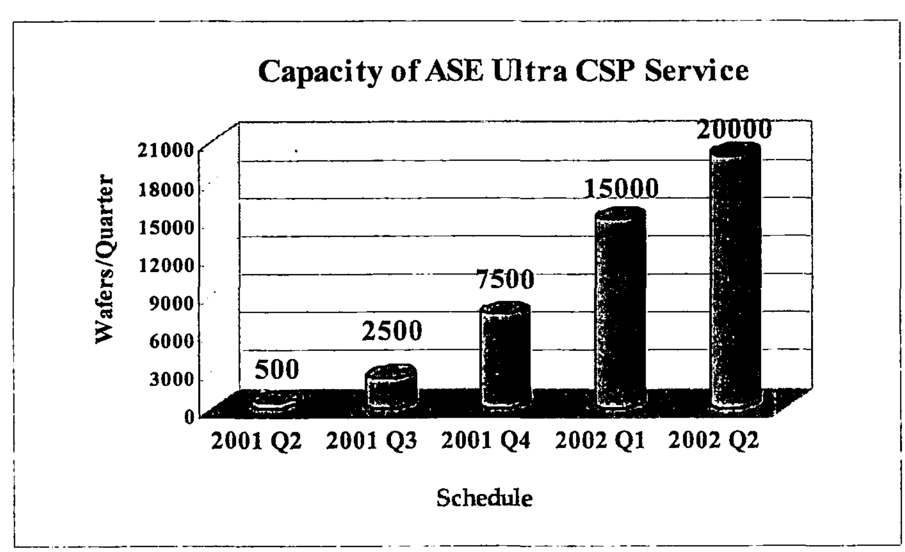
Qualification Plan

- Board Level Tests

Tests Methods	S.S.	Test Conditions	
1. TCT	32	-40 ℃ ~ 125 ℃	1000 cycles
2. Bending Test	10	1 mm deflection @ 1Hz	
3. Drop Test	10	1 meter height	

Capacity & Cycle Time

- Capacity



Note: Combined capacity of 6" and 8" wafers based on 3K dice/ Wafer

Capacity & Cycle Time

- Cycle Time

	Mask		Ball Mount Tool		Process	
			Auto	Manual		
	Design	MFG	Design+MFG	Design+MFG	1st Si	Productior
Bumping	2	5	NA	NA	10	6
REP (1 BCB)	3	5	NA	NA	12	7
RDL (2 BCB)	15	5	NA	NA	15	8
UCSP (1 BCB)	3	5	25	7	15	9
UCSP (2 BCB)	15	5	25	7	17	10

Units: working day

Roadmap

- Ultra CSP Technology Roadmap

Eutectic solder ball — **Ready**

Lead-free solder ball — **Mar. '02**

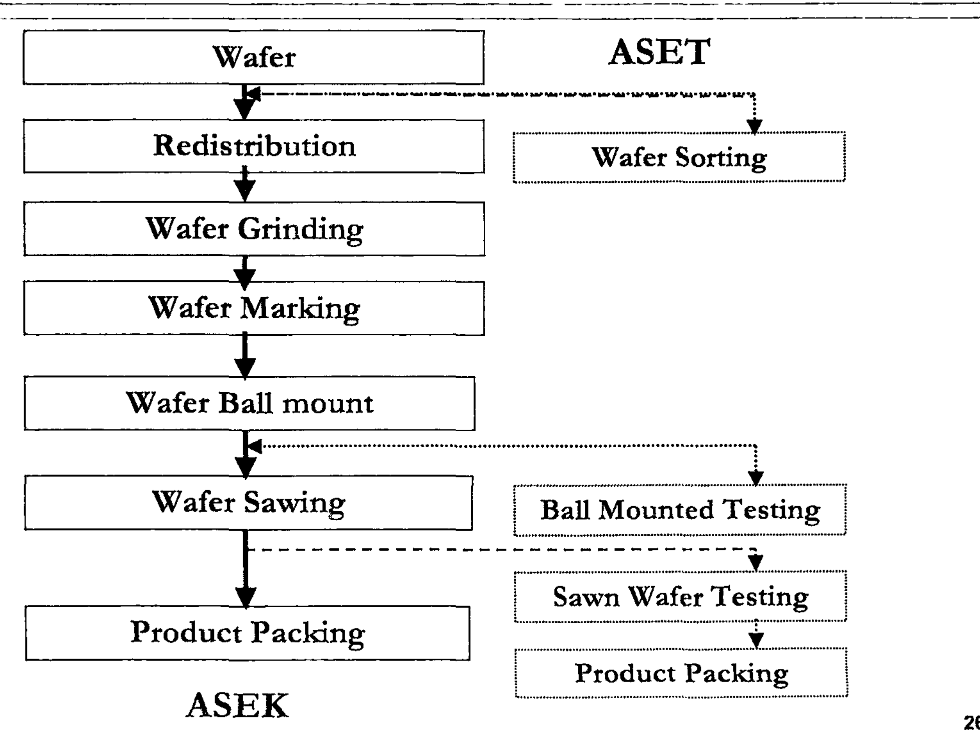
Milestone

- Ultra CSP Readiness

• Project master plan	Finished
• Machine survey and delivery	Finished
• Prototype	Ready
• Internal qualification	Finished
• Pre-production	Q4 2001

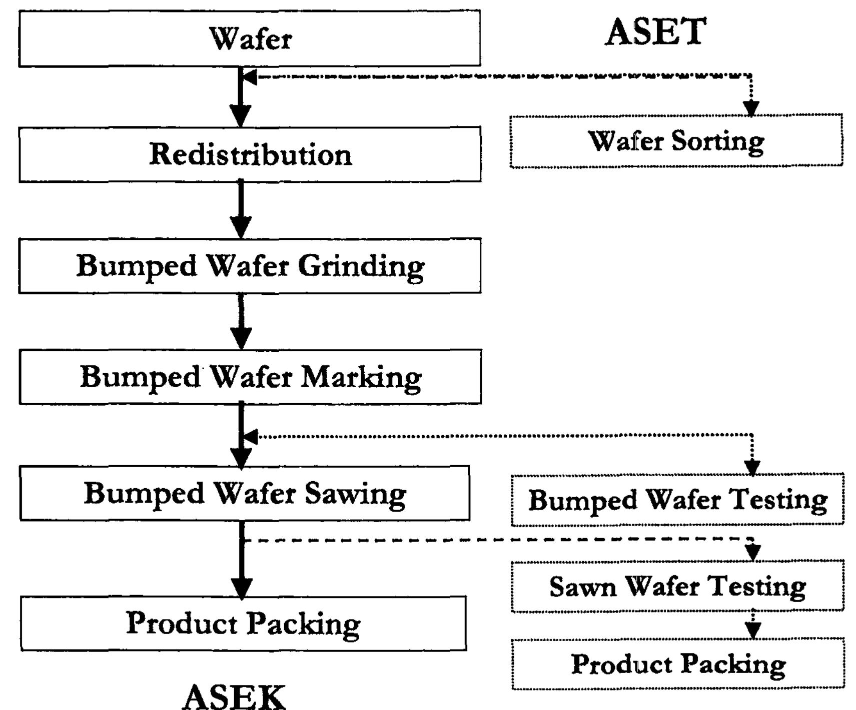
Competitive Advantage

- ASE edge: Total Solution for Ultra CSP



Competitive Advantage

- ASE edge: Total Solution for WLCSP



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Summary

- Ideal package solution for low pin-count devices. Success has been found in memory and integrated passive devices.
- The application is being extended to power and RF module and DSP.
- The combined service of wafer BCB re-passivation process and backend assembly process in ASE, make it more reliable in the aspects of both quality and time-to-market. The said service is available for both 6" and 8" wafers.
- Moreover, ASE provides a total turn-key solution which includes wafer sorting, re-passivation, backend assembly and final test.
- However, the service can be flexible and limited to backend only, including backside grinding, marking, singulation and pick & place.