Solder Bumping Technology using Ti-W/ Cu Structure

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Introduction
1. What is Flip Chip?

1. Flip Chip is an interconnection technology, not a specific package type.

2. Flip Chip is defined as mounting the chip to a substrate with any kind of materials and methods, as long as the chip surface(active area) is facing to the substrate.

3. Flip Chip Type
: FCIP(Flip chip in package), FCOB(Flip chip on board), FCCSP(Flip chip CSP)

4. Why Flip Chip is important in technology?
: Flip Chip is more than an assembly flow, it's a "technology" with impact in both development and production

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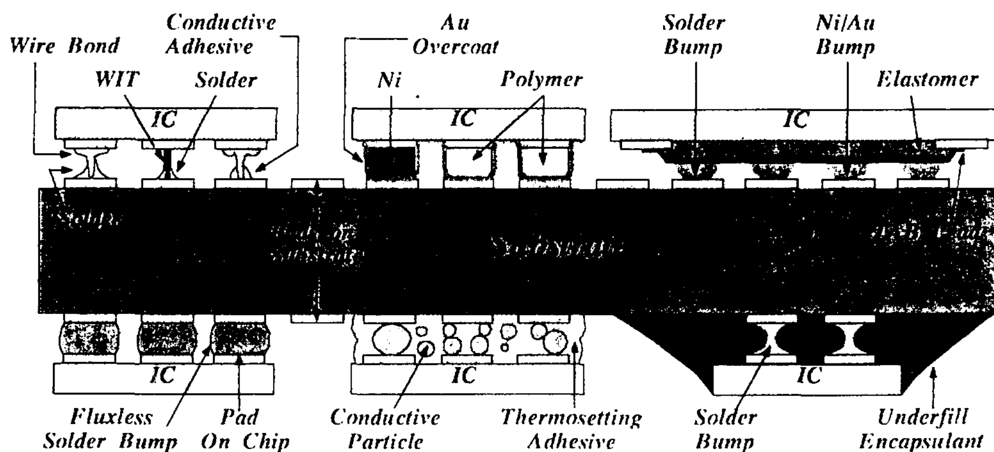
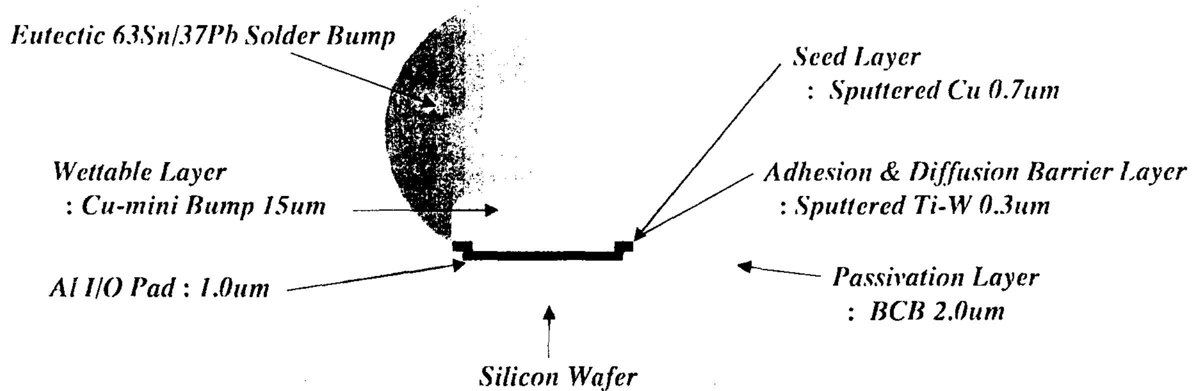
2. Various Flip Chip Technologies



3. Schematic of Cu-mini Bump and Solder Bump



4. UBM(Under Bump Metallurgy)

- *Good adhesion to the wafer passivation*
- *Good adhesion to the IC final metal pad*
- *Protection of the IC final metal from the enviroment*
- *Low resistance between IC final metal and solder bump*
- *An effective solder diffusion barrier*
- *A solder wettable metal of appropriate thickness*
- *Ability to be used on probed wafer*

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5. Ti-W/ Cu UBM

- *Less expensive than evaporation method*
- *Good adhesion to the IC final metal pad as well as passivation*
- *Low electrical resistance between IC final metal and solder bump*
- *Compatibility with Au bumping(Ti-W/ Au UBM) process*
- *A characteristic of diffusion barrier : Ti-W > Ti > Cr*

Barrier Metal	Heating Condition	Result
Ti-W	350 ℃ - 6hr	-
Ti	350 ℃ - 6hr	Occurrence of oxide-segregation
Cr	250 ℃ - 4hr	High electrical resistance

- *Good wettability : Cu > Ni*

Rating of the Wettability of Various Base Materials

Good	Fair	Moderate	Difficult	Practically Impossible
Au, Sn-Pb, Sn, Ag, Pd, Cu	Cu-Sn, Cu-Zn, Cu-Ni, Ni-Ag	Alloy42, Ni-Fe, Ni	Al-Cu-Sn, Al	Cr, W, Ti, Mo, Mg

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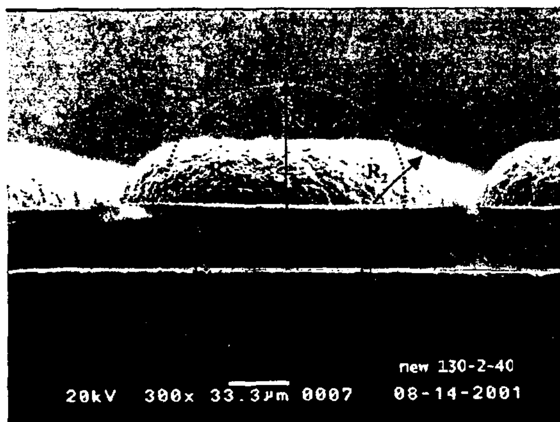
Solder Bump Design Rule

1. Formulae



As Plated (Mushroom)

$$V_S = V_{S1} + V_{S2}$$

$$V_{S1} = \pi[(R_2 \quad R_{UBM}^2) + (R_{UBM} \quad R_2^2) + 2/3\, R_2^3]$$

$$V_{S2} = \pi R_{UBM}^2 \quad H_1$$

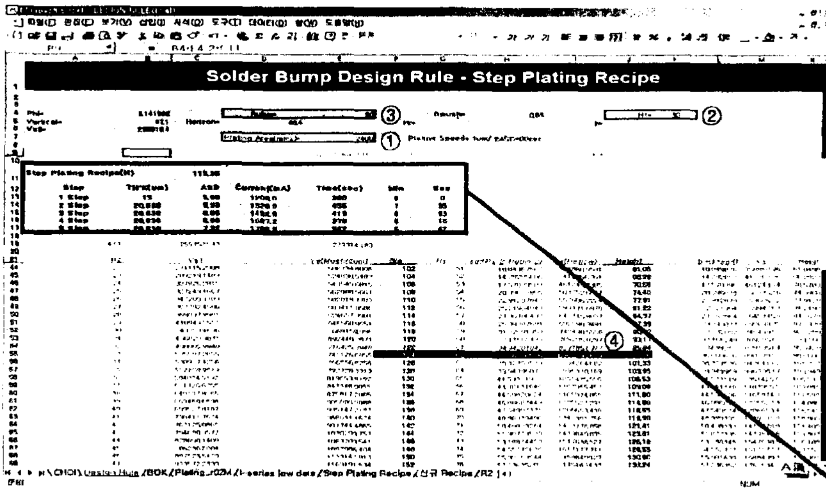
After Reflow

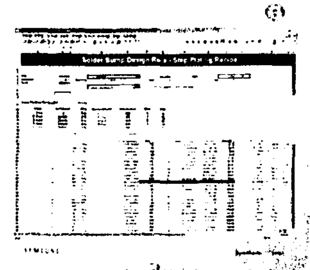
$$V_S = \pi[2/3\, R_S^3 + R_S^2 k\sqrt{R_S^2 - R_{UBM}^2} - (k\sqrt{R_S^2 - R_{UBM}^2})^3 / 3]$$

Solder Bump Height

$$R_H = k\sqrt{R_S^2 - R_{UBM}^2} + R_S$$

2. Program A
– Solder Plating Recipe





①Plating Area

②PR Thickness

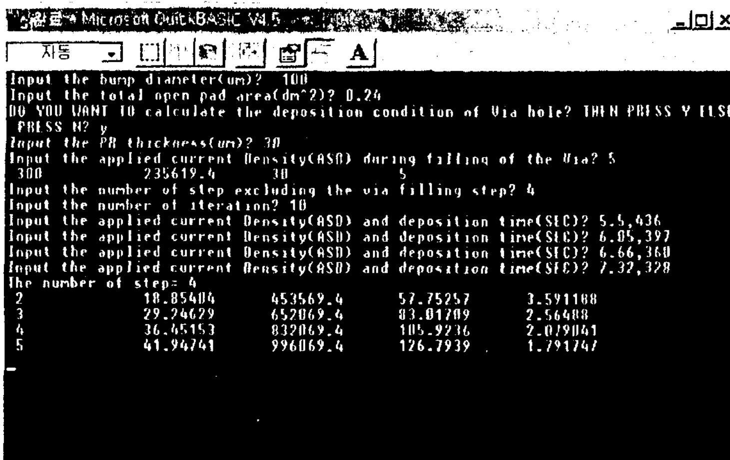
③Ratio

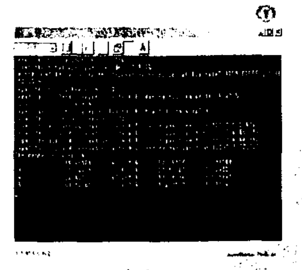
④Required Bump Height

▼

Plating Recipe

3. Program B
– Actual Current Density Simulation





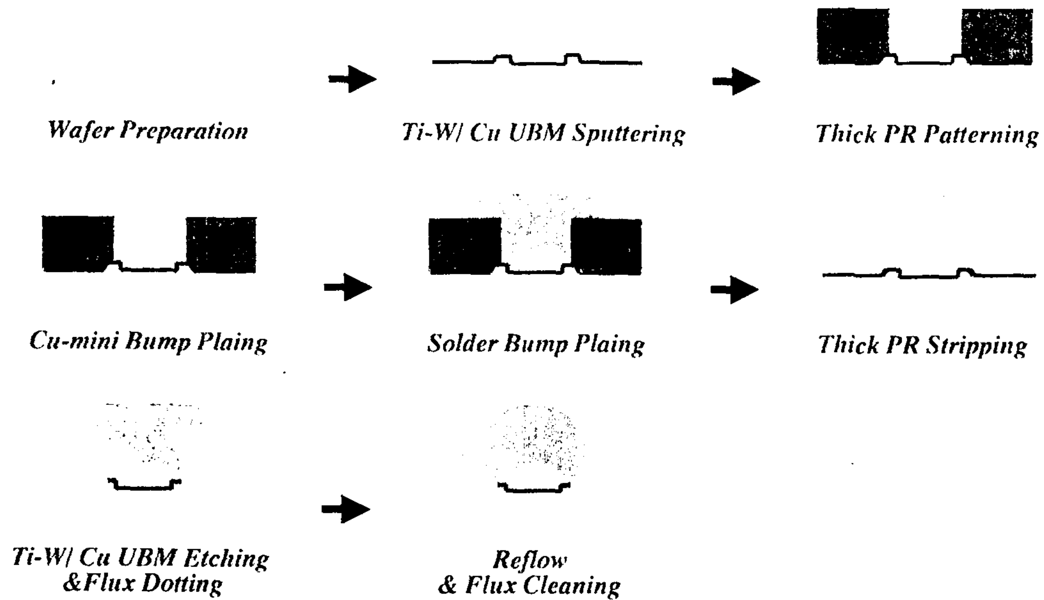
ⓐ Expected Mushroom Volume during Step Solder Plating

ⓑ Straight Height based on Chemical Equivalent

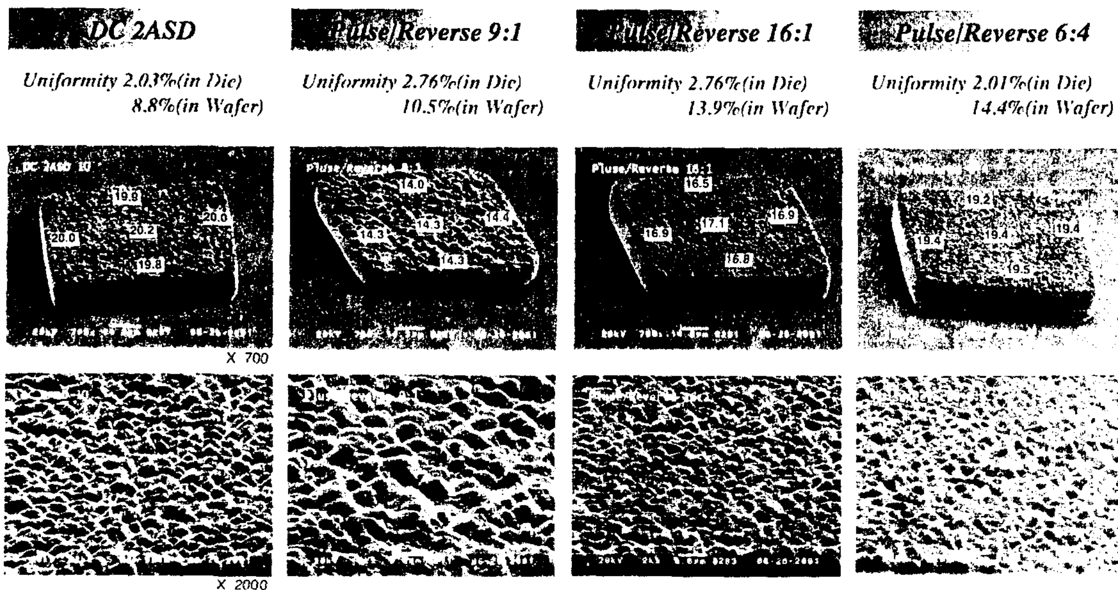
ⓒ Actual Current Density of Mushroom Surface during Step Solder Plating

Solder Bump Fabrication

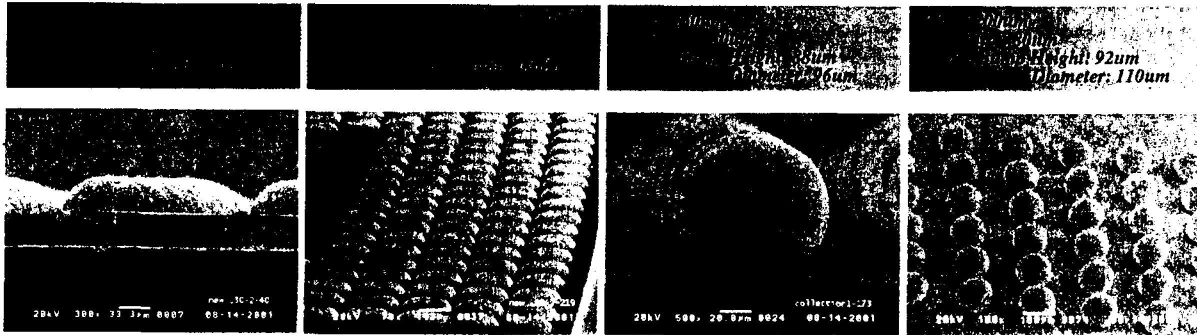
1. Solder Bumping Process



2. Cu-mini Bump Formation



3. Solder Bump Formation



Uniformity 1.7%(in Die) 4.2%(in Wafer)

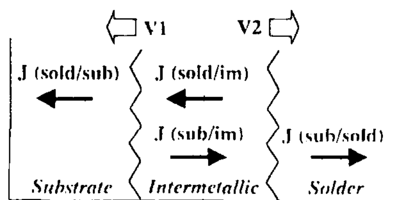
Uniformity 1.6%(in Die) 3.7%(in Wafer)

Uniformity 1.2%(in Die) 4.9%(in Wafer)

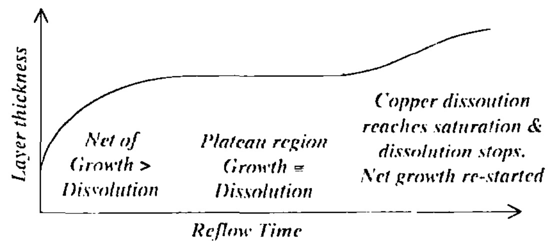
Uniformity 1.2%(in Die) 3.7%(in Wafer)

The Results of Reliability Test

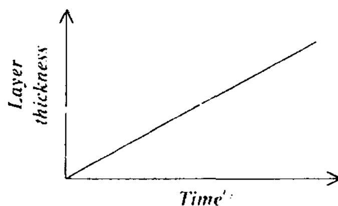
1. Theory of IMC Growth Kinetics



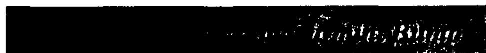
(a) Schematic diagram of IMC growth



(c) Ideal 3-step IMC growth



(b) Ideal diffusion controlled growth



- *Diffusion controlled growth*
- *Rapid initial growth & later diffusion controlled growth*
- *3-stages growth*

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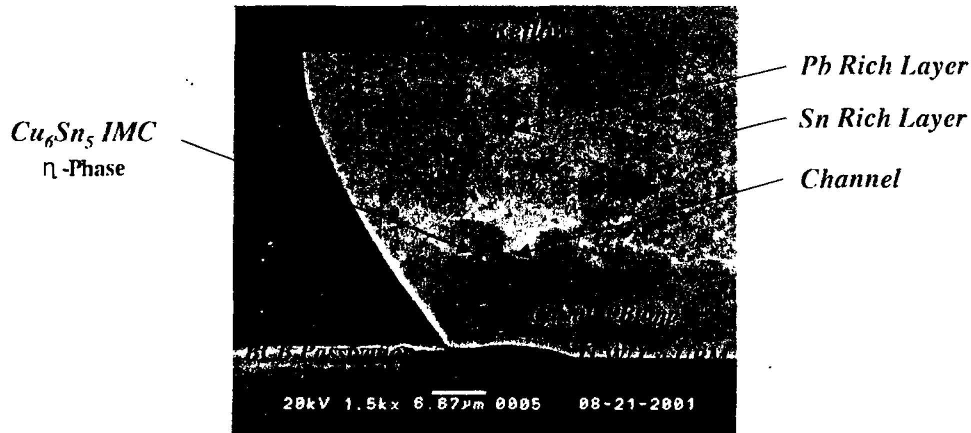
2. Interfacial Reaction between Solder and Cu-mini Bump

- Growth of Cu_6Sn_5 IMC Structure



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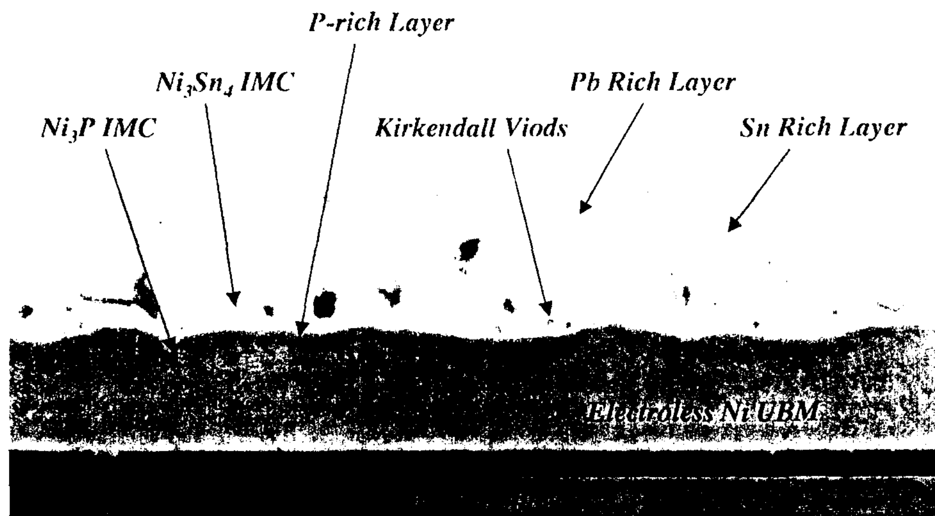
3. Interfacial Reaction between Solder and Electroless Ni UBM

- Growth of Ni_3Sn_4 IMC Structure



4. Microstructure Investigation

Intermetallic compound of Cu_6Sn_5 that has Scallop-like shape grows at the interface between Cu and solder

- *Micro- channel formed along the Cu6Sn5 grain boundary offers a fast diffusion path for IMC growth*
- *Spalling occurs*

Failure locus : Inside of solder and IMC

Intermetallic compound of Ni-Sn that has lath type grows at the interface between Ni and solder

- *IMC growth rate of Ni-Sn compounds is lower than that of Cu-Sn compounds*
- *Kirkendall void formation and embrittlement (Spalling does not observe)*

Failure locus : Inside of solder and IMC and trace of the Kirkendall voids

The formation of Kirkendall void
: If one element diffuse more quickly than the other,
excess vacancies will be formed in the material with the highest diffusion rate

- *Excess vacancies accumulate and coalesce*
- *A line of voids form*

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5. Diffusion Coefficient

[illegible]

At Room Temperature(25℃): $D=2 \times 10^{-6}$ cm²/sec
Between 140℃ and 230 ℃: $D=2.4 \times 10^{-3} \times \exp(-33.1/RT)$ cm²/sec

[illegible] of Ni (into Sn)

Between 25℃ and 100 ℃: $D=1.92 \times 10^{-2} \times \exp(-18.1/RT)$ cm²/sec
Between 120℃ and 200 ℃: $D=1.87 \times 10^{-2} \times \exp(-54.2/RT)$ cm²/sec

Power Law Modeling

$X(t,T) = k\, t^{n}$ for $X(0, T) = 0$

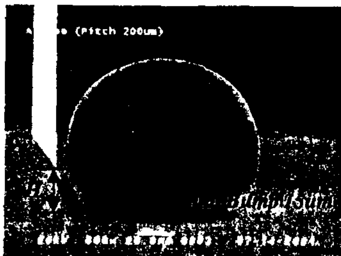
X : Average Thickness	t : Reflow Time	k : $k_0 \exp(-Q/RT)$
T : Isothemal Temperature	n : Growth Exponent	

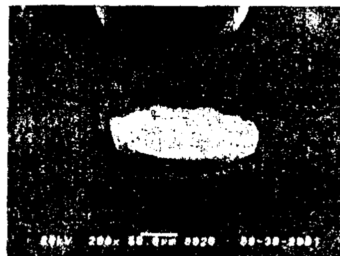
6. Room Temperature Physical Properties of IMCs

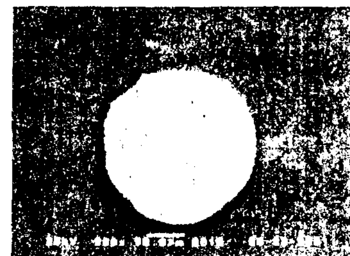
Properties	Cu_6Sn_5 (η -Phase)	Cu_3Sn (ε -Phase)	Ni_3Sn_4
Vickers Hardness (kg/mm2)	378 ± 55	343 ± 47	365 ± 7
Toughness (MPa m$^{-1/2}$)	1.4 ± 0.3	1.7 ± 0.3	1.2 ± 0.1
Youngs Modulus (GPa)	85.56 ± 1.65	108.3 ± 4.4	133.3 ± 5.6
Shear Modulus (GPa)	50.21	42.41	45.0
Thermal Expension (X 10^{-6}/ ℃)	16.3 ± 0.3	19.0 ± 0.3	13.7 ± 0.3
Thermal Diffusivity (cm^2/sec)	0.145 ± 0.012	0.24 ± 0.024	0.083 ± 0.008
Heat Capacity (J/gm/deg)	0.286 ± 0.012	0.326 ± 0.012	0.272 ± 0.012
Resistivity (μ ohm·cm)	17.5 ± 0.1	8.93 ± 0.02	28.5 ± 0.1
Density (gm/cc)	8.28 ± 0.02	8.9 ± 0.02	8.65 ± 0.02
Thermal Conductivity (watt/cm·deg)	0.341 ± 0.051	0.704 ± 0.098	0.196 ± 0.019

Source: The mechanics solder alloy interconnects

7. Failure Analysis – (a)





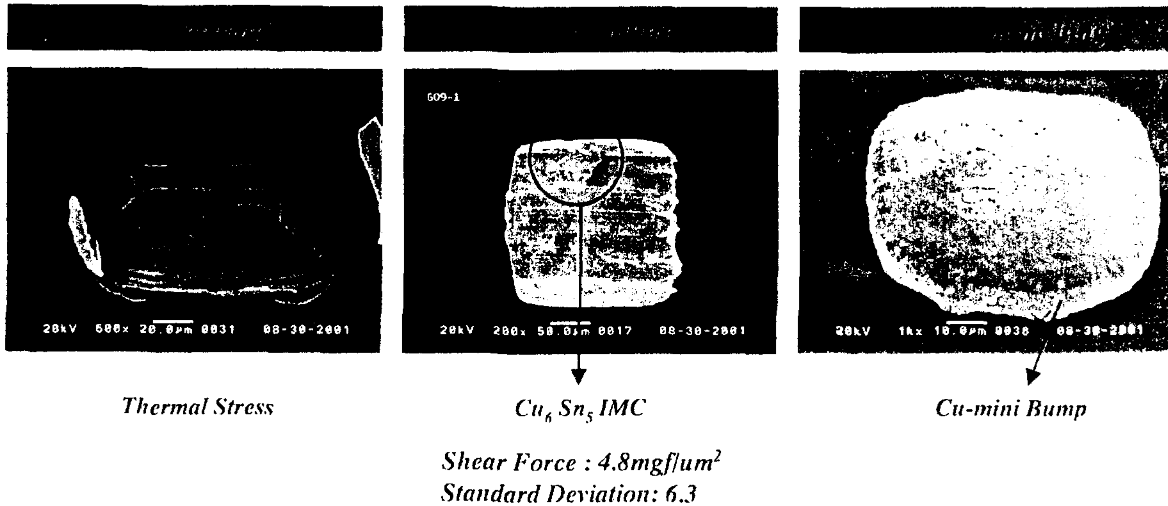


Titled image *Top view*

Test Condition
H : 20um
Test speed: 200 um/sec
Test load: 3.0 g
Load speed: 330 um/sec
Over travel: 150 um

Shear Force : 5.8mgf/um^2
Standard Deviation: 13.8
Shear Mode: Soft Shear inside Solder

7. Failure Analysis – (b)



Thermal Stress *Cu_6Sn_5 IMC* *Cu-mini Bump*

Shear Force : 4.8mgf/um^2
Standard Deviation: 6.3

Conclusion and Future Works

Electroplating solder bumping process by using Ti-W/Cu UBM system was succesfully developed.

The solder bump uniformity could be controlled by electroplating method within 5%

With the simple calculation, We could predict the solder ball size.

<u>Future work</u>

Reliability test on board level

Developments of lead free solder bump by electroplating method

New-UBM stucture for lead free solder bump