The Thermal Characterization of Chip Size Packages

Sang Wook Park, Sang Ha Kim, Joon Ki Hong, Deok Hoon Kim*
Hynix Semiconductor Co., Ltd.
* Flip Chip Technologies
sawpark@hynix.com

Abstract

Chip Size Packages (CSP) are now widely used in high speed DRAM. The major driving force of CSP development is its superior electrical performance than that of conventional package. However, the power dissipation of high speed DRAM like DDR or RAMBUS DRAM chip reaches up to near 2W. This fact makes the thermal management methods in DRAM package be more carefully considered.

In this study, the thermal performances of 3 type CSPs named μ-BGA^{TM}, *Ultra*CSP^{TM} and OmegaCSP^{TM} were measured under the JEDEC specifications and their thermal characteristics were of a simulation model utilizing CFD and FEM code. The results show that there is a good agreement between the simulation and measurement within Max. 10% of Θ_{ja}. And they show the wafer level CSPs have a superior thermal performance than that of μ-BGA. Especially the analysis results show that the thermal performance of wafer level CSPs are excellent for module level in real operational mode without any heat sink.

Key word : μ-BGA, *Ultra*CSP, OmegaCSP, thermal performance, CFD, FEM

Introduction

The driving force of package development is the realization of small size, high reliability and low cost package. Currently, the TSOP is widely used in field of DRAM package because of its acceptable performance and low cost. However, as the electronic system get smaller in its size, lighter weight and higher in its speed, the TSOPs are being very replaced with CSPs in many applications like PDA (Personal Digital Assistant) or note book PC. Especially, the many DRAM makers are developing the CSPs for the high speed DRAM such as RAMBUS DRAM to optimize the device performance because the CSPs have solutions of electrical and thermal managements for its immunized undesirable parasitic RLC and short thermal path to the environment.

The CSPs can be categorized briefly by three groups, the rigid substrate type like FBGA, flexible substrate type like μ-BGA^{TM} and wafer level package type like UltraCSP^{TM} and OmegaCSP^{TM}. [1-2] Flexible or rigid substrate type CSPs are now widely used in flash memory and SRAM, and has a high potential to be used in DDR or RAMBUS DRAM. The assembly infrastructure for these CSPs has been built-up to a certain level and most system makers are now very interested and ready for use of these CSPs in their systems. However, the relatively high assembly cost and difficulties in manufacturing are

reported still remained limitations of these CSPs.

The wafer level CSP (WLP), as it can be seen in the name, is made by a wafer level process where as the other packages are made by a unit level or strip level process. The WLP seems to be advantageous in terms of cost because the structure and accompanying process seem to be simpler than those of other CSP groups. On the other hand, its robustness and reliability seems to be one of concerns because it is almost the same as the flip chip die without any protection element like thick plastic encapsulant in plastic packages. Thus its robustness and reliability should be verified in order to replace the current plastic packages. [3-5] However, the matured fabrication technologies can help the WLP to obtain a sufficient design margin of interconnection lines and its excellent electrical performance make the device makers to develop technologies of a WLP.

It is said that the electrical performance and reliability are first considerations in DRAM packaging technologies. Thermal performance has been a secondary consideration in DRAM packaging because the power dissipation has been not much serious. In case of SDRAM used in PC133, the power dissipation is about 0.5W/chip where it reaches up to about 2W/chip in case of 400MHz D-RDRAM. [6] As the chip size is getting smaller, thermal resistance of package becomes more serious problem because the dissipation power density of chip goes to higher. That makes the thermal management in DRAM be much more important than the past had been. In this study, thermal performance of μ-BGA ^{TM} and WLP was characterized and was investigated how much have a thermal design margin for high-speed DRAM applications.

Structure and Characteristics of CSPs

Figure 1 shows the cross sectional view and assembled out photograph of μ-BGA ^{TM}, UltraCSP ^{TM} and OmegaCSP ^{TM}. The test vehicle is the 72M D-RAMBUS DRAM of Hyundai Electronics. As the shown in the figure, the interconnection methods of these packages are similar and are proper to get sufficient design margin for good electrical performance. The principal dimensions used in this study are summarized in Table 1.

It is important point that the assembly process of WLP is simpler than μ-BGA ^{TM}. It is similar to that of IC fabrication as shown below ;

1) Spin coating of 1st dielectric layer for planarization
2) Bonding pad via opening
3) Redistribution layer metalization and patterning
4) Spin coating of 2nd dielectric layer for protecting metal trace
5) Solder ball land via opening and Solder ball mounting

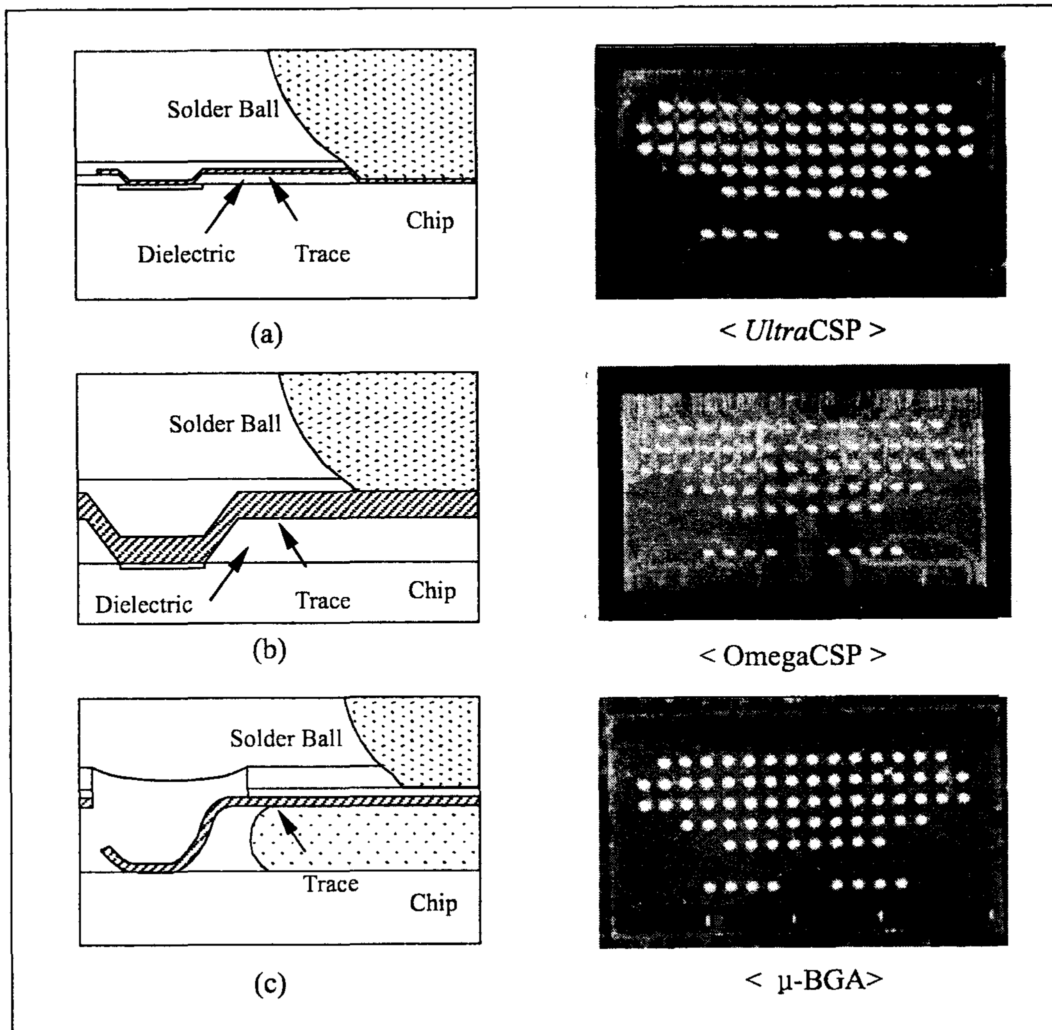


Fig. 1. Cross sectional view and photograph of CSPs

This fabrication process is suitable for making very fine interconnection lines. This fact gives a more freedom for complicate trace designing to meet the RLC specifications of package for high speed DRAMs. However, It is reported that the solder joint reliability of WLP is not so good compared with μ-BGA. Thus its reliability issues are only weak points in WLP and such problems expected to be solved near future by many researchers. Among the efforts to improve the reliability of WLP, the OmegaCSP showed that the solder joint reliability of WLP could be improved by adopting the thick metal tracer and thick stress buffer layer having proper mechanical properties. [4-5]

On the other hand, the thermal performances of CSPs are expected due to its short thermal path to the ambient and board. In respect of thermal performance, these CSP has the advantages as shown below:

1) has the direct thermal path junction to board through vertical direction

2) has the very thin dielectric layer between chip and solder ball

3) has its back side of silicon chip directly exposed to the ambient

This design concept is very effective to the high power device whose dissipation power is above 1W.

TABLE I. Principal Dimensions of CSPs

Package	*Ultra*CSP	OmegaCSP	μ-BGA
Size	7.3 x 13.1	7.3 x 13.1	7.9 x 14.0
Overall Height	1.08	0.73	0.90
Ball Size/Pitch	0.45/0.75	0.35/0.75	0.35/0.75
Trace Line			
Material	Al/Ni/Cu	Ni/Cu	Cu/Au
Width	0.04 typ.	0.04 typ.	0.05 typ.
Thickness	0.002	0.012	0.020
Under Dielectric Layer			
Material	BCB	Polymer	Elastomer
Thickness	0.005	0.020	0.150

Thermal Analysis of CSPs

Traditionally, the thermal performance of a given package has been represented by the junction-to-ambient thermal resistance, Θ_{ja}, defined as below;

$$\Theta_{ja} = \frac{T_j - T_a}{P_{diss}}$$

Where T_j and T_a are the junction and ambient temperature, respectively, measured after the system has achieved the steady state and P is the dissipation power at the given chip.

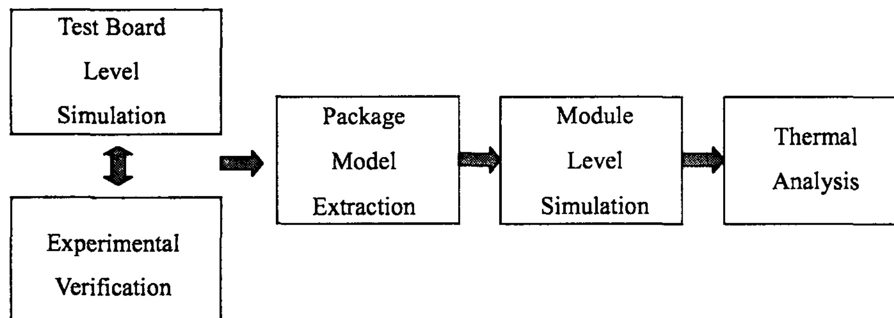


Fig. 2. Flowchart of thermal analysis for CSPs

It is a very well-defined parameter to represent the thermal performance of package. This parameter easily can be extracted by experiment based on JEDEC or Semi-Standard. However, since thermal

resistance is highly dependent on the construction of thermal board, material conductivity and environmental conditions, the application of this parameter must be carefully considered for each package and board. Therefore, this parameter is not sufficient to understand the thermal characteristics of packages in various applications. To get more thermal information in a specific application, the CFD and FEM simulation is a good tool and it can help to establish package thermal design rules.

Figure 2 show the procedure of thermal characterizing of CSPs in this study. To extract the verified package model of CSPs, we performed the simulations and experiments in exact same situations. Then, we characterize the maximum device junction temperature and power limit of the packages by adopting the package model in real RAMBUS module level.

Model Setup – Figure 3 show the typical thermal model in this study. The package and thermal test board were modeled in full 3D utilizing the Flotherm CFD code.[7] Figure 4 is the thermal network of CSP and each resistor represents the intrinsic thermal resistance of each component through the junction to air. The compact model using the thermal resistor network has some advantages to understand the thermal characteristics of CSPs having simple structure. [8-10]

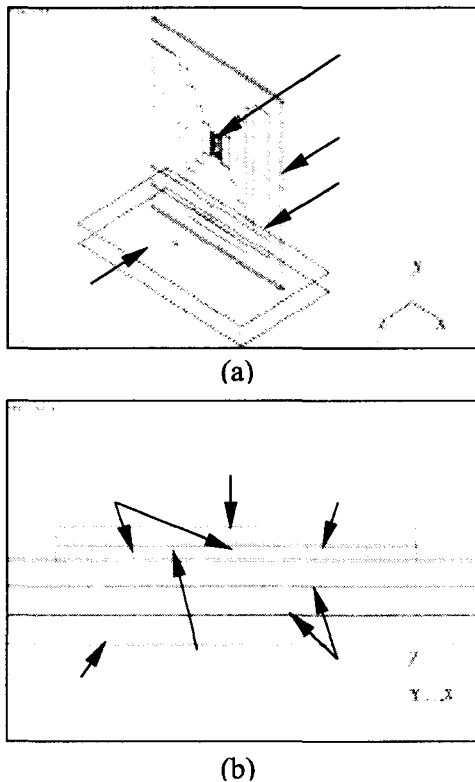


Fig. 3. Typical CFD model of CSP
((a) 3-D view (b) sectional view)

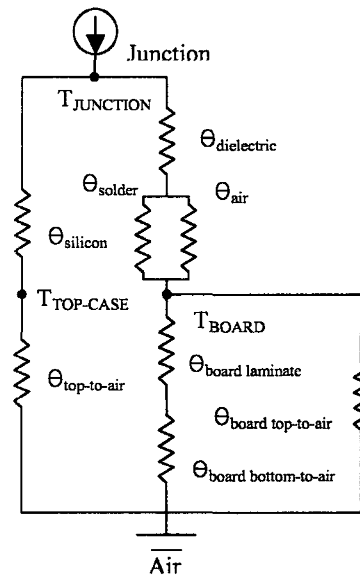


Fig. 4. Thermal network diagram of CSP

However, There are some difficulties to get the proper thermal model verified by experiment – especially in module level – because this kind of model needs the BCI (boundary condition independent) environments. Therefore, in this study the thermal model using CFD code only used. Table 2 shows the thermal conductivity of each material using in the thermal model.

TABLE II. Thermal conductivity of raw materials

Raw material	K (W/m.K)
Silicon	145
Elastomer	0.175
Alloy42	14.7
Low k Polymer	0.15
Copper	3875
Fr4	0.30
Air	0.0261

Package Model – Package model can be simplified to three cuboids of chip, dielectric layer and solder ball layer. Figure 5 shows the trace pattern of CSP. The design of trace is so complicate that it is impossible to model that pattern in detail. Therefore, the dielectric layer containing that pattern can be simplified to an equivalent cuboid having the effective thermal conductivity by considering the metal trace thickness and its coverage. For instance, the dielectric layer of OmegaCSP simplified to one cuboid having 32um thickness and its effective thermal conductivity ($k_{xx,eff}$) is 43.4 W/mk.

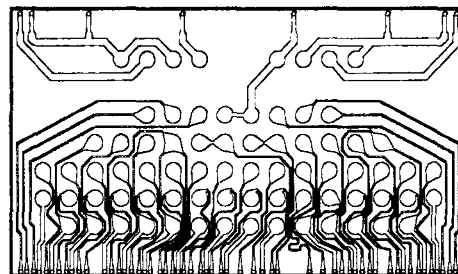


Fig. 5. Metal pattern design of CSP

Test Board Model – Generally the main heat flow path of test system is die-to-solder ball-to-thermal test board-to-air. This fact shows that the test board model is very important in order to numerically verify the thermal performances of packages accurately. In this study, we used the JEDEC standard test board like Fig 6. The principal dimensions of test board were summarized at Table 3.

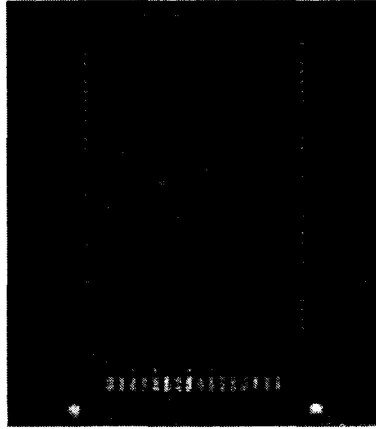


Fig. 6. Thermal test board

TABLE Ⅲ. Specifications of thermal test board

Dimension	Specification
Board thickness	1.57mm
Board dimension	101.6 x 114.3 mm^2
Board material	FR4
Fan-out trace length	25mm
Trace thickness	0.071mm ± 20%
Trace width	0.15mm ± 10%
Via spacing	2.54mm
Via land	1.27mm
Via drill hole	0.83mm

The signal layers of test board can be simplified to small cuboids. The thermal conductivity of each cuboid can be calculated by fallowing equations. In order to calculate the effective thermal conductivity of board accurately, the thermal spreading effect can be considered.[11-12]This method is effective if the board was simplified to single cuboid. Another way to minimize the errors of thermal conductivity in board is adopting the model having multiple layers along the cross section of board. In this study, we used the later method and it is effective for the test board and DRAM PCB having metal plane such ground or power plane.

Solder Ball Model – The solder balls are modeled as one cuboid with substance of single conductivity inside. This modeling method is very general to reduce the computational cost in CFD field. As this single cuboid consist of solder ball and air acting thermal resistors in parallel, the effective thermal conductivity becomes $k_{SL} = f_{solder}k_{solder} + f_{air}k_{air}$ ~ 9.27 W/mK. However this approach is base on

assumption that the same temperature gradient exists on both resistors. In fact, the different conductivity of material causes the thermal constriction near the solder ball and air. This error can mislead the over-estimation of the thermal performance. In this case, the effective thermal conductivity can be properly obtained by using the thermal sub-modeling method. [13-14]

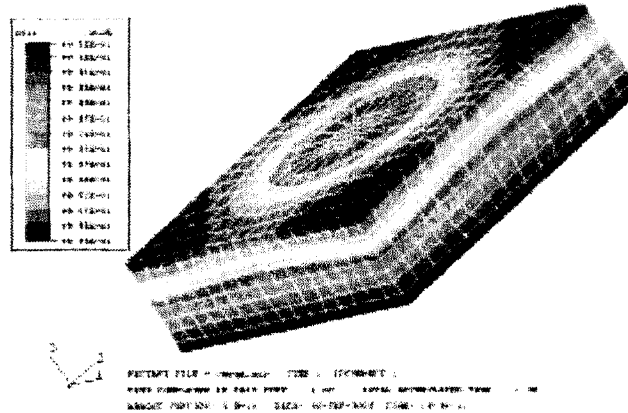


Fig. 6. Temperature contour of solder ball layer for sub-modeling analysis

Fig 6 shows the result of a conductive thermal simulation using ABAQUS that is commercial FEM code. The effective conductivity of solder ball layer is predicted to be 1.29 W/mK from the FEM results. Table 4 shows the simulation results with or without adopting thermal sub-modeling method. The difference between two models can be more pronounced in the condition that the board is good heat spreader – especially real memory module. Therefore thermal sub-modeling method is needed to predict accurate thermal performance of packages.

TABLE IV. The effect of thermal sub-model on thermal resistance

Sub-Model	k_{zz} for solder ball layer	Cal. Θ_{ja} *
Detail model	-	58.21
With	1.29	58.80
Without	9.27	55.59

** for OmegaCSP @ P_{diss} = 2.0W, natural convection*

Experimental Verification

Table 5 shows the summary of the thermal test conditions of the CSPs. The thermal performances of 8 test-packages were measured under both natural convection conditions in 1ft^3 sealed chamber and forced convection conditions in wind tunnel with a 12" square test section. Each sample has exposed at 4 air velocities; 0, 200, 400, 600 ft/min with the forced air direction along the long dimension of the package.

Four dissipation power levels were applied to the package. The value of Θ_{ja} and junction temperature predicted by the model for each conditions were compared to the sample average value.

Table Ⅴ. Thermal test conditions for CSPs

Heating Power (W)	0.5, 1.0, 1.5, 2.0
Heating Time (min)	> Avg. 15min
Air Velocity (ft/min)	0 – 600
Calibration Range (℃)	0 - 125
Ambient Temperature (℃)	23- 24

The tested CSPs were constructed using Hyundai's 72M Direct RAMBUS DRAM chip. The DUT was electrically interconnected like simple diode. So that the chip was normally heated by VCC and VSS pin, and the junction temperature was calculated from the detected forward bias voltage (V_f) of substrate diode In order to use the V_f as the temperature sensitive parameter (TSP), the calibrations of the diode were performed at the temperature range from 25℃ to 125℃ after equilibrium.

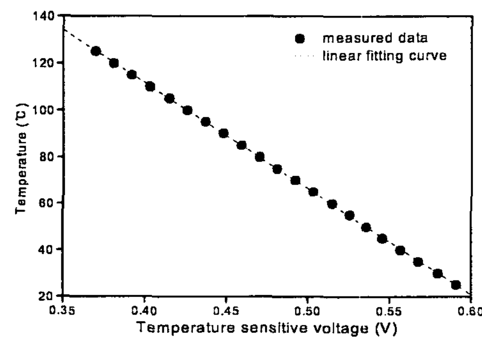


Fig. 8. Temperature calibration curve

Figure 8 shows the calibration curve of RAMBUS DRAM. The slope of that curve so called k-factor. The k-factor can be defined following equation. In this study, the value was 450℃/Volt.

$$k = \left| \frac{T_{j2} - T_{j1}}{V_{f2} - V_{f1}} \right|$$

Results and Discussion

Thermal Characteristics of CSPs - The numerical analysis was performed at the range of dissipation power from 0.5W to 2.5W within still-air chamber or wind tunnel. Figure 9 shows the temperature contour corresponding to the natural convection case at 2.0W dissipation power. As a matter of course,

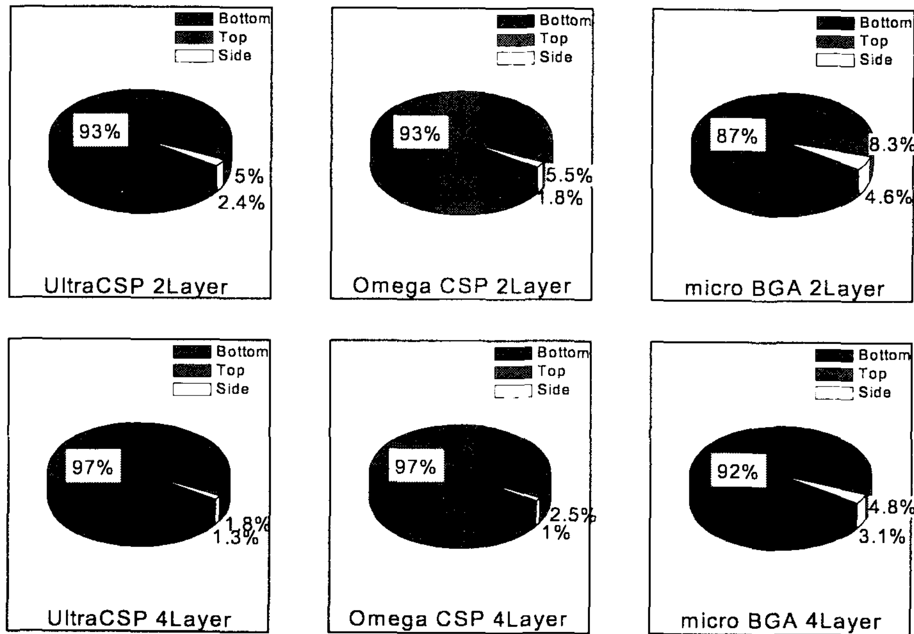
the temperature gradient has a maximum value at solder ball layer and the major heat path is die-to-board-to-air. The principle results in case that the power level is 2.0W are summarized Table 6. The average deviation of model from experiment is about 10%. The level of agreement between the predicted and measured values can be considered good.

Fig. 9. Temperature contour of OmegaCSP for natural convection (P_{diss}=2.0W)

TABLE VI. Junction-to-air thermal resistance of CSPs

Condition		Junction-to-air thermal resistance (℃/W)					
Board	V_{air} (ft/min)	μ-BGA		*Ultra*CSP		OmegaCSP	
		Exp.	Cal.	Exp.	Cal.	Exp.	Cal.
2 layer	0	60.7	67.0	52.6	54.1	57.9	60.0
	200	51.1	53.5	40.5	42.5	47.9	50.1
	400	46.6	45.5	37.0	35.7	42.8	42.7
	600	43.1	41.0	33.4	32.1	39.6	38.6
4 layer	0	37.6	39.8	25.6	24.7	28.4	30.4
	200	32.7	34.3	21.8	20.7	26.7	26.4
	400	32.2	31.2	20.8	19.1	26.1	24.4
	600	31.5	29.4	19.4	18.2	25.8	23.2

The simulation results show that the thermal resistance of μ-BGA is relatively higher than wafer level CSP. This fact is related to the dielectric layer's thickness of CSPs. Figure 10 shows the results of the heat flux for each CSP at natural convection. The heat flux to the board of μ-BGA is 5-6% below the average heat flux value of wafer level CSP. Such fact show the dielectric layer acts as the major thermal resistor in CSP structure. In aspect of solder joint reliability or electrical performance, the thick dielectric layer has some advantage because it act as stress buffer layer and decrease the capacitance of package.[1] However, as this feature can increase the cost for thermal management, it is need to determine the proper thickness of dielectric layer. We will discuss about this point at module level simulation of CSPs.



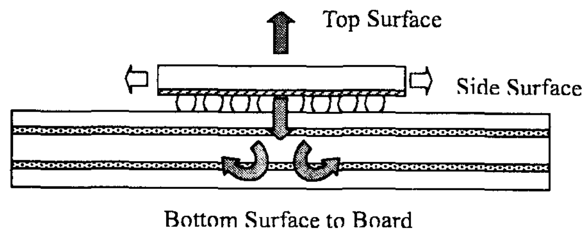


Fig. 10. Heat flux projection of CSPs

Module Level Simulation of CSPs - Figure 11 show the model of memory module mounted by 8 CSPs in this study. In this model, the CSP model was extracted from the simulation of thermal test board verified by experiment. Therefore the modeling error of CSP can be minimized. The size of module is 133x32x1.27 mm3. The RAMBUS module has generally 8 copper layer and many signal vias. Therefore the thermal conductivity of RAMBUS module is higher than that of normal DRAM module. Especially, the signal vias around the ball land of module are so many that they can be considered to the thermal vias. In this study, it is calculated by FEM the effective thermal conductivity of region around ball land including signal vias.

Figure 12 shows the schematic diagram of unit via of RAMBUS DRAM module. Its effective thermal conductivity was calculated by FEM that $k_{zz,via}$ = 15.8 W/mK and $k_{xx,via}$ = 13.9W/mK. Additionally, the

analytic solution is reported such that the effective cross plane thermal conductivity of PCB can be calculated by the fallowing simple equation. [15]

$$k_{zz,via} = k_{zz,novia}[\frac{\pi}{4}(d/p)^2 + \frac{k_{copper}}{k_{FR4}}\pi(\frac{t_{copper}}{p})(d/p)+1]$$

Where d is via diameter and p is via pitch, and t_{copper} is thickness of copper in the via hole. The $k_{zz,via}$ and $k_{zz,novia}$ are the cross plane thermal conductivity considering and not considering the via holes, respectively. The analytic solution showed that it is slightly higher than FEM result and the value is 18.6 W/mK. In this study, we used the value from FEM analysis in aspect of considering the safety factor.

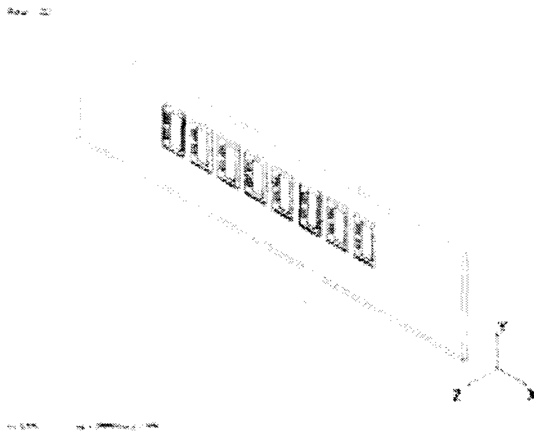


Fig. 11. CFD model of CSP module

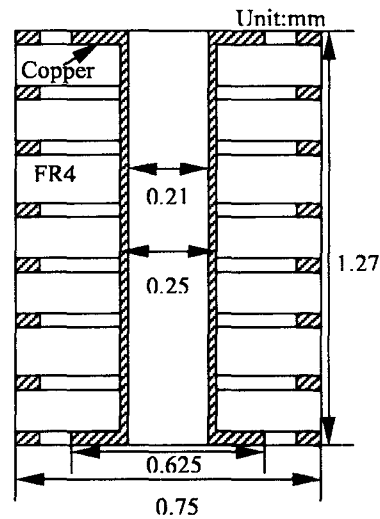


Fig. 12. Schematic diagram of via hole

Table 7 shows the results of RAMBUS module level simulation. The environment conditions is so simple system level that the ambient temperature is 55℃ and air velocity is 200ft/min. Additionally, considering the RAMBUS chip act serial in operating, the center CSP is only active and the others are standby. The standby power level is 0.08W.

TABLE Ⅶ. Maximum temperature of CSP module

Package / Pdiss	Maximum Temperature (℃)		
	μ-BGA	*Ultra*CSP	OmegaCSP
1.0 W	90.3	74.5	80.8
2.0 W	121.1	89.5	100.4
3.0 W	151.9	104.4	110.0

Considering the operating power of RQMBUS DRAM is normally 2.0W, the maximum junction temperature of μ-BGA is about 120℃. The value is much higher than that of other CSPs. Considering

the maximum allowable temperature are normally $T_j < 105$℃ and $T_{board} < 90$ as the limitation for proper device operating in DRAM, the μ-BGA is not acceptable for RAMBUS DRAM applications if not adopting a heat spreader.

The simple three-resistor network model can help to determine the power limit or design margin of these CSPs. The thermal network of CSP is so simple that the relations of heat flux and temperature can be expressed as fallowing equations. [14,16]

$$Q_b = \frac{R_{ja}P_d - T_{ba}}{R_{ja} + R_{jb}}$$

$$T_{ba} = R_{ba}Q_b + T_{load} \cong R_{ba}Q_b$$

(Assumed $T_{load} = 0$)

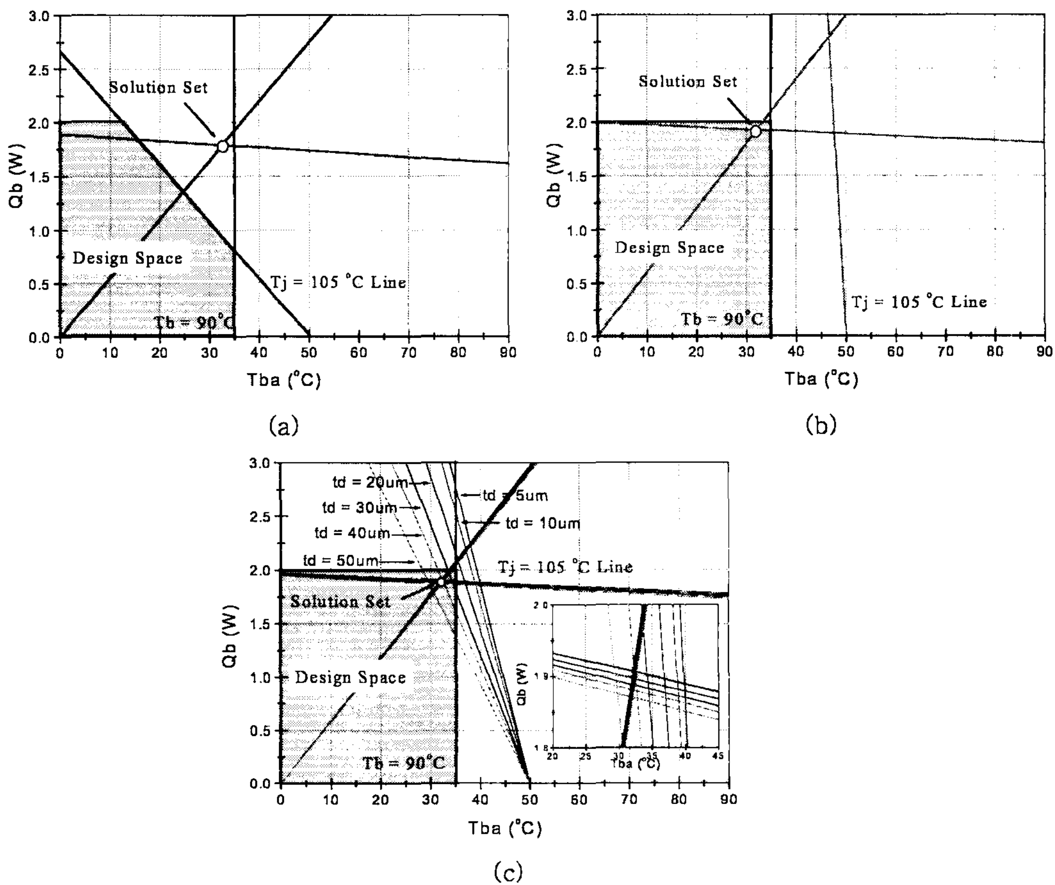


Fig. 13. Solution space of CSPs in system environment

[(a) μ-BGA, (b) *Ultra*CSP, (c) OmegaCSP]

Figure 13 show the design margin of each CSP for the fixed simple system environment that the operating power is 2.0W, airflow rate is 200ft/min and ambient temperature is 55℃. All CSPs have the small margin for limitation of board temperature. However, the wafer level CSP has sufficient thermal design margin for junction temperature considering the ambient temperature is 55℃ that is so high temperature. These results show the wafer level CSP has an acceptable thermal performance for high speed DRAM application if the thickness of dielectric is properly controlled.

As the figure 13 (c) shows the dielectric layer's thickness analysis for OmegaCSP, the $40\mu m$ dielectric layer is marginal to the specification of thermal performance. As adopting thicker dielectric layer, the board temperature is not much different but junction temperature grows higher. This fact reveals the high-speed memory module that has high copper converge and many vias can act a kind of heat spreader if the package that has low junction-to-board thermal resistance is mounted. Therefore, the wafer level CSP can be cost effective solution in aspect of thermal performance.

Summary

This study demonstrated the thermal performance of CSPs named μ-BGA, UltraCSP and OmegaCSP using CFD tool and FEM tool. The simulation results were verified by experiments under JEDEC standards. The maximum error rate between simulation and experiment is about 10%. As the verified CSPs model was apply to module level, the thermal performances of three CSPs were compared with each other and we revealed the cost effective package solution for thermal management in high-speed DRAM application.

1. The CFD model of solder ball can be single cuboid having effective thermal conductivity. Such modeling method can help to reduce the computational load. For this model, the thermal sub-modeling is proper approach using FEM code.

2. The thermal resistance of junction to air for wafer level CSP was 5-30% lower value than that of μ-BGA in thermal test under JEDEC standard environment. The discrepancy increased as the copper portion of thermal test board increased.

3. In module level simulations, the wafer level CSPs except μ-BGA show the acceptable thermal performance under simple system environment that are 2.0W power dissipation, 55℃ ambient temperature and 200ft/min air flow rate. Their junction and board temperature are below the normal thermal specifications for DRAM that maximum allowable junction temperature and board temperature are 105℃ and 90℃, respectively. The wafer level CSPs can be applied to the high-speed DRAM

applications without any thermal enhancement like heat spreader.

4. The thermal resistance of junction to air for CSPs highly depends on the thickness of dielectric layer. It is desirable to guarantee the proper operating of device that layer's thickness is controlled below 40μm.

μ-BGA *TM* is a trademark of Tesser Inc.

*Ultra*CSP *TM* is a trademark of Flip Chip Technologies

OmegaCSP *TM* is a trademark of Hyundai Electronics Co., Ltd.

Flotherm *TM* is a trademark of Flomerics Inc.

ABAQUS *TM* is a trademark of HKS Inc.

Reference

[1] D. H. Kim , S. W. Park, J. M. Kim, D. J. Lee, S. B. Ye, K. W. Kwak and H. S. Yoon, " Electrical Performance of a Lead Frame CSP and a Wafer Level CSP for DRAM Applications" Fourth Pan Pacific Microelectronics Symposium, Feb., 1999.

[2] R. T. Crowley, T. W. Goodman, and E. J. Vardman, "Chip Size Packaging Development", Aug. 1995.

[3] Hong Yang. *et al*, "Reliability characterization in *Ultra*CSPTM package development" in Proc. 50th ECTC, LAS VEGAS, NEVADA, May 2000, pp. 1376-1383.

[4] In-Soo Kang. et al, "The solder joint and runner metal reliability of wafer level CSP, (OmegaCSP) " in in Proc. 50th ECTC, LAS VEGAS, NEVADA, May 2000, pp. 87-92.

[5] Jong-Heon Kim. et al, "The reliability assessment of wafer level CSP" The Proceeding of SMTA, OmegaCSP, Sept. 23, 2000, Chicago, USA.

[6] "Hyundai Electronics RAMBUS/DDR Data Book", 2000.

[7] "Flotherm Manual Ver. 2.2", United Kingdom, 1999.

[8] H. Vinke and C. J. M. Lasance, "Compact models for accurate thermal characterization of electronic parts" IEEE Trans. CPMT Part A., Vol. 20, No. 4, pp. 411-419, 1995.

[9] D. H. Kim and S. J. Ham, "Thermal performance of CSP in DRAM applications" *Chip Scale International 99* SEMI, San Jose. CA. USA. Sept. 13. 1999.

[10] Avram Bar-Cohen and William B. Krueger, "Thermal characterization of chip packages-evolutionary development of compact models" IEEE Trans. CPMT Part A., Vol. 20, No. 4, pp. 399-410, 1997.

[11] T. F. Lemczyk, B. Mack, J. R. Culham and M. M. Yovanovich, "PCB trace thermal analysis and effective conductivity" 7th IEEE SEMI-THERM Symposium, pp. 15-22, 1991.

[12] J. R. Culham and M. M. Yovanovich, "Factors affecting the calculation of effective conductivity in printed circuit boards" IEEE InterSociety Conference on Thermal Phenomena, pp. 460-467, 1998.

[13] Z. Johnson, K. Ramarkrishina, B. Joiner and M. Eyman, "Thermal sub-modeling of the wirebonded plastic ball grid array pacakge" 13th IEEE SEMI-THERM Symposium, pp. 1-9, 1997.

[14] Ching-Bai Hwang, "Thermal design for flip chip on board in natural convection" 15th IEEE SEMI-THERM Symposium, pp. 125-132, 1999.

[15] R. S. Li, "Optimization of thermal via design parameters based on an analytical thermal resistance model" IEEE InterSociety Conference on Thermal Phenomena, pp. 475-480, 1998.

[16] S. Mulgaonker and H. M. Berg, "Thermal sensitivity analysis for the 119 PBGA-A framework for rapid prototyping" IEEE Trans. CPMT Part A., Vol. 19, No. 1, pp. 66-75, 1996.

Thermal Characterization of Chip Size Packages

Hynix Semiconductor Co., Ltd.
Package/Module R&D Division

Sang Wook Park

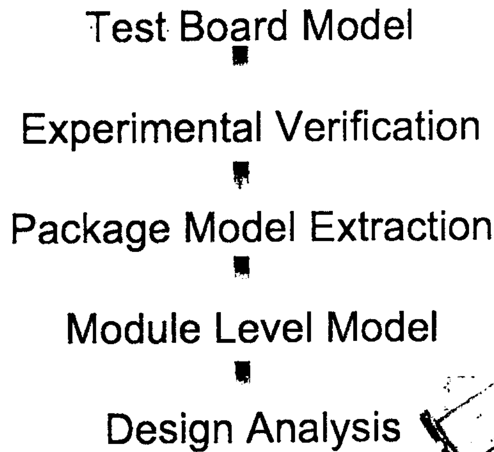
Contents

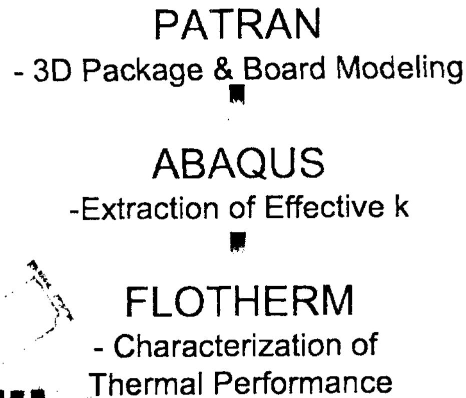
Sep. 13. 2001
3rd Joint Seminar on Packaging

- Introduction
- CSP Description
- Thermal Modeling using Flotherm™
- Thermal Sub-modeling using ABAQUS™
- Experiment Verification
- Module Level Analysis
- Summary

Introduction

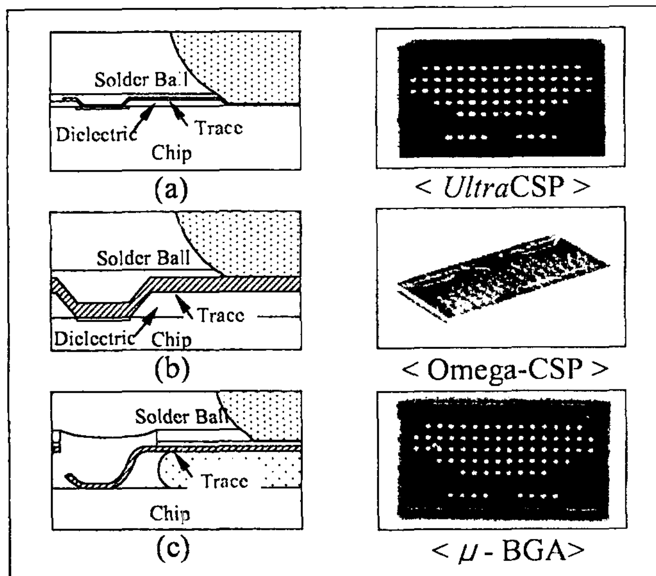
Characterization Procedure / ***Solving Procedure***





Sep. 13. 2001
3rd Joint Seminar on Packaging

CSP Description



- **Structure of CSP**

UltraCSP
- Wafer Level CSP
- Thin Dielectric Layer
- Flip Chip Technology

OmegaCSP
- Wafer Level CSP
- Medium Layer
- Hyundai Electronics

MicroBGA
- Flex Substrate CSP
- Ribbon Bonding
- Thick dielectric Layer

Principal Dimension of CSP

Package	μ-BGA	UltraCSP	Ω-CSP
Size	7.9x14.0	7.3x13.1	7.3x13.1
Height	0.90	1.08	0.73
Ball Size/Pitch	0.35/0.75	0.45/0.75	0.35/0.75
Trace Line			
Material	Cu/Au	Al/Ni/Cu	Ni/Cu
Width	0.05 typ.	0.04 typ.	0.04 typ.
Thickness	0.020	0.002	0.012
Under Dielectric Layer:			
Material	Elastomer	BCB	Low k Polymer
Thickness	0.15	0.005	0.02

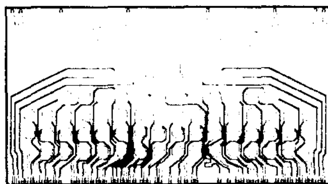
Thermal Conductivity

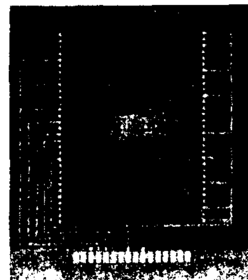
Raw Material	k (W/mK)
Silicon	Flotherm Defaults
Elastomer	0.175
Alloy 42	14.7
Low k ploymer	0.15
Copper	385
Fr4	0.3
Air	0.0261

- Simple Structure
- Dielectric Layer Thickness
- Test Vehicle is Hyundai 72M RAMBUS DRAM (How Old !!)

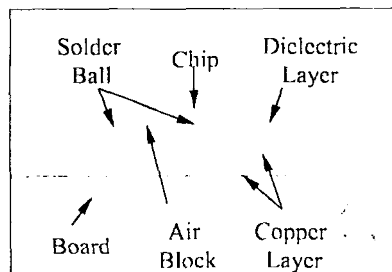
Thermal Modeling

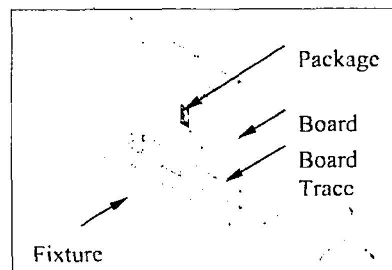
Package Model



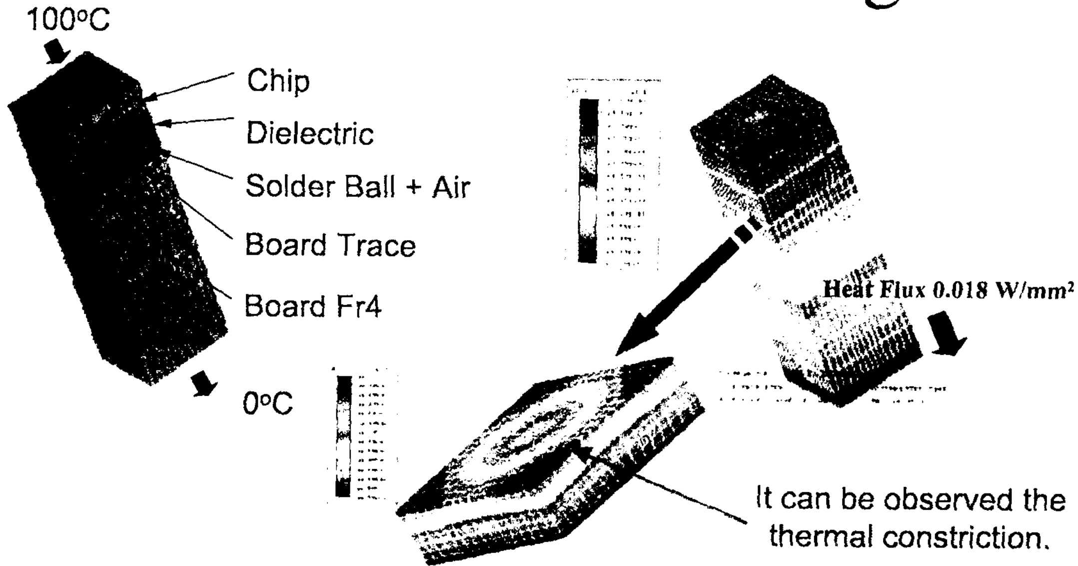


Test Board Model





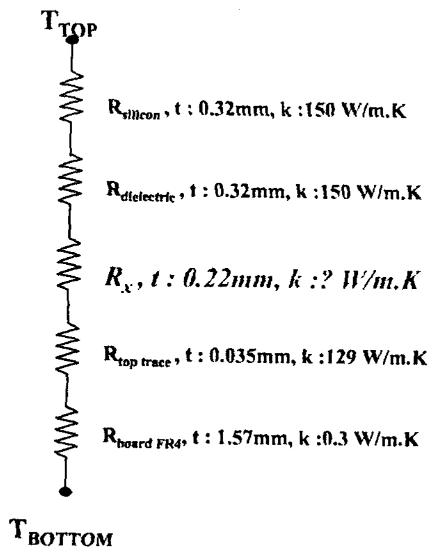
Thermal Sub-modeling



ABAQUS FEM Model & Results

Thermal Sub-Modeling

Total Thermal Network



Calculation

- The total thermal resistance can be calculated by using simple thermal network analysis.
- This method help us to decrease the modeling and iteration time.

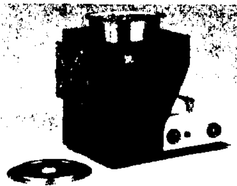
$$R_x = \Delta T / q - \sum R_i$$
$$R_i = l_i / k_i A_i$$

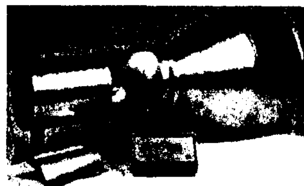
Where
R : Thermal Resistance
q : Total Heat Flux
l : distance
k : Thermal conductivity
A : Area

Experimental Verification

Phase 10 Thermal Analyzer

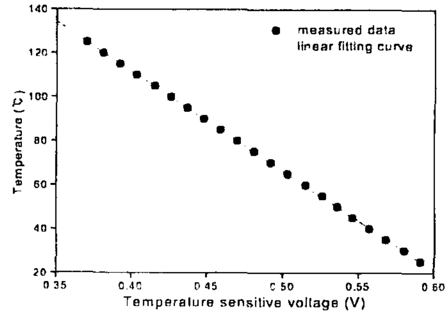
Still Air Chamber





Calibration Bath **Wind Tunnel**

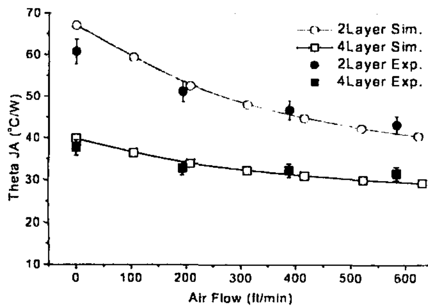
Calibration Curve

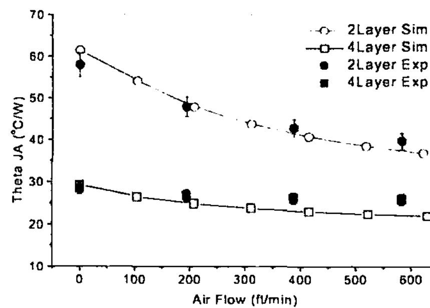


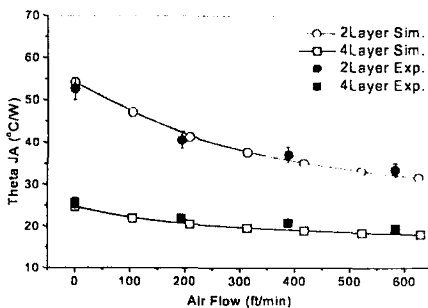
Measurement Conditions		
Board	P_{diss}(W)	V_{air} (ft/min)
2 Layer	0.5	0 (natural)
	1.0	200
4 Layer	1.5	400
	2.0	600

Verification Results

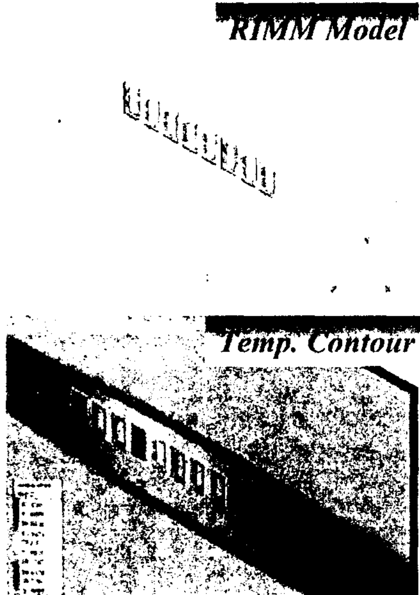
The Package Models are good for Thermal Characterizing of each package

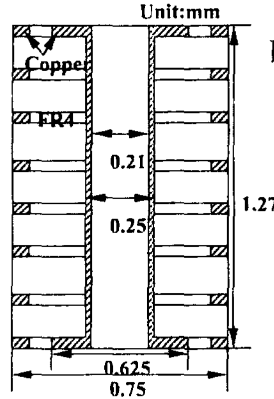






Module Level Analysis





Via Hole of RIMM

Effective thermal conductivity of via can be calculated using thermal sub-modeling

The verified package models were adopted to this module level analysis.

The signal via holes of RIMM can be considered as the thermal via holes.

Module Level Results

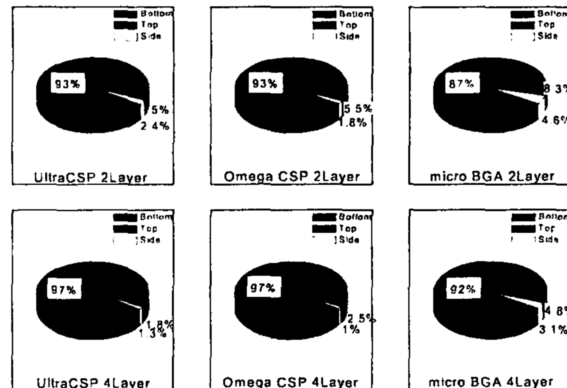
Max Tj of CSP Modules

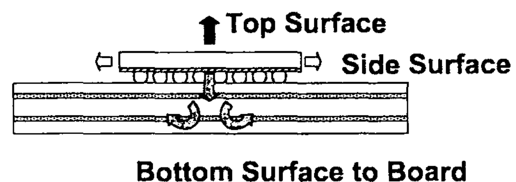
P_{diss}	μ-BGA	UltraCSP	Ω-CSP
1.0	90.3	74.5	79.0
2.0	121.1	89.5	98.6
3.0	151.9	104.4	108.2

Max Tb & Qb of CSP Modules

	μ-BGA	UltraCSP	Ω-CSP
Tb(°C)	87.5	87.2	88.5
Qb(W)	1.79	1.93	1.91

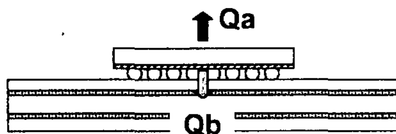
@ Ta=55oC, P_{diss}=2.0W





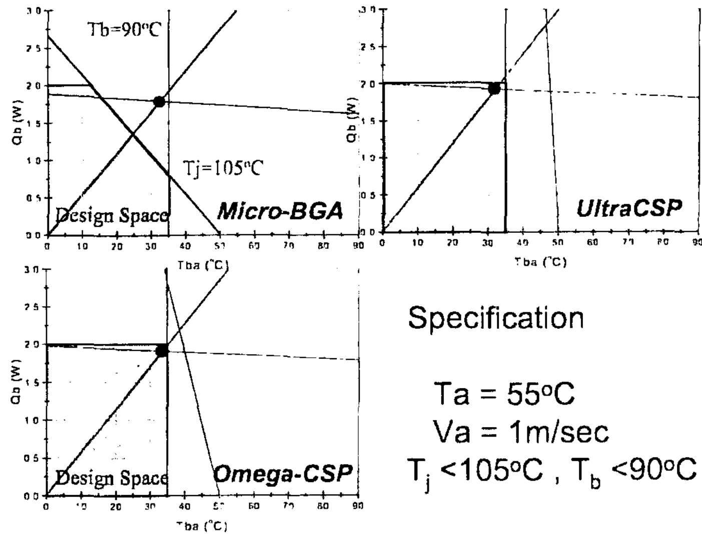
Thermal Sensitivity Analysis

Notation & Calculation



$Pd = Qb + Qa$
$Qb = (Tj - Tb)/Rjb$
$Qa = (Tj - Ta)/Rja$
$Tba = Tb - Ta$
$Qb = (Rja \times Pd - Tab)/(Rja + Rjb)$
$Tba \sim Rba \times Qb$

Design Margin Analysis



Specification

$Ta = 55^{o}C$
$Va = 1m/sec$
$T_j < 105^{o}C$, $T_b < 90^{o}C$

Sep. 13. 2001
3rd Joint Seminar on Packaging

Summary

- Thermal sub-modeling method is so effective to improved the mesh convergence and avoid overestimating the effective thermal conductivity
- The thermal performance of CSP is highly dependent on the thickness of dielectric layer of CSP.
- The wafer level CSP has an acceptable thermal performance though a heat sink is not adopted.