Package Design Considerations for High Speed IC

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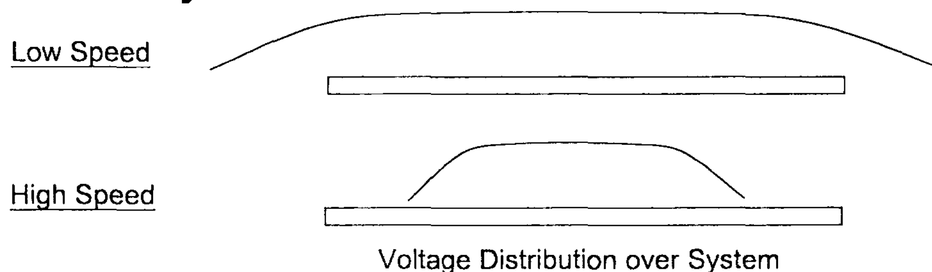
How can we define the High Speed Device in Package?

- System Clock Speed can't tell all about the speed of system.
- To know the real speed, Need to know raising and falling speed of signals. When Electrical length become shorter than size of system, the current in system shows an wave like behavior. An High speed can be defined as a system size relatively big enough comparing to wave length or an wave length relatively shorter than system size.



Voltage Distribution over System

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The Driving Force for Package is to Speed Up the System

- **Increasing IO**
  - From LeadFrame Package to BGA
- **Increasing Power Consumption**
  - Thermally Enhanced System
- **Reliability**
  - It was Very important and Now it is important
- **Increasing Switching Speed**
  - Electrically Fast Response
  - Less Noisy system

Why Different Package is Required for High Speed?

- **The Parasitic, make trouble in High Speed can't be handled as a discrete. They should be controlled by transmission line design.**
- **Multi-layered substrate type package has advantage in high speed by controlling transmission line structure.**

Mold Compound
Die Attach Adhesive
Gold Wire
Cu Leadframe
Al Heat Spreader
Die Attach Pad

MQFP
w/Drop-in Al Heat Spreader

PBGA with Multi-layer substrate

FC-BGA with Multi-layer substrate

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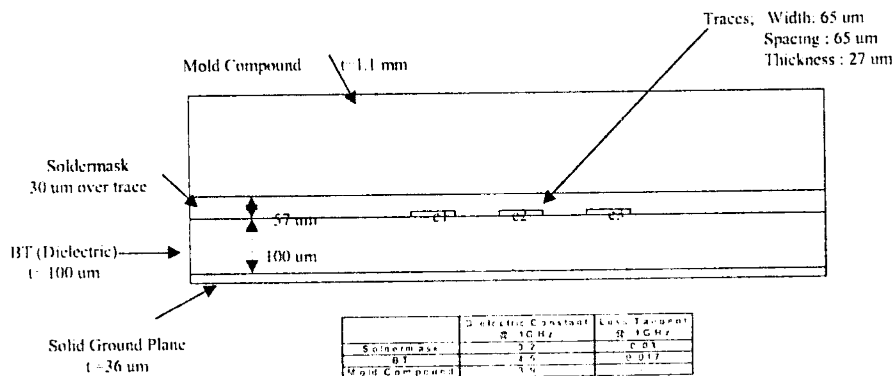
What would be an Alternatives in a Package for High Speed

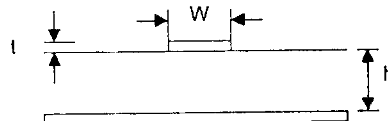
- Smaller Size package has less parasitic and make the package more robust for frequency changes.
- Shorter interconnection to the board is easier to control the parasitic.
- Precisely Controlled Impedance Pattern Design



Controlled Pattern Design for High Speed

- Impedance has two meaning
  - Characteristic Impedance Zo need to be set as 50 Ohm and controlled by adjusting stack up structures.
  - Total Impedance can't be controlled by stack up but should be controlled by redesigning the patterns.

$$Z_o = \sqrt{\frac{L_{11}}{C_{11}}}$$



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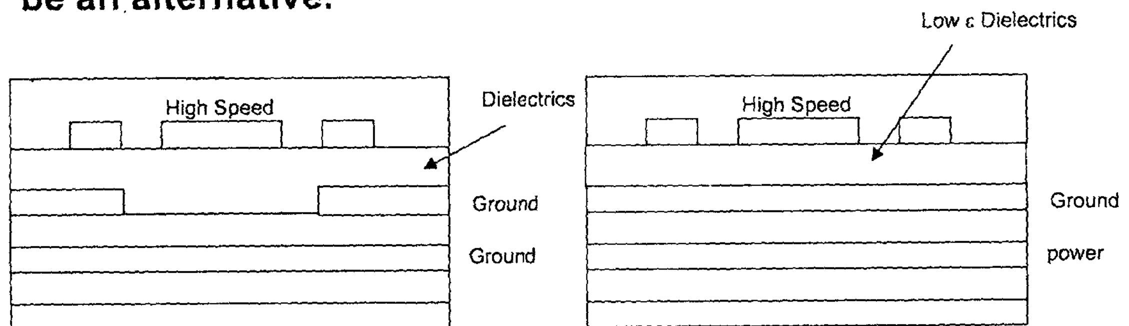
Stack Up Structure for High Speed

- The I/O transmission line should have wider trace as long as the space permit.
- The low dielectric constant material is recommended to be layered under the transmission line to compensate Impedance reduction.
- Removing GND plane under the High Speed Signal can be an alternative.



Stack up Design for Easy to Make Impedance Controlling

- Stack Up should be properly designed to control Impedance not only in calculation but also in actual part .
  - Supplier manufacturing process has limitation to control the pattern width variation
  - Impedance should be controlled within 5%~ 10%
- Wider the Trace, less the variance relatively.
  - 20 % variation in 60um line with12 um tolerance.
  - 10% variation in 120um line with 12 um tolerance.
- Wider the Width, less the impedance
  - but it need to be controlled to have 50 Ohm
  - Thicker substrate or smaller dielectric constant.

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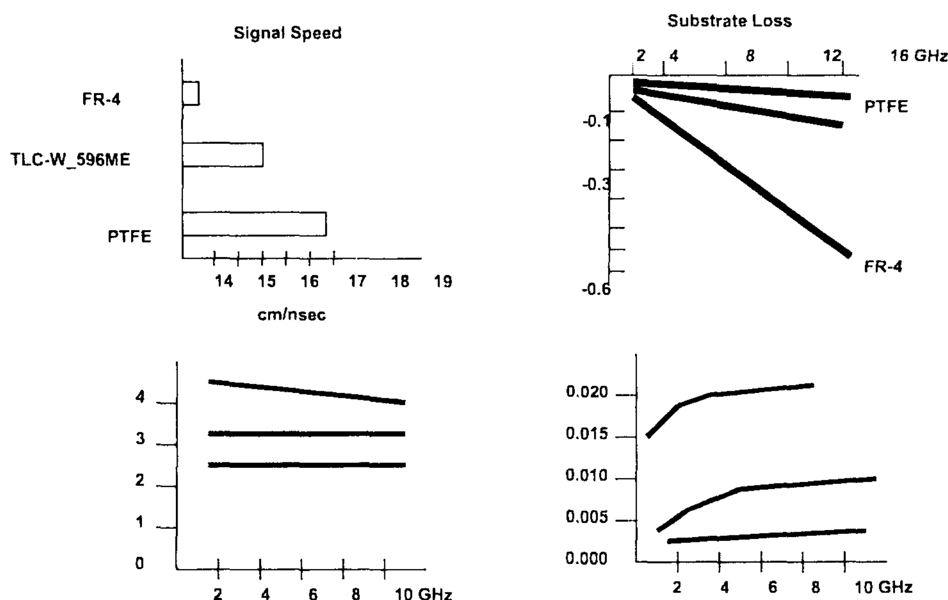
The Package Material Selection for High Speed

- **Dielectrics**
  - Dielectric constant should be proper number to get target impedance value. Neither low nor high dielectric constant is a good answer.
  - BT, FR4: ε_r = 4 PTFE: ε_r = 2.5
  - Loss Tanδ : Always low number is best choice but not significant below 10GHz.
- **Conductor Foils**
  - Profile : The foil should have smooth surface on bottom side rolled foil is preferred than plated copper over resin
  - Thickness : 20 um is enough for thickness over 1GHz
  - Resistivity : Resistance become a major barrier for high speed due to skin depth.

The Package Material Selection for High Speed

- **Dielectrics**



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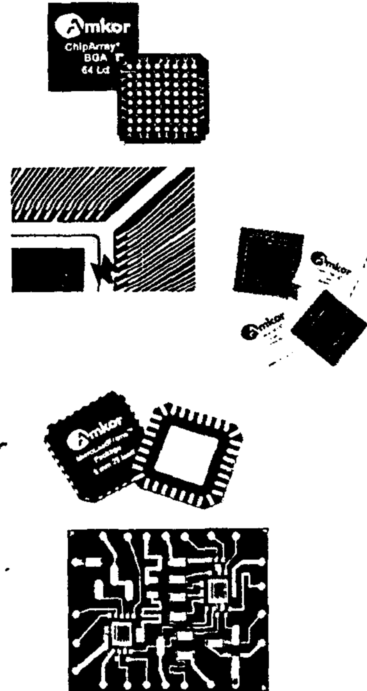
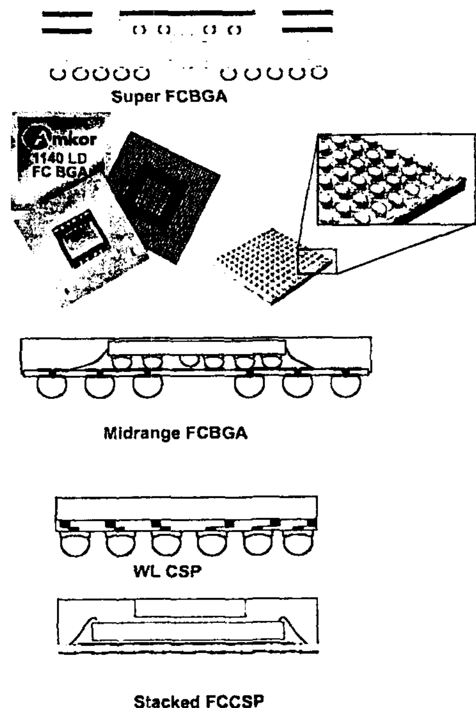
Package Selection for High Speed

- **Wire Bond Type Package ~ 10GHz**
  - CSP : Small Size, Short Wire
  - PBGA : High IO, PWR\GND Plane,PWR\GND Ring
  - HPBGA: Multi tier for High IO,Multi PWR\GND plane
  - EBGA\SBGA\TSBGA: Via less electrical path for High Speed IO
  - MLF : Short current path, Signle layer
  - SiP : Active + Passive Component, Impedance Controlled Transmission line design



Package Selection for High Speed

- **FC Bond Type Package ~ 40GHz**
  - Super FC: High thermal performance with high IO count (~ 3000 pin)
  - FCBGA : Impedance controlled transmission line, PWR\GND plane, passive components.
  - FCCSP : Small Size FC, Low cost application for 100~300 pin counts
  - WLP : RDL design (Re-Distribution Layer) + Solder Bump



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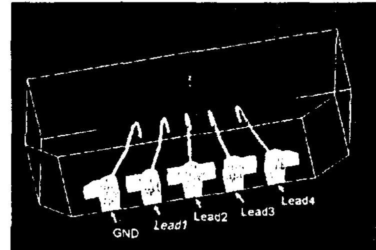
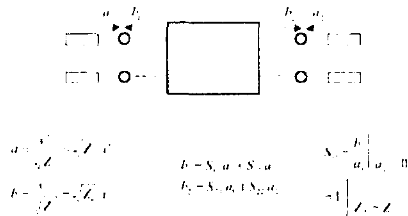
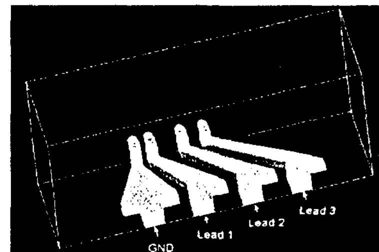
Find Limitation of Wire bonding for High Speed

- **MLF Modeling, Wire Bonding Vs FC Bonding**
  - Use Same Device, Same Size Package.
  - Frequency Range up to 40GHz
- **S-parameter Modeling**



Simulation model WB

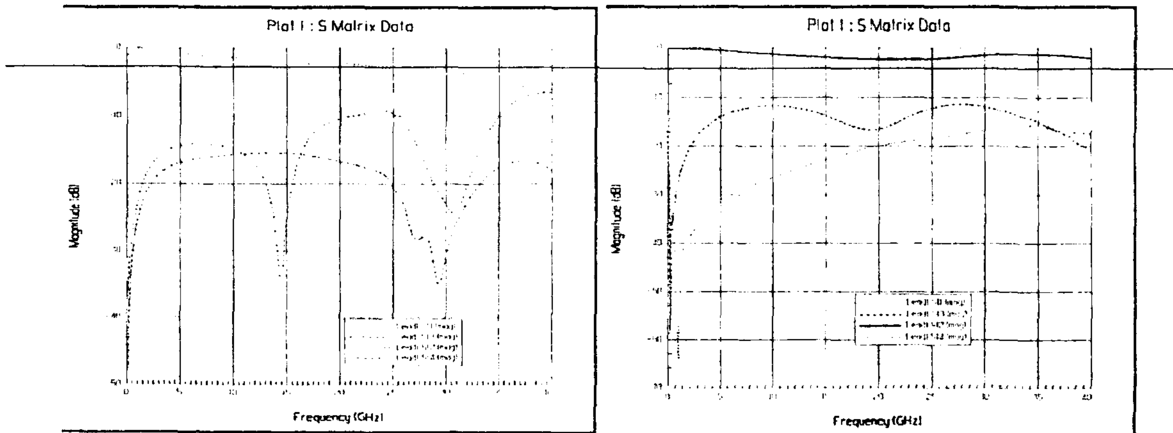




Simulation model FC

The Limitation of Wire bonding for High Speed

- **Simulation Results show the Wire bonding on the MLF package can support up to 20GHz where shows typical -3dB**



Wire bond-MLF FC-MLF

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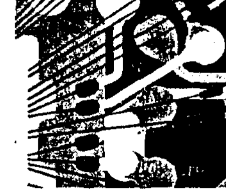
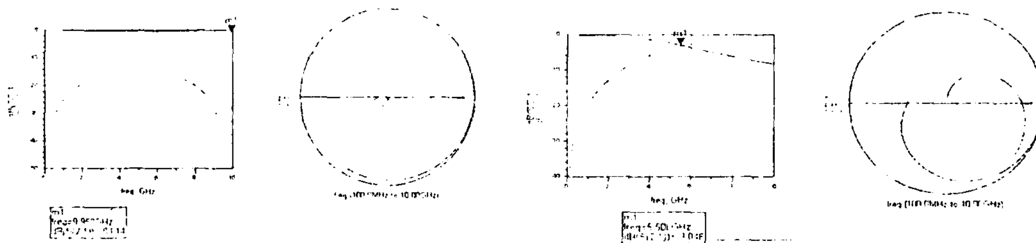
A Possible Low Cost Model for High Speed



- **Not all IO are required High Speed**
  - Find a solution at the Low cost version, If there is only a couple of critical IO
- **Optimization for high Speed IO**

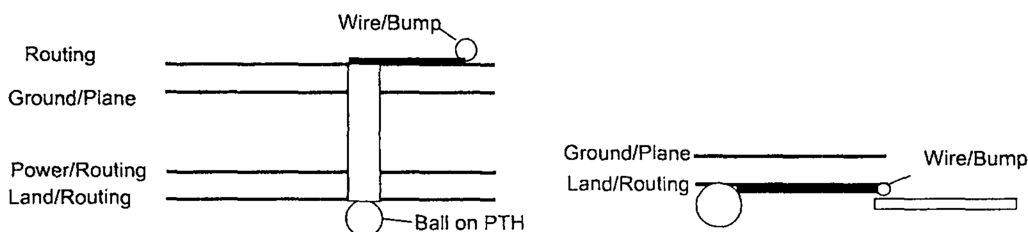
Wirelength:0.58 mm
S_Ball Diameter:630 um
Transmission lines are optimized to 50 Ohms for both bottom and signal top layer.

Wirelength:3.09 mm
S_Ball Diameter:630 um
Transmission lines are optimized to 50 Ohms for both bottom and signal top layer.



Impedance Matching in a Package for High Speed

- **Chip to substrate interconnection, wires or bumps shall be controlled.**
  - Number of wire for GND/PWR should be decided by Impedance consideration
- **Impedance matching between the transmission lines and via.**
  - Changing the via size or adjusting the number of via.
  - Removing the via from the package can be an option.



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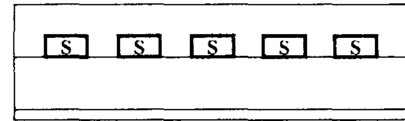
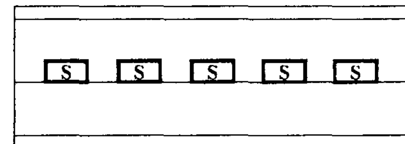
Microstrip/ Strip Line/ CPW for High Speed

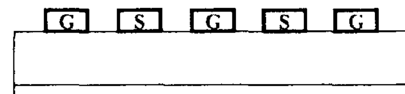
- **Microstrip**
  - Short transmission line
  - Midrange IO chip interconnection
  - Low cost model



- **Stripline**
  - Low signal attenuation
  - High density FC design

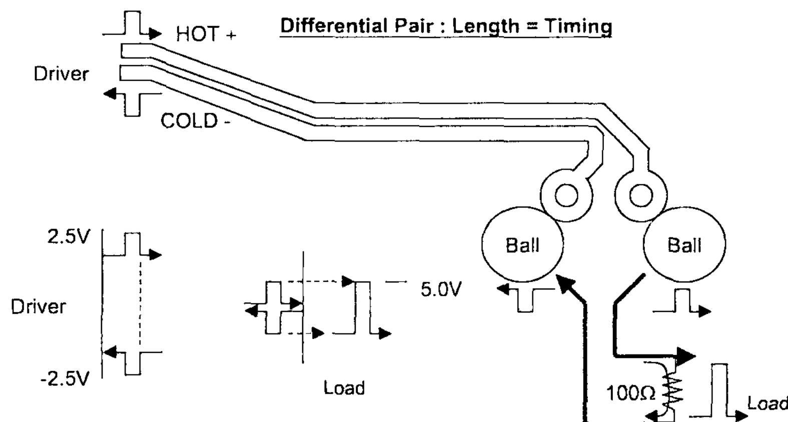


- **CPW(Co-Planar Wave Guide)**
  - Restricted High Speed IO
  - Low cost model
  - Low signal attenuation



LVDS, pairs for High Speed with Low Voltages

- **Impedance for Differential pairs**
  - 100 Ohm for impedance matching
  - Delay need to be controlled by adjusting the skew.



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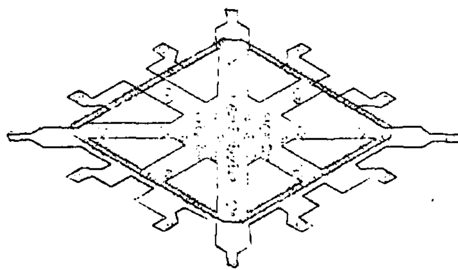
Plane Design for High Speed

- The Role of Ground/Power plane changed from a thermal dissipation path to a capacitance.
- Embedded capacitor will be required to enhance power/ ground stability.
- Number of vias to be used and area separation between.

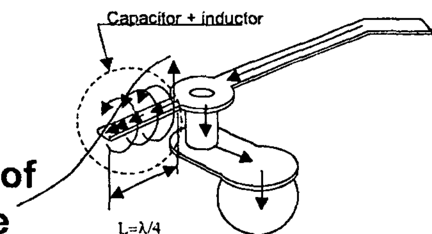


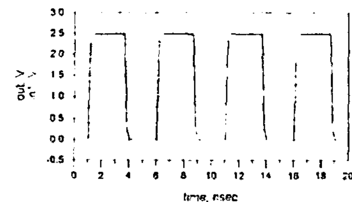
27mm x 27mm 256/272 PBGA

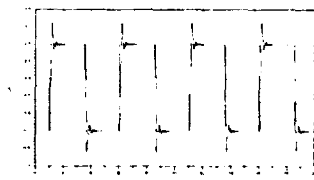
inductance = 0.09 nH

Parasitic structures on Substrates for Manufacturing

- Plating Tails effect should be considered over 10GHz
- Design to minimize the capacitance of solder ball land : via in pad structure
- Wire Bonding / Bump Pad size should be designed to be matched to impedance of wire / bump pad
  - S-parameter analysis.







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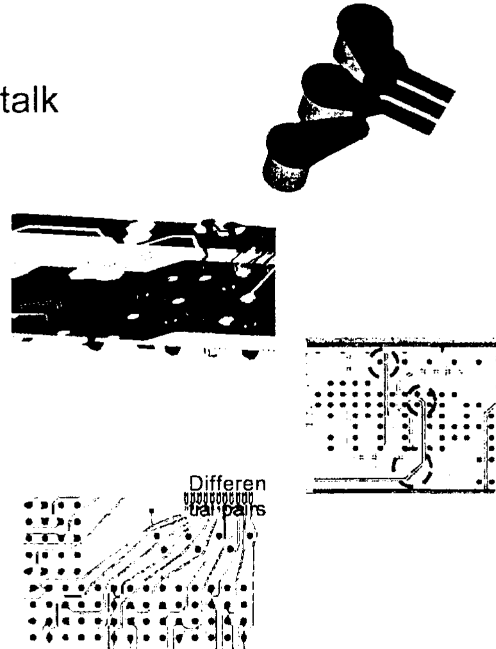
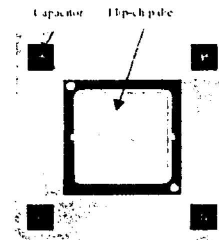
Methods to Reduce the Problem at High Speed

- **Ground Shielding**
  - Capacitive (backward) Crosstalk
- **Power/Ground separation**
  - SSN, Ground bounce
- **Cross Routing**
  - Cross Talk between layers
- **Parallel Routing**
  - EMI for Differential Pair
- **Removing plating Line**
  - Delay, over/undershoot



Methods to Reduce the Problem at High Speed

- **Increasing Stack up Layer**
  - Ground Bounce\ IR Drop\
- **Passive Component**
  - Impedance matching
  - Ground\IR Drop
- **Plating Method Change**
  - Impedance Matching
  - Reduce Reflection
  - Improving Effective Conductivity



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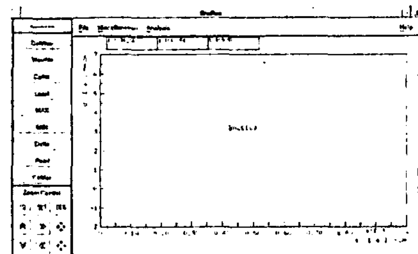
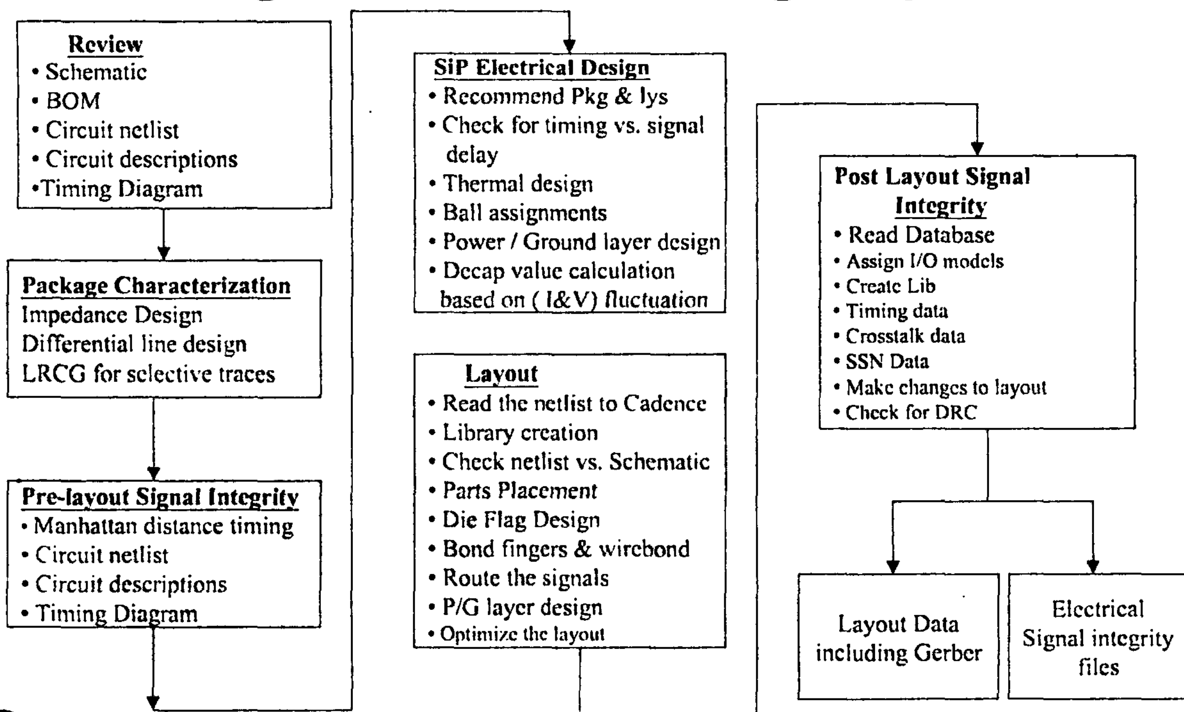
What is required for Design Tool at High Speed

- 2D modeling function for characteristic impedance calculation for transmission line
- Distribution model analysis function
- System Timing Modeling
  - Differential Pair skew constrain function
- Time Domain Analysis
  - Wave form integrity : Real time
- Cross talk Analysis
  - Backward cross talk
  - Forward cross talk
- Power/Ground plane Analysis Tool
  - H-spice/ 3D distributed model



Design Process for High Speed



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Amkor's Approaches for High Speed

- Package Design Optimization for Electrical Performance become most hot issue over emerging GHz up to 100GHz
- High Speed Silicon Device design have to be closely connected to package design from the its design and have to be co-worked for Best performance
- For consumer market surviving, The proper package selection and proper co-developing procedure, based on mutual understanding of electrical information should be setup

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