Analysis of Signal Interference for 3-D Microsystems.

3-D 마이크로시스템을 위한 신호 간섭 분석

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Abstract

In this paper, we explain briefly polysilicon guard layer in a simple 3-D structure. Simulation was performed extensively to see interference and characterize the role of the polysilicon guard layer. Especially, we performed extensively S-parameter simulation to analysis the signal interference. The interference was characterized in terns of oxide thickness, polysilicon doping concentration, thickness, number of contact of polysilicon guard, and metal guard size.

Key Words : Signal Interference, 3-D Microsystems, guard layer, S-parameter

1. Introduction

Silicon CMOS has grown tremendously over the past 25 years due to the excellent scaling properties of MOS transistors. The scaling down of MOS devices has been resulting in consistent improvement in density, performance, and power. Now the gate lengths of MOS transistors are near and well below 50 nm in research and development phase. It seems that CMOS technology will be faced with some physical limits in the near future. Interconnect delays become dominant with the scaling down. In spite of new materials like Cu ad low-k dielectric, interconnect delay is expected to be substantial below 130 nm technology node, thereby severely limiting chip performance. So it is now needed to consider 3-D devices to be scaled 20 nm regime and 3-D integration of the devices so that we can achieve higher density and/or real microsystems. Thus 3-D integration enhances system performance in terms of high speed operation, increased packing density, multi-functional operation, integration of heterogeneous devices/materials [1]- [3]. To achieve such systems, dense and high-bandwidth interconnection technology in intra- ad inter-wafer is imperative.

In this paper, we explain briefly polysilicon guard layer in a simple 3-D structure. Simulation was performed extensively to see interference and characterize the role of the polysilicon guard layer.

2. 3-D Structure and Vertical Interconnect

Fig. 1 shows simple schematic cross-sectional view of the 3-D CMOS structure with 2 device layers, where oxide-to-oxide bonding was assumed. This bonding is very simple, but requires high temperature (800 ℃) anneal to make strong the bonding strength. Therefore any metal layer cannot be used. We consider the cross-talking between bottom and top devices becomes severe as operation frequency goes to high. In this situation, we think the doped polysilicon as shown in Fig. 1 can suppress the

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cross-talking between them and study the role of the polysilicon as a guard with various process parameters. The polysilicon acts as a kind of guard to suppress the interference.

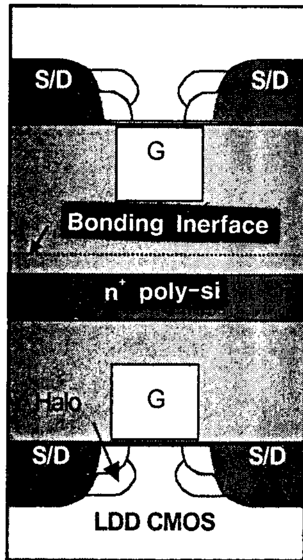


Fig. 1. 3-D structure with 2 device layers. As an example, 2 CMOS device layers are bonded. The poly-Si layer betwen top and bottom devices can block effectively signal interference between them

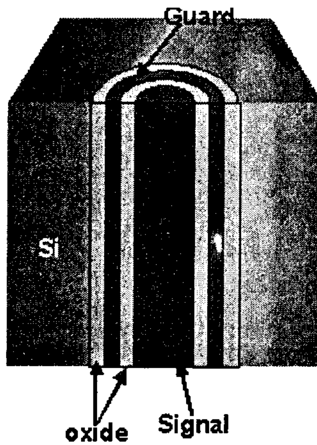


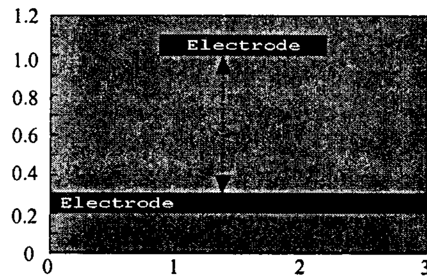
Fig. 2. Schematic cross-sectional view of round -type vertical interconnect. The poly-Si acts as a guard to suppress signal coupling and is used ground electrode to give impedence matching.

Thus the polysilicon can be also applied to vertical signal line as shown in Fig. 2, where the polysilicon can suppress coupling between the signal line and the Si substrate, and also acts as a ground electrode for impedance matching. Here round-type vertical interconnect was assumed and other shape is possible. The guard layer can be implemented by in-situ polysilicon deposition using LPCVD.

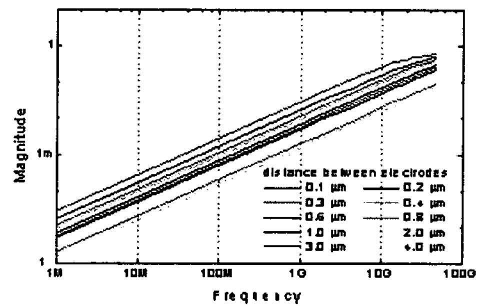
3. Simulation Results

3-1. Signal Interference

We performed device simulations by using SILVACO ATLAS (device simulator). Each structure files includes doping profile, grid, and electrode information. The interference was characterized by the magnitude of S_{21} which is a Scattering parameter. To analyze the effect of signal interference, we chose simple test structure as shown in Fig. 3 (a).



(a)



(b)

Fig. 3. Structure for signal interference. (a) test structure in the unit of ㎛. (b) magnitude of S_{21} as a parameter of dielectric thickness.

The interference was characterized by

conventional 2-D S-parameter simulation. Dielectric material between electrodes is SiO_2 and the thickness of the layer is changed from 0.1 ㎛ to 4 ㎛. Fig. 3 (b) shows the simulated magnitude of S_{21} versus frequency as a parameter of oxide thickness. Basically the interference between electrodes increases as the frequency increases. The magnitude of S_{21} decreases as the dielectric thickness increases. In case of dielectric thickness of 0.1 ㎛, saturation in S_{21} is observed over the frequency range higher than about 10 GHz and will be analyzed other place.

3-2. Characterization of Guard Layer

Also, we have done S-parameter simulation to characterize the polysilicon guard as shown in Fig. 4 in terms of polysilicon guard doping concentration, dielectric thickness, polysilicon guard thickness, contact type, metal guard size.

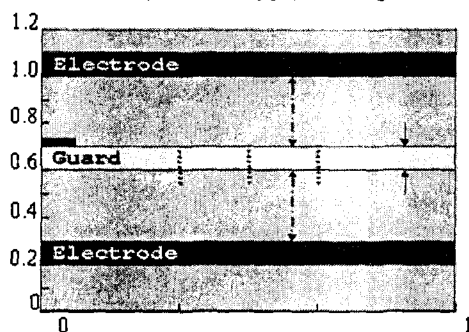


Fig. 4. Test structure to characterize the poly-Si guard layer located in oxide between electrodes. All sizes are in the unit of ㎛.

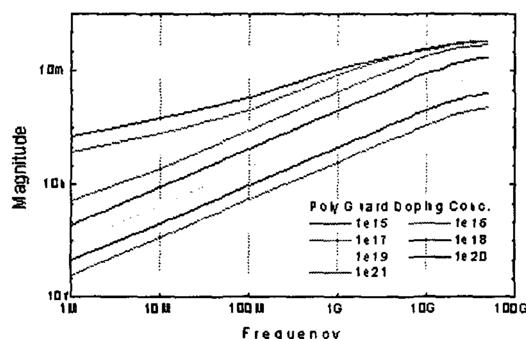


Fig. 5. S_{21} characteristics of poly-si guard in fig.4 versus frequency as a parameter of poly-si concentration

In Fig. 4, the polysilicon guard is located at the oxide layer between electrodes and can suppress signal cross-talking between them. All size are in the unit of ㎛.

Fig. 5 shows the simulated magnitude of S_{21} versus frequency as a parameter of polysilicon guard doping concentration. The doping was changed from 10^{15} cm^{-3} to 10^{21} cm^{-3} with the step of one order magnitude. Magnitude of S_{21} decreases as doping concentration increases over all frequency range. The interference is suppressed significantly with the increase of the polysilicon doping, which means low resistance polysilicon by doping acts as a metal guard. Polysilicon guard doped by 10^{15} cm^{-3} (or 10^{16} cm^{-3}) shows nonlinear characteristics with frequency and may be considered as high resistance of the polysilicon. S_{21} saturation phenomenon and the nonlinear characteristics need to be analyzed in detail and will be shown other place. Fig. 6 shows the simulated magnitude of S_{21} versus frequency as a parameter of dielectric thickness (dash dot type arrow in Fig. 4) between electrode and guard. The polysilicon was doped by 10^{20} cm^{-3}. Magnitude of S_{21} decreases as dielectric thickness increases. The effect of the dielectric thickness is also significant

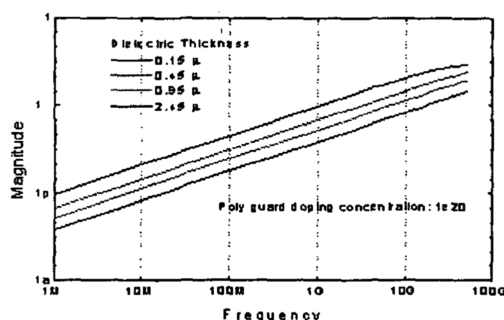


Fig. 6. S_{21} characteristics with frequency as a parameter of dielectric thickness(0.15, 0.45, 0.95, 2.45 ㎛). The poly-Si guard was doped by $1\times 10^{20} cm^{-3}$

In Fig. 7, it is shown the simulated magnitude of S_{21} versus frequency as a parameter of polysilicon guard thickness (solid arrow mark in Fig. 4). The thickness values are 0.1, 0.5, 1,0, 2.0, and 5.0 ㎛ at the fixed doping concentration of 1×10^{20} cm^{-3}. The magnitude of S_{21} decreases as polysilicon guard thickness increases from 0.1 to

0.5 ㎛ (5 increase) due to the reduced resistance. However, polysilicon guard thicker than about 0.5 ㎛ has no significant reduction in S_{21}. From these data, we can conclude thin polysilicon doped heavily can block effectively the interference.

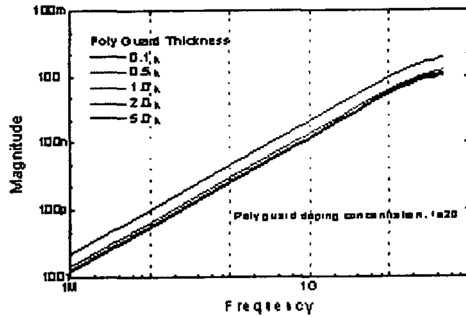


Fig. 7. S_{21} characteristics with frequency as a parameter of poly-si thickness (0.1, 0.5, 1.0, 2.0 and 5.0 ㎛). The poly-Si guard was doped by $1\times10^{20}cm^{-3}$

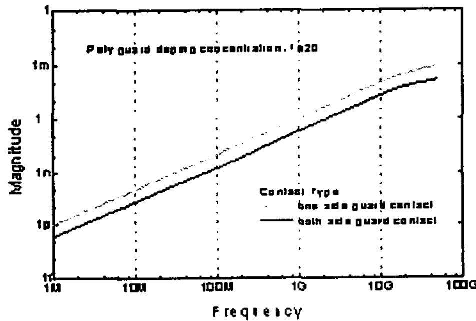


Fig. 8. S_{21} characteristics with frequency as a parameter of contact number. The poly-si guard was doped by $1\times10^{20}cm^{-3}$

S_{21} characteristics with contact number on the polysilicon guard are shown in Fig. 8. In this case, polysilicon doping concentration is 1×10^{20} cm^{-3}. Magnitude of S_{21} decreases as guard contact number increases. Therefore it is needed to make contacts on polysilicon guard as many as possible. The effect of the guard size on the interference is given in Fig. 9. As shown in Fig. 4, white dashed arrow mark stands for the guard size and the sizes are 1.0, 1.5, and 2.0 ㎛. The simulated magnitude of S_{21} versus frequency as a parameter of guard size is shown in Fig. 9. With the increase of the guard size, the interference is improved, but not significant. Anyway to reduce the signal interference, the size of the guard layer needs to be considered.

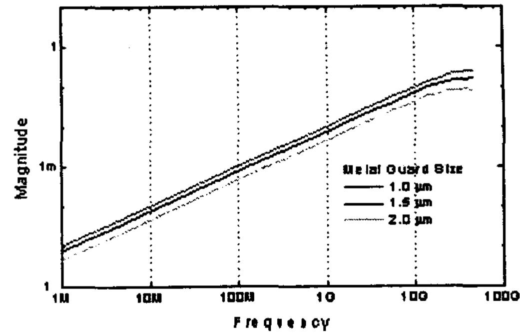


Fig. 9. S_{21} characteristics with frequency as a parameter of guard size(1.0, 1.5 and 2.0㎛) The guard size is represented by white dashed arrow mark in Fig.4.

4. Conclusion.

Simple 3-D structure with two device layers and vertical interconnect structure were explained. Signal interference for 3-D Microsystems has been characterized. We performed extensively S-parameter simulation to analysis the signal interference. The interference was characterized in terms of oxide thickness, polysilicon doping concentration, thickness, number of contact of polysilicon guard, and metal guard size. It was found that the suppression of the interference depend strongly on the concentration of polysilicon guard and the oxide thickness, but not on the polysilicon thickness. Interference was analyzed by using S_{21}. In this work, we focused on passive devices. As future study, it is needed to analyze signal interference for active devices and more complicated structure.

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