Dynamic Characteristic Analysis of SSSC Based on Multi-bridge PAM Inverter

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Abstract -- This paper proposes a static synchronous series compensator based on multi-bridge inverter. The proposed system consists of 6 H-bridge modules per phase, which generate 13 pulses for each half period of power frequency. The dynamic characteristic was analyzed by simulations with EMTP code, assuming that it is inserted in the 154-kV transmission line of one-machine-infinite-bus power system. The feasibility of hardware implementation was verified through experimental works using a scaled model. The proposed system does not require a coupling transformer for voltage injection, and has flexibility in expanding the operation voltage by increasing the number of H-bridge modules.

Keywords -- SSSC (static synchronous series compensator), EMTP (electro-magnetic transients program), TACS (transient analysis of control system), TCSC (thyristor controlled series compensator), STATCOM (static synchronous compensator)

I. INTRODUCTION

Recently two types of series compensator were developed, which can compensate the line reactance in continuous manner using high-power semiconductor devices. TCSC, which consists of several series-connected modules of thyristor-switched capacitor parallel with thyristor-controlled reactor, regulates the line reactance by changing conduction angle of thyristor switches. SSSC, which consists of a voltage source inverter with dc capacitor, regulates the line reactance by injecting a controllable ac voltage.[1]

STATCOM was a first FACTS device using voltage source inverter with GTO, which is connected parallel with the bus needed for compensation. SSSC has same configuration of power circuit as STATCOM, but different configuration in control. SSSC is inserted in a transmission line to control the voltage across the transmission line.[2]

In order to increase operation voltage, FACTS device has an inverter whose pole consists of many GTOs connected in series. However, series connection of GTO brings about many difficulties. Although it is proven technology, still there is a restriction in the maximum allowable number for actual application. Step-down transformers are normally used for properly matching the inverter operation voltage with the power system voltage.

Multi-level inverter was proposed to increase the system operation voltage avoiding series connection of switching devices.[3] But multi-level inverter has complexity in formation of output voltage and requires many back-connection diodes. In order to complement this weak point, multi-bridge inverter composed of 5 H-bridge modules per phase has been proposed for STATCOM application.[4][5]

In this paper an SSSC based on multi-bridge inverter, which is composed of 6 H-bridge modules per phase, is proposed. The formation of output voltage in multi-bridge inverter is described in Section II, based on the output voltage of each module depending on switching status. The operation of proposed system is verified through simulations with EMTP codes, which is described in Section III.[6][7] Experimental results with a scaled model is described in Section IV .

II. MULTI-BRIDGE INVERTER

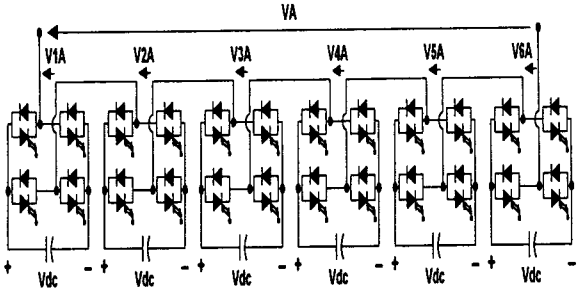
A. Operational Principle

The proposed SSSC consists of 6 H-bridge modules per phase as shown in Fig. 1a. The formation of output voltage can be explained using Fig. 1b. Each bridge has a different duration of conduction so that total output voltage has minimum level of harmonics. Since the dc capacitor is charged with V_{dc}, each module generates output voltage V1A ~ V6A. The output voltage VA is composed of 13 pulses per half period of power frequency. Fig. 1c represents how each module generates the output voltage depending on the switching state. The relationship between switching state and output voltage, whose waveform is shown in the right side of Fig. 1c, can be summarized in Table 1. Fig. 1d shows a calculation method of firing angle θ_1-θ_6 to minimize the harmonic level of output voltage by making the output waveform close to be sinusoidal. In this figure θ_6 was selected as an example.

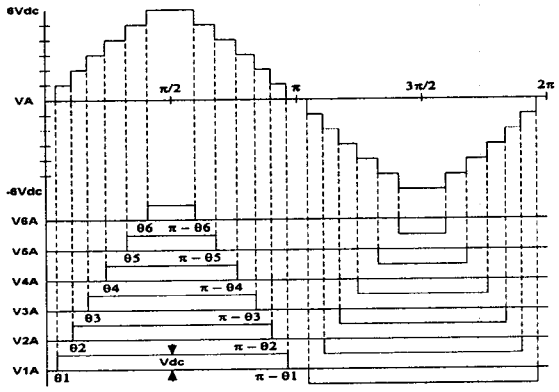
Table 1. Switching state of H-bridge inverter

V1A	Switching State
V_{dc}	S1, S4 : ON & S2, S3 : OFF
0	S1, S3 : ON & S2, S4 : OFF S2, S4 : ON & S1, S3 : OFF
$-V_{dc}$	S2, S3 : ON & S1, S4 : OFF

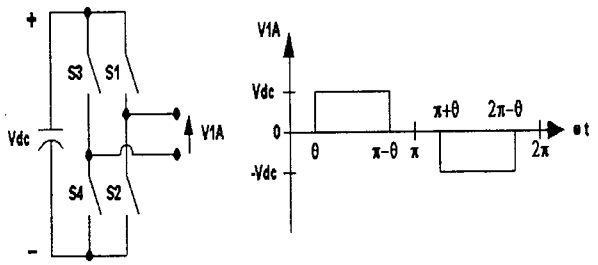
The basic principle to make the area of output waveform same as the area of ideal sinusoidal waveform can be explained as the following. Using the expanded graph, the value of θ_A and θ_B can be calculated from the known values of segment AB, which is obtained by the number of H-bridge modules.



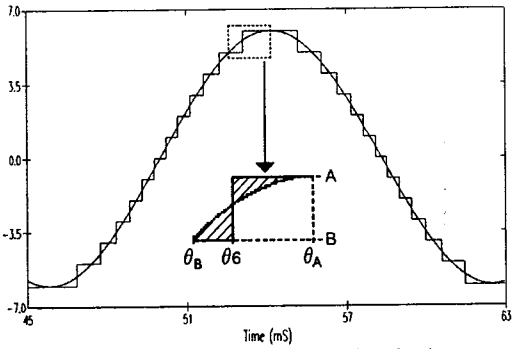
(a) multi-bridge inverter



(b) principle of building output voltage



(c) Switching pattern and output



(d) Calculation method for harmonic reduction

Fig. 1. Principle of multi-bridge inverter operation

The θ_6 can be calculated by the following equation, if both scratched areas are equal.

$$\int_{\theta_B}^{\theta_6}(\sin\theta - B)d\theta - \int_{\theta_6}^{\theta_A}(A - \sin\theta)d\theta = 0 \qquad (1)$$

By arranging equation (1), the following equation is obtained.

$$\theta_6 = \frac{A\theta_A - B\theta_B + \cos\theta_A - \cos\theta_B}{A - B} \qquad (2)$$

From equation (2), θ_A and θ_B can be obtained as the following equation.

$$\theta_A = \sin^{-1} A\,, \quad \theta_B = \sin^{-1} B \qquad (3)$$

Generalizing equation (2), the following equation can be obtained.

$$\theta_n = \left(n\theta_{\frac{n}{M}} - (n-1)\theta_{\frac{n-1}{M}}\right) + M\left(\cos\theta_{\frac{n}{M}} - \cos\theta_{\frac{n-1}{M}}\right) \qquad (4)$$

where, $n = 1, 2, \mathrm{K}\ , 6 \quad A = \frac{n}{M} \quad B = \frac{n-1}{M}$

M is the number of H-bridge modules, which is 6 for the proposed system.

B. Conceptual System Design

Implementing the multi-bridge inverter using currently commercialized GTO, the maximum rating for single H-bridge module without series connection of GTO can be roughly calculated as the following.

Rated DC voltage : $V_{dc} \cong 5\text{kV}$
Rated output voltage : $V_o \cong V_{dc} \cong 5\text{kV}$
Rated power : $S \cong 1/2 \cdot V_{dc} \cdot 2\text{kA} \cong 5\text{MVA}$

The above rating is too low to apply one module directly for FACTS devices. Therefore, series connection of inverter modules is indispensable. Since the proposed multi-bridge inverter has 6 H-bridge modules, the system rating is calculated as the following.

Rated DC voltage: $6 \cdot V_{dc} \cong 30\text{kV}$
Rated output voltage: $V_o \cong V_{dc} \cong 30\text{kV}$
Rated power: $S \cong 3 \cdot V_{dc} \cdot 2\text{kA} \cong 30\text{MVA}$

The above rated output voltage is about 33.74% of the phase voltage in 154-kV transmission line. This voltage is enough for satisfying the operation voltage of FATCS devices to be applied for the actual transmission line.

III. EMTP SIMULATION

A. Simulation Model

In order to analyze the operation of proposed SSSC based on multi-bridge inverter, computer simulations with EMTP code were performed.

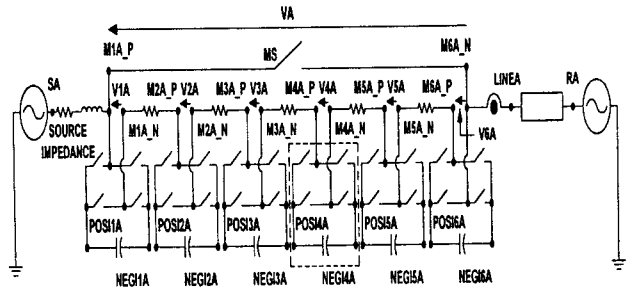


Fig. 2. Simulation model for whole system

Fig. 2 shows a single-phase simulation model for the whole system. Other phases have same configurations. The power system is represented by one-machine-infinite-bus. The transmission line is modeled with a reactor considering only lumped line reactance. The circuit parameters used in the simulation are shown in Table 2.

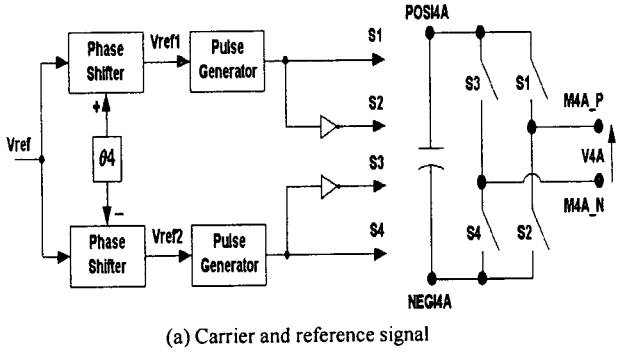
Table 2. Simulation line parameter

L/L voltage	154[kV]
Base power	160[MVA]
Source frequency	60[Hz]
Line inductance	98.15[mH]
Power angle	30°

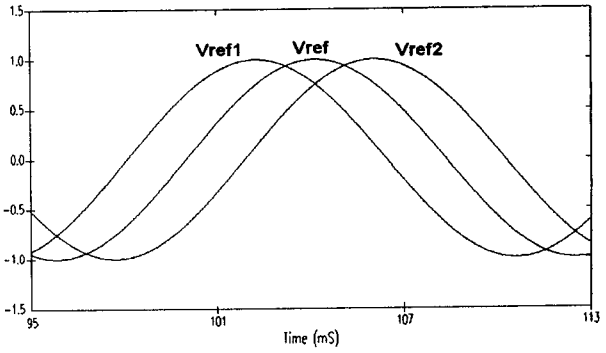
B. Gate Pulse Generation

Fig. 3 shows a principle of gate pulse generation for multi-bridge inverter. Fig. 3a shows procedure to generate gate pulses from the reference value of injecting voltage. As shown in Fig. 3b, two other reference voltages V_{ref1} and V_{ref2} are produced through leading and lagging V_{ref} signal by θ_4. These two signals are used to generate gate pulses for supplying turn-on signals to switch S1 and S4 in the inverter module. Other turn-on signals are obtained, passing these two signals through NOT logic for switch S2 and S3. Four gate pulses generated through the above procedures are shown in Fig. 3c.

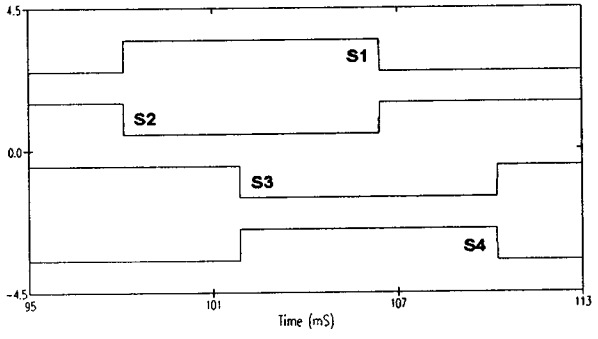
Four sets of gate pulse for other 3 sets of H-bridge module are generated using similar procedures through leading or lagging V_{ref} signal by θ_1, θ_2, and θ_3. Fig. 3d shows output voltage of V4A in per unit together with V_{ref} by supplying gate pulses shown in Fig. 3c.



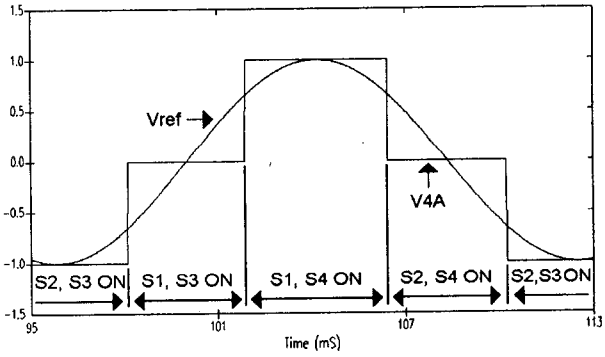
(a) Carrier and reference signal



(b) Gate pulse generation scheme



(c) Gate pulse and inverter output



(d) V4A and V_{ref} waveform

Fig. 3 Principle of gate pulse generation

C. Controller Structure

Fig. 4 shows a controller used for simulation of the proposed SSSC based on multi-bridge inverter. Since each H-bridge module has a separate dc capacitor, separate control is needed for each phase.

The line current is measured and sent to the phase-lock loop and the phase-lock loop generates angle signal θ synchronized with the line current. The angle θ is properly adjusted for each phase. The reference value of compensating voltage V_q^* is multiplied by gain K to calculate the reference dc voltage V_{dc}^*. V_{dc}^* is compared with the actual dc capacitor voltage of each

phase separately. The error voltage is passed through PI controller and limiter to obtain the firing angle, which is corrected by phase-lock angle θ. The value of V_{dc}^* was determined by 9.2kV. The measured dc voltage is calculated by averaging dc voltages of 6 H-bridge modules. The output signal of PI-Controller is multiplied with the mode sign of V_q^*. The mode sign is used to determine SSSC operation in C-mode or L-mode. The mode sign is +1 for C-mode and –1 for L-mode. C-mode means that the phase angle of injected voltage is leading to that of the line current, while L-mode means that the phase angle of injected voltage is lagging to that of the line current.

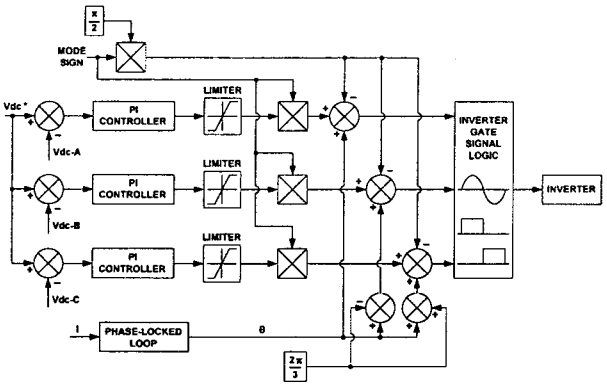
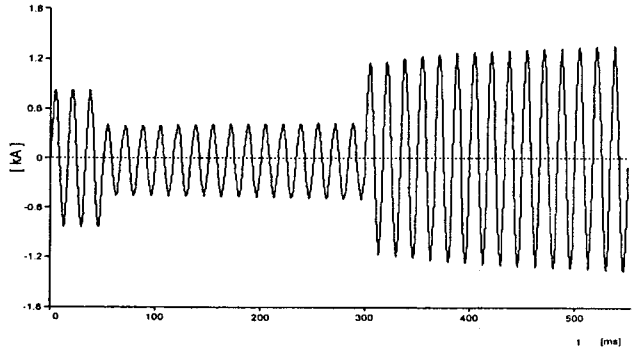


Fig. 4. Simulation controller

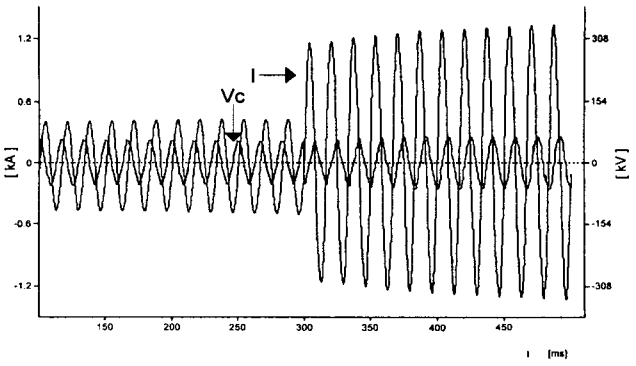
Synchronized signal with the 3-phase line current, control signal for the dc capacitor voltage, and the mode sign are combined together to generate the reference signal for inverter firing angle. There are 6 sets of controller shown in Fig. 4, in order to supply all the gate signals for 3 sets of 6 H-bridge modules.

D. Simulation Results

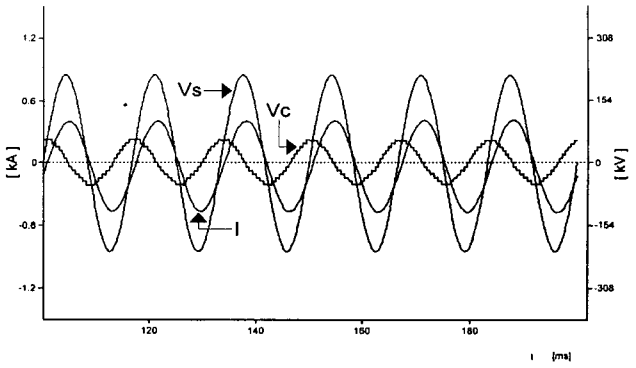
The scenario considered in this simulation is as the following. SSSC is on standby mode from 0~50ms. The mechanical switch MS is ON-state and all the switches in multi-bridge inverter are OFF-state. During 50ms~300ms the mode sign is set by –1 and SSSC operates in L-mode. During 300ms~550ms the mode sign is set by +1 and SSSC operates in C-Mode.



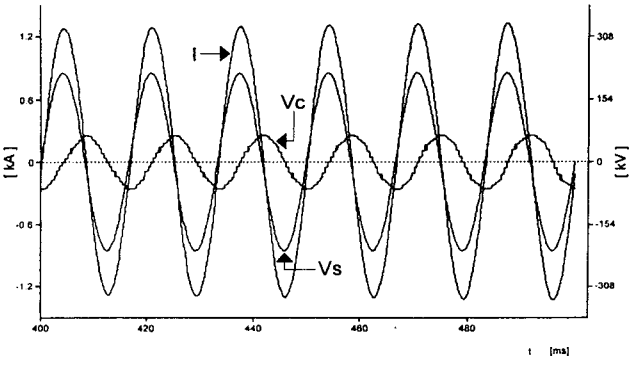
(a) line current



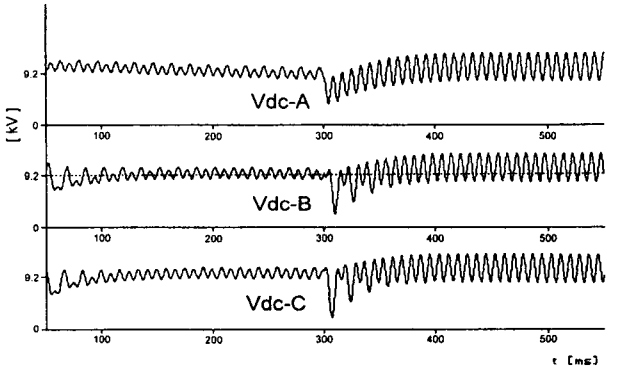
(b) inverter voltage and line current



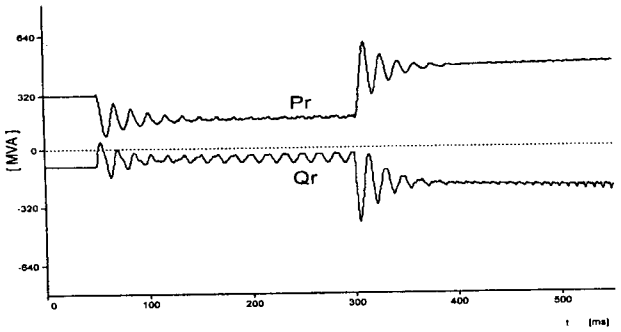
(c) source voltage, inverter voltage, and line current in L-Mode



(d) source voltage, inverter voltage, and line current in C-Mode



(e) DC capacitor voltage



(f) active and reactive power in receiving point

Fig. 5. Simulation results

Fig. 5 shows simulation results for dynamic characteristic analysis of the proposed SSSC. Fig. 5a shows the line current variation during simulation time. The line current decreases in L-mode and increases in C-mode compared with that in standby mode. Fig. 5b shows the inverter injection voltage and the line current during transition from L-mode to C-mode. The transition is completed within half cycle of power frequency.

Fig. 5c shows the source voltage, the inverter injection voltage, and the line current when SSSC operates in L-mode, whose equivalent line reactance is 139.4[mH]. Fig. 5d shows the source voltage, the inverter injection voltage, and the line current when SSSC operates in C-mode, whose equivalent line reactance is 57.9[mH].

Fig. 5e shows the DC capacitor voltages measured, which have very similar shape for each phase. Fig. 5f shows the variations of active power P_r and reactive power Q_r at the receiving end. Transmission line supplies the active power of 320[MW] and the reactive power of -85[Mvar] when SSSC operates in standby mode. The active power decreases down to 166.4 [MW] and the reactive power decreases down to –29.1[Mvar] in L-mode respectively. The active power P_r increases up to 467.2[MW] and the reactive power increases up to –162.7 [Mvar] in C-mode respectively.

IV. SCALED-MODEL EXPERIMENT

A hardware scaled-model has been built to confirm the simulation results and to verify the feasibility of actual system implementation. For the convenience of experiment, it is considered that the multi-bridge inverter has only 4 H-bridge modules per phase. Fig. 6 shows the circuit diagram for the scaled model, which has 16 single-type IGBT units per phase. TMS320C31 was used for whole system control and pulse generation. The reference for gate pulse generation was determined by detecting zero-cross point of the line current. The firing angle of each inverter module is determined with respect to this reference. The dc voltage of each inverter module is controlled independently. Table 3 shows circuit parameters for the scaled model.

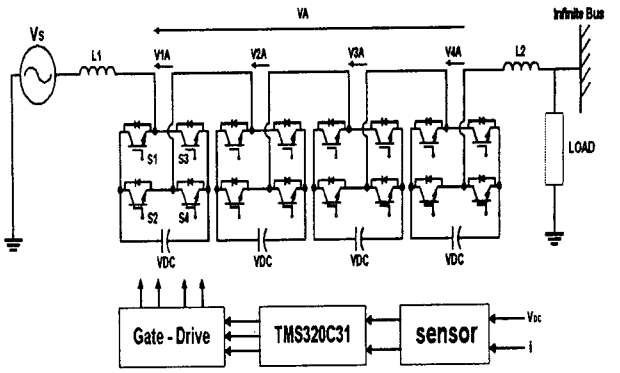
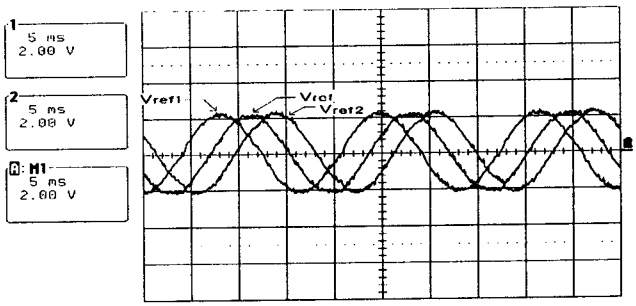


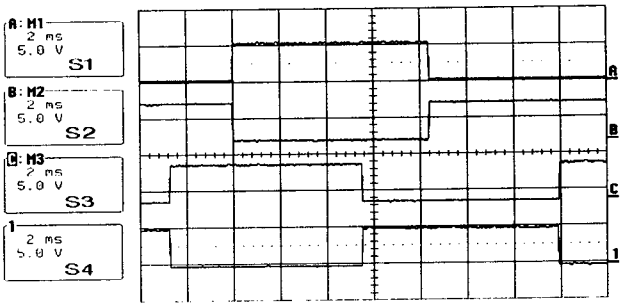
Fig. 6. Hardware configuration of scaled model

Table 3. Scaled model circuit parameters

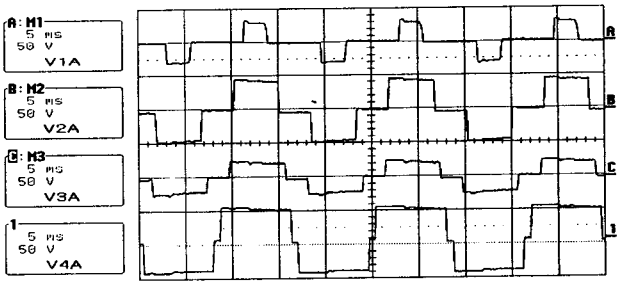
Source voltage	100[V]
Line model L_1	20.9[mH]
Line model L_2	40[mH]
Load	30[Ω]
DC link capacitor	2200[μF]



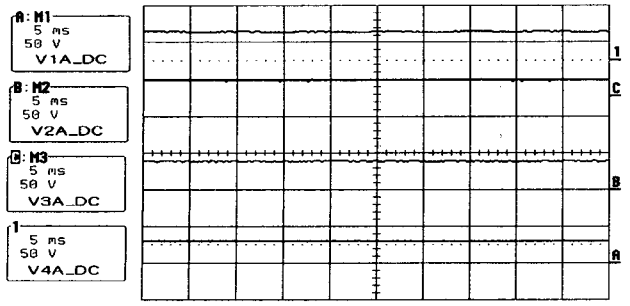
(a) reference value of injecting voltage



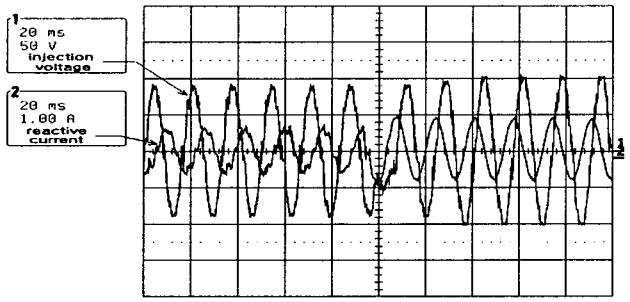
(b) gate pulse for each switch in one module



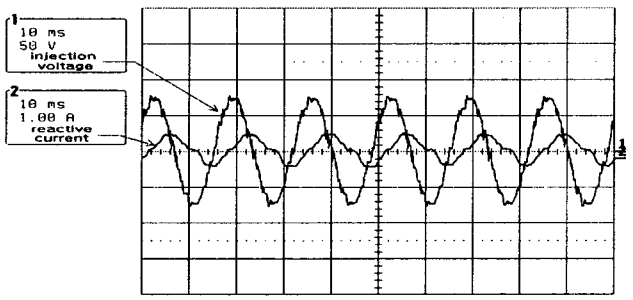
(c) output voltage waveform of each module



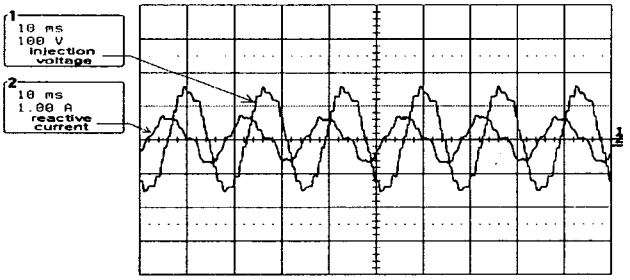
(d) dc capacitor voltage of each module



(e) injecting voltage and reactive current



(f) injecting voltage and reactive current(lag)



(g) injecting voltage and reactive current(lead)

Fig. 7. Experimental results with scaled model

Fig. 7 shows the experimental results for the scaled model of the proposed SSSC. Fig 7a shows the reference value of injecting voltage, which generates gate pulses for each inverter module. Fig. 7b shows 4 gate pulses to be supplied for the switches in one inverter module. Fig. 7c shows the output voltage of each inverter module respectively. The waveforms are very similar to the simulation result. The differences are due to the losses in the H-bridge modules.

Fig. 7d shows the variation of dc capacitor voltage, in which each voltage is almost equally distributed. This means that the controller operates properly. Fig. 7e shows the variations of injecting voltage and reactive current, when the proposed SSSC has a sudden state change from supplying lagging reactive power to supplying leading reactive power. Transition from the lagging to the leading state can be completed within one cycle of power frequency. Fig 7f shows the expanded waveform of Fig. 7e in L-mode, while Fig. 7g shows the expanded waveform of Fig. 7e in C-mode. These results verify that the proposed SSSC operates properly.

V. CONCLUSION

This paper proposes an SSSC based on multi-bridge inverter, which is composed of 6 H-bridge modules per phase. Dynamic characteristic for the proposed system was analyzed through simulations with EMTP code. The feasibility of hardware implementation was verified through experimental works using a scaled model.

The proposed system has flexibility in matching the operation voltage with the power system voltage by adding or subtracting the number of H-bridge modules. It can be directly inserted into the transmission line without coupling transformer. The developed simulation model could be useful to obtain many design data for the actual hardware system.

VI. REFERENCES

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