Suppression of Harmonics of Multi-Level Converter applied for Back-to-Back HVdc Link

Noriyuki Kimura, Akira Kouno, Toshimitsu Morizane, Katsunori Taniguchi
Osaka Institute of Technology
Ohmiya 5-16-1, Asahi-ku, Osaka, Japan 535-8585

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INTRODUCTION

This paper proposes to use a multilevel converter configuration for back-to-back (BTB) HVdc Link. Multilevel converter (MLC) configuration [1], which is enhanced from the neutral point clamped converter [2], can avoid series connection of the switching device in one valve, or at least can reduce the number of the series connected switching device. Smaller number of the series connected switching devices allows to adjust the switching characteristics and to reduce the capacitance of the snubber circuit. Smaller snubber capacitance means smaller snubber loss. MLC also can reduce higher harmonics while keeping switching frequency at the lowest, that is fundamental frequency. However, it is known that maintaining constant dc voltage of each dc side capacitor is difficult for a MLC [3,4]. Analysis including the loss of the converter is performed by the authors, and the results show that the condition required to stabilize the capacitor voltage for single MLC with one pulse operation is difficult to be satisfied [5,6]. Hence the authors propose to use double converter configuration as a BTB HVdc link.

In this paper, we have investigated nine and eleven level converters. First, we show the basic characteristics of nine level converter, and we discuss about the method to eliminate higher harmonic components and coordination with voltage and power control. Then we show the computer simulation research for the steady state and the transients.

2. NINE LEVEL CONVERTER

Figure 1 shows the circuit of 3 phase 9 level converter.

Figure 2 shows the output voltage of the converter in U-phase voltage. Pulse widths θ_{pi} and θ_{ni} (i=1 to 4) are half the duration of the output voltage of each level. Assuming that $V_{cp1}=V_{cp2}=\ldots=V_{cn2}=V_{cn1}=V_{dc}/8$ and $\theta_i = \theta_{pi} = \theta_{ni}$, the amplitude of each harmonic component the Fourier expansion is expressed as following equation.

$$A_n = \frac{2V_{dc}}{n\pi}\sin\left(\frac{n\pi}{2}\right)\frac{1}{4}\sum_{i=1}^{4}\sin n\theta_i \qquad \ldots(1)$$

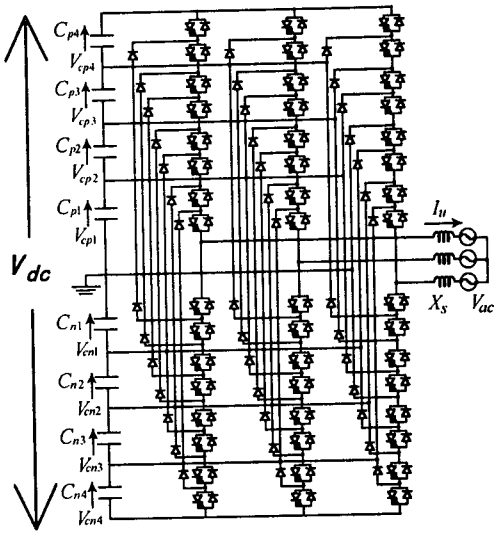

Fig.1 Circuit configuration of 9-level Converter

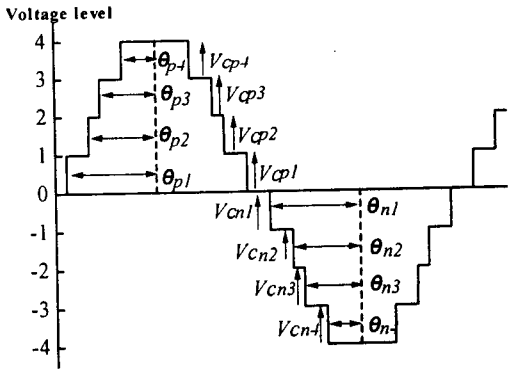

Fig.2 Output Voltage Waveform of 9-level Converter

From eq. (1), rms. value of the output voltage of the MLC, V_{con}, is expressed as eq. (2).

$$V_{con}=\frac{\sqrt{6}}{\pi}V_{dc}M \qquad \ldots(2),$$

where M is the modulation factor and is determined as $M=\frac{1}{4}(\sin\theta_1+\sin\theta_2+\sin\theta_3+\sin\theta_4)$. And, M cannot be unity since it is necessary that the condition, $90[\text{deg.}]>\theta_1>\theta_2>\theta_3>\theta_4>0[\text{deg.}]$, is satisfied.

2.1 Generation of switching signal

Generation method of switching signal is shown in Fig.3. 3 phase sinusoidal signals, synchronized to the system voltage, V_u, V_v, V_w are generated. Switching pulses are generated by comparing these sinusoidal signals with the reference voltage V_{p4}~V_{n4}. The phase of the output voltage of the converter can be changed by changing the phase of V_u, V_v, V_w The reference voltage V_{p4}~V_{n4}. are calculated from the pulse width order θ_{pi} and θ_{ni}as follows.

$$V_{pi} = \cos\theta_{pi} \qquad V_{ni} = -\cos\theta_{ni} .$$

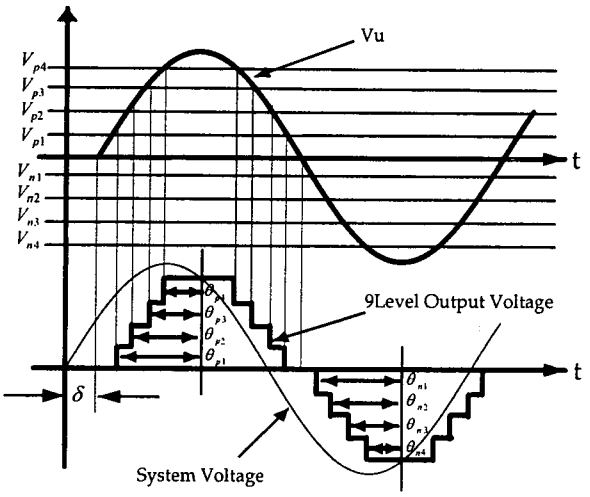

Fig.3 Control Voltage (Vu) and output voltage waveform of 9-level converter

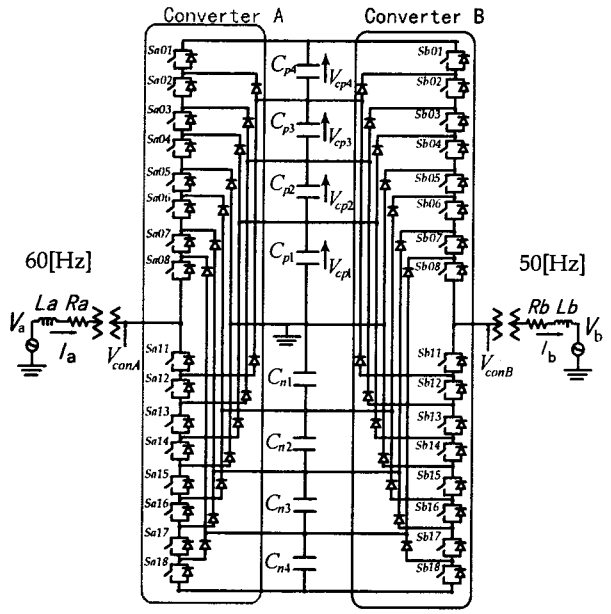

Fig.4 One line Diagram of 9-level BTB system

2.2 Charge and discharge of dc capacitor

The MLC is connected to the system via the AC reactor (ACL). The average current of each DC capacitor is expressed as eq.(3) by neglecting the resistance of the ACL.

$$I_{Ci} = \frac{\sqrt{6}V_{ac}}{\pi X_S}\sin\theta_i \sin\delta \quad ...(3)$$

here, $\theta_i = \theta_{pi} = \theta_{ni}$. δ is the phase difference beween the system voltage and the output voltage of the MLC. When δ is positive, the DC capacitor is discharged and is charged when δ is negative. The current depends on each pulse width θ_i as seen from eq.(3). This fact means that each pulse width of the output voltage of the MLC must be the same to keep the voltage balance of the DC capacitors for single converter configuration. The shape of the output voltage has to be that of a 3-level neutral point clamped converter. To solve this problem, authors have proposed to use double converter configuration as shown in Fig.4 [3]. In this configuration, one converter, named A, controls DC voltage and another converter, named B, controls output real power. Both converters can generate or consume reactive power independently. Phase and pulse widths of each converter may be controlled for that purpose and for the suppression of the harmonics.

3. SUPPRESSION OF HIGHER HARMONICS

The staircase voltage waveform such as Fig.3 is expected to be able to suppress the higher harmonics. The authors investigated the conditions necessary to suppress the higher harmonics and propose the control method of the fundamental voltage amplitude for the BTB system.

3.1 Nine level converter

Nine level converter is expected to be able to eliminate 5th, 7th and 11th harmonic component while generating arbitrary output voltage in fundamental component, that is the modulation factor M. This means $A_5=A_7=A_{11}=0$ at arbitrary A_1 of eq.(1). Controller of harmonic suppression needs a set of pulse width of each voltage level corresponds to the ordered M. We have calculated these sets of pulse width numerically by the computer. Each pulse width changed with 0.2 degree step. A set of pulse width is accepted as the solution of above equations, if the following condition is satisfied.

$$\frac{|A_n|}{A_1} \times 100 < 0.2[\%]; n = 5,7,11 \quad ...(4)$$

The calculated results are shown in Fig.5 as markers. In some part of the modulation factor, there is no solution. To have a set of pulse width continuously for any arbitrary modulation factor, M, between 0.65 and 0.85, we use the following approximated 4th order equation.

$$\theta_n[\text{deg}] = a_{n0} + a_{n1}M + a_{n2}M^2 + a_{n3}M^3 + a_{n4}M^4 \quad ...(5)$$

The coefficients of eq.(5) for the pulse width of each voltage level are shown in Table 1.

The lines in Fig.6 show the theoretically expected amplitude of higher harmonic component of the output voltage of the MLC. Markers denote the results of Fourier analysis of the steady state simulation performed in the section 5.

Table 1 Coefficients of equation (4)

	θ1	θ2	θ3	θ4
an0	7022.4	-3696.9	2554.7	-1851.4
an1	-40221	21595	-13531	9809.5
an2	86170	-47152	27111	-19096
an3	-81181	45940	-24181	16303
an4	28444	-16732	8182.6	-5107.6

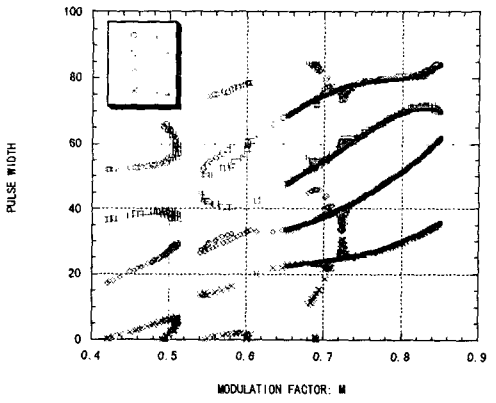

Fig.5 Pulse width pattern of 9-level converter suppressing 5,7,11th harmonics and approximated line

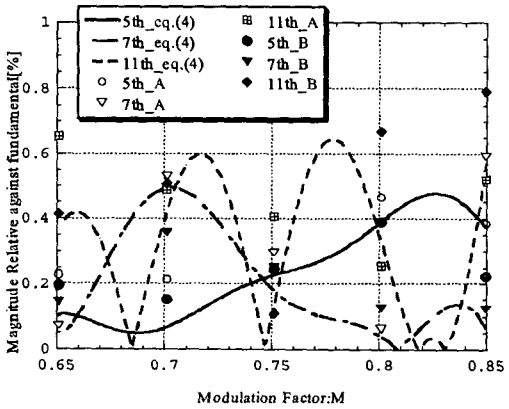

Fig.6 Harmonics of equation (4) and BTB simulation result

3.2 Eleven level converter

To eliminate 13th harmonic component, authors investigated to increase the number of level to 11. The same procedure to determine the pulse width set as for the 9-level converter was taken.

The results of calculated sets of pulse widths are shown in Fig.7 as markers. It is seen that there is a large discontinuity along the modulation factor around M= 0.7. Approximated equation is used to determine the set of pulse width for the ordered modulation factor, M.

The lines in Fig.8 show the theoretically expected amplitude of higher harmonic component of the output voltage of the 11 level converter. Markers denote the results of Fourier analysis of the steady state simulation performed in the section 5. Large amount of harmonic generation near discontinuity occurs when approximated equation is used. Solving this difficulty by increasing the number of level has some problems, such as the increase of the cost in parallel clamping diodes and decreasing the controllability of the voltage balance in dc capacitors.

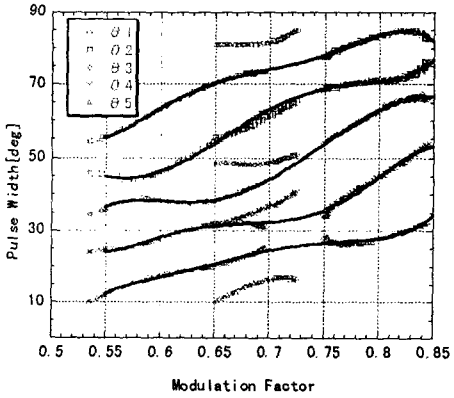

Fig.7 Pulse width pattern of 11-level converter for suppressing 5,7,11,13th harmonics and approximated line

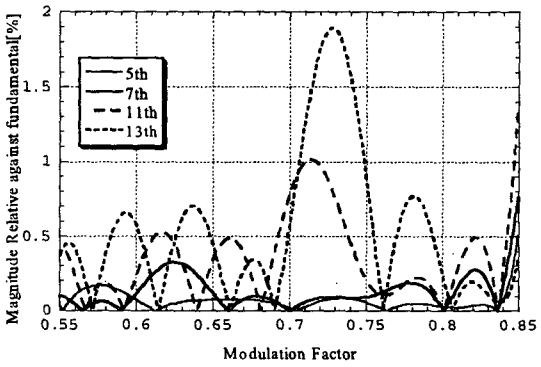

Fig.8 Harmonics of and approximated equation

3.3 Nine level converter with partial three pulse

Authors investigated to use multi-pulse in the highest and lowest level only to eliminate 13th harmonic component. The output voltage shape is shown in Fig.9.

The same procedure to determine the pulse width set as for the 9-level converter was taken. Calculated sets of pulse width are shown in Fig.10. The solutions exist continuously between 0.63 and 0.87 in modulation factor M.

Approximated equation is also used to determine the set of pulse width for the ordered modulation factor, M. The lines in Fig.11 show the theoretically expected amplitude of higher harmonic component of the output voltage of the 9 level with partial 3-pulse converter. Markers denote the results of Fourier analysis of the steady state simulation performed in the section 5. Each harmonic component is suppressed almost less than 1%. Using 3 pulses in two levels show the satisfactory results.

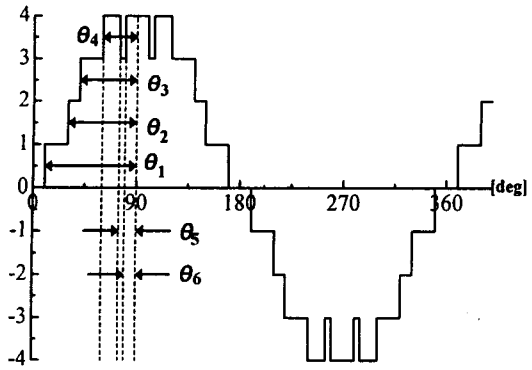

Fig.9 Output voltage waveform of 9-level 3pulse

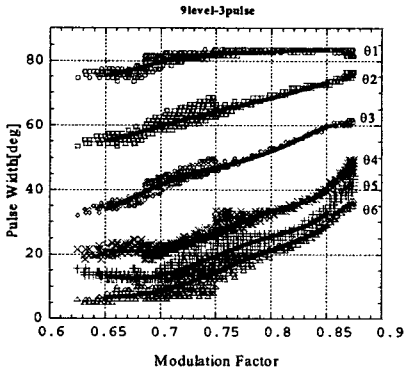

Fig.10 Pulse width pattern of 9-level 3pulse converter for suppressing 5,7,11,13th harmonics and approximated line

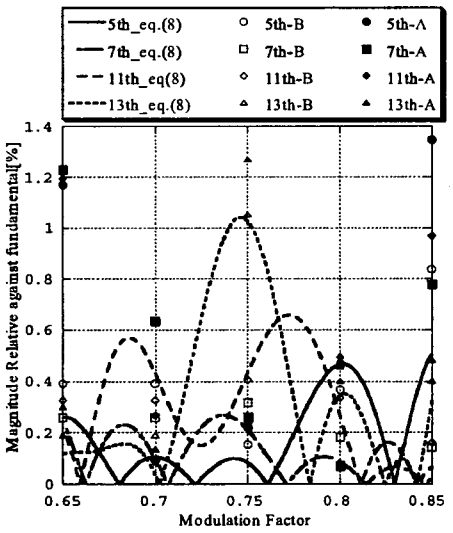

Fig.11 Harmonics of approximated equation and BTB simulation result

4. CONTROLLER OF MULTI LEVEL CONVERTER

The BTB system using MLC must have the real power control, the reactive power control, the total dc voltage control and the capacitor voltage balance control. Two converters share these controls as shown in Table 2.

Table 2 Control System of Converter

Control Parametre	ConverterA	ConverterB
Modulation Factor	Reactive Power	Reactive Power
Phase Difference	Total DC Voltage	Real Power
Pulse Width	Capacitor Voltage Balance	Harmonics

Figure 12 shows the real power control in the converter B and the total dc voltage control in the converter A. Error signal changes the frequency of the control voltage signal shown in Fig.3. The phase angle is changed as the integration of the frequency difference between the control voltage and the system voltage.

Authors propose to add the extra signal from the phase order of the converter B to the total dc voltage control, which uses the phase order of the converter A, to improve the response of . the total dc voltage control when the order of the real power control is changed.

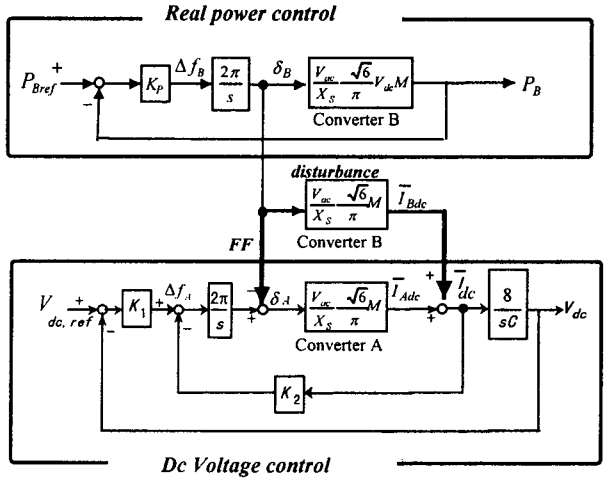

Fig.12 Block diagram of real power and dc voltage controller

The capacitor voltages are compared in the different three categories. Error signals of each voltage level are generated as eq.(6)-(8).

$$\Delta A_{PN} = K_3\left(V_{cp} - V_{cn}\right) \quad ...(6)$$

$$\Delta A_{P12} = \left(K_4 + \frac{K_5}{s}\right)\left(V_{cp34} - V_{cp12}\right) \quad ...(7)$$

$$\Delta A_{P1} = \left(K_4 + \frac{K_5}{s}\right)\left(V_{cp2} - V_{cp1}\right) \quad ...(8)$$

Pulse width θ_1 is determined by the following equation for example. Similar equation is used for other pulse width.

$$\sin\theta_{P1} = \sin\theta_{1ref} + \left(\frac{\delta_A}{\delta_A^2 + k}\right)\left(\frac{1}{4}\Delta A_{pn} + \frac{1}{2}\Delta A_{p12} + \Delta A_{p1}\right) \quad ...(9)$$

It must be noted that modulation factor, M, is not

changed by the DC voltage balance.

The reactive power controller in both converter A and B is the simple P-I controller. Error signal changes the modulation factor, *M*.

5. SIMULATION

Computer simulations using Alternative Transient Program (ATP) are performed. Rated power of the converter is set to be 100MW.

Table 3 Simulation Parameters

Line-to-line Voltage	245[KV]	
Total DC Voltage	400[KV]	
ACL	0.1[H],1[Ω]	
DC Capacitance	1000[μF]	
Rated Power	100[MVA]	
Transformer	System-Y	Converter-Δ
Transformer Ratio	0.577	1

5.1 Steady State Simulation

Steady state simulations are performed by setting the modulation factor to be 0.65,0.7 ,0.75,0.8 and 0.85. The results of Fourier analysis of the output voltage of the 9-level and the 9-level with partial 3-pulse converter are shown in Fig.6 and 11, respectively. Good coincidence with the theoretical calculation is seen.

5.2 Simulation of Power Flow Inversion

The simulation results of power flow inversion for the 9-level with partial 3-pulse converter are shown in Fig.13. The real power order of converter B is started to increase at 1 sec. and increased from -100MW to 100MW in ramp shape within 0.2 sec. Reactive power order is kept to be zero throughout the simulation.

These results show substantially quick response in real power control. They also show good stability in DC voltage balance. Comparison of the response of the total DC voltage controller with and without the feed-forward (FF) signal from the real power controller is shown in Fig.14. Change of the dc capacitor voltage with the FF signal is less than 5% and the error of reactive power output is 1/5, compared to the response of the control system without FF.

CONCLUSION

The authors have investigated the control method of the BTB system using multilevel converter to suppress the harmonics. Sets of the pulse width to eliminate the higher harmonic components are numerically calculated. Higher harmonic components of 5th, 7th, 11th and 13th of the 9-level with partial 3-pulse converter is expected to be almost less than 1%. Steady state simulation results using ATP also verify these expected effects. Simulation results of power flow inversion using ATP verify the effectiveness of the proposed control method.

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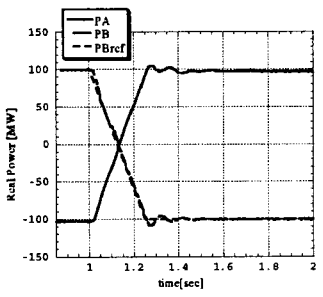
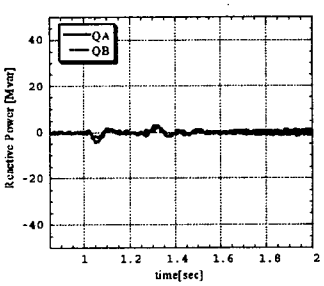


(a) Real Power



(b) Reactive Power

Fig.13 Simulation results of power flow inversion

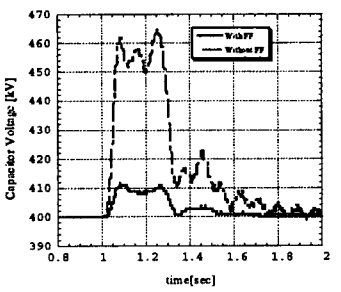


Fig.14 DC voltage waveform with FF and without FF