Grid-Connected Photovoltaic Inverter with Zero-Current-Switching

Hang-Seok Choi, Y. J. Cho, J. D. Kim and B.H. Cho

Department of Electrical Engineering

Seoul National University, Seoul, Korea

E-mail:hangseok@hitel.net

***Abstract** - This paper presents a new zero current switching (ZCS) inverter for grid-connected photovoltaic system. The proposed circuit provides zero current switching condition for all the switches, which reduces switching losses significantly. It is controlled to extract maximum power from the solar array and to provide sinusoidal current into the mains. Analysis, small signal modeling and design procedure are presented. The validity of the proposed system is verified by experimental results from the 1.2 kW prototype inverter operating at 40kHz.*

I. INTRODUCTION

With the increasing concern about global environmental protection, the need to produce pollution-free natural energy has pointed us towards alternative sources of energy. Recently, solar energy has been drawing increasing interest as an alternative source of energy for the future since solar energy is clean, pollution-free and inexhaustible.

In an effort to utilize the solar energy effectively, a great deal of research has been done on the grid-connected photovoltaic generation system for the past several years [1-5]. Generally, the grid-connected photovoltaic (PV) system extracts maximum power from the PV arrays providing current to the mains in phase with the sinusoidal voltage of the mains. When the utility power sources should provide the peak power to the load, the energy provided by PV arrays can alleviate the burden of utility power sources.

This paper proposes a transformer-less PV inverter employing zero current switching (ZCS) PWM switch cell proposed in [6,7]. By using these techniques, ZCS of the main switches and the auxiliary switches are achieved. Since the proposed inverter operates as an alternating Buck converter, the switching loss and the output current ripple can be minimized. It is controlled to extract maximum power from the solar array and to provide sinusoidal current into the mains. It uses analog controller employing the average current control to regulate the solar array output power according to the reference value generated by the peak power tracker. Analysis, small signal modeling and design procedure are presented. The validity of the proposed system is verified by the experimental results from the 1.2 kW prototype inverter operating at 40kHz.

II. PROPOSED PV INVERTER SYSTEM

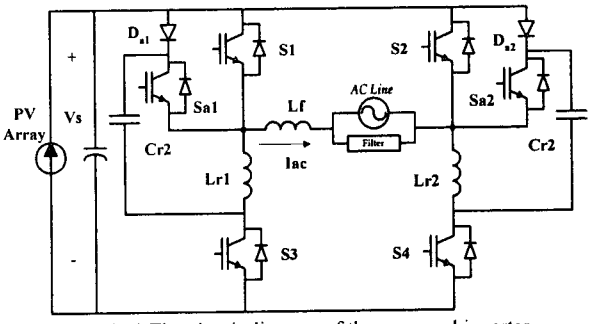

Fig.1 The circuit diagram of the proposed inverter

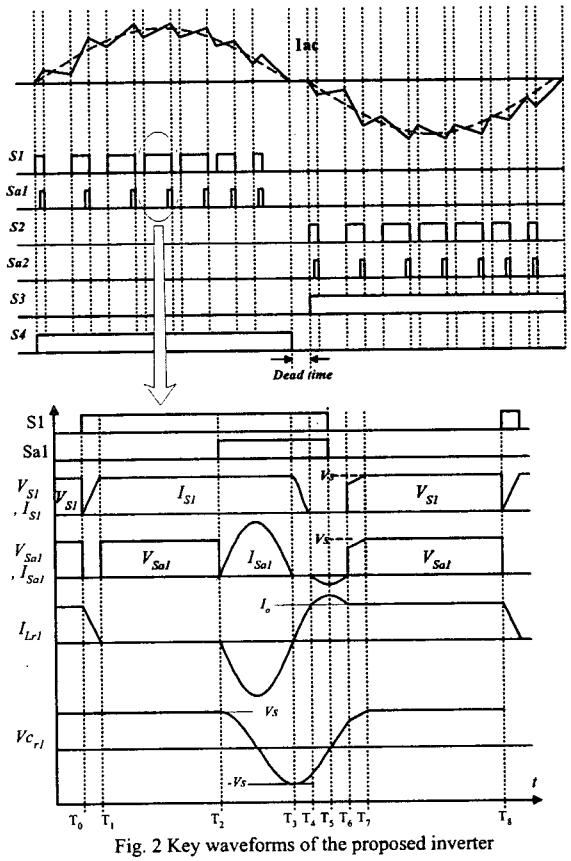

Fig. 2 Key waveforms of the proposed inverter

Fig.1 shows the basic circuit diagram of the proposed inverter. The proposed inverter operates as an alternating

Buck converter. The upper switches S1, S2 operate at 40kHz and the lower arm switches S3, S4 operate at 60Hz alternating the polarity of the Buck converter. For simplicity, it is assumed that the switch S1 operates as a switch and S3 operates as a freewheeling diode, while S4 is always turned on. To analyze the steady state operation, it is assumed that all components and devices are ideal and the output inductor is large enough to be regarded as a constant current source during one operating cycle. The proposed inverter has seven operation modes during one switching cycle. The key waveforms and the equivalent circuit of each operation mode are shown in Fig. 2 and 3, respectively. In order to guarantee the minimum duty ratio for a proper operation of the auxiliary circuit, dead time is introduced between the gating signals of S3 and S4 as can be seen in Fig. 2.

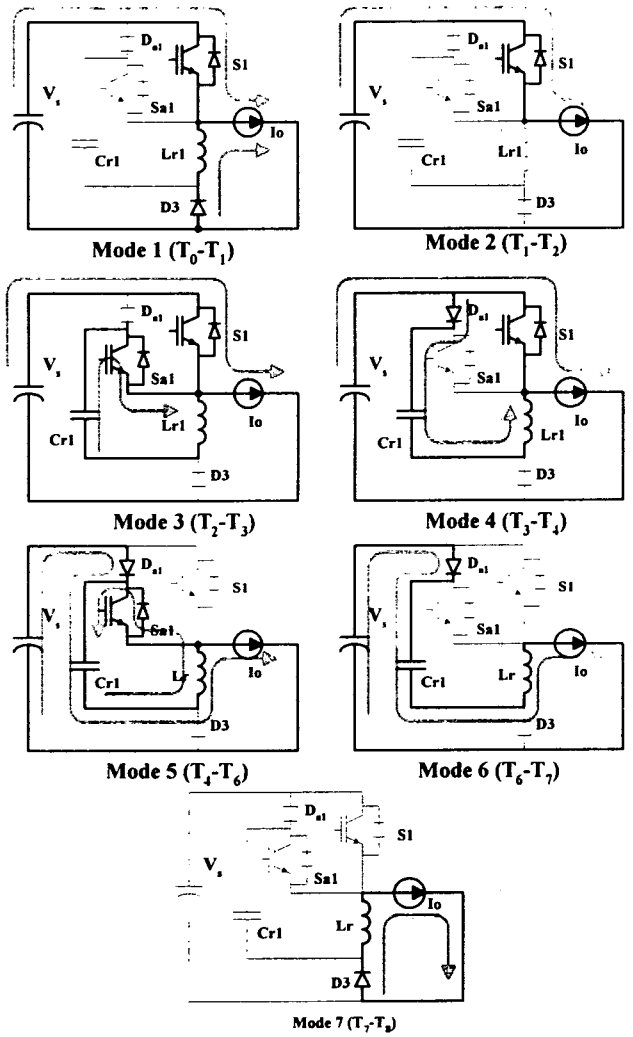

Fig. 3 Equivalent circuit of each operation mode

Mode1 (T_0-T_1): Prior to T_0, the output current Io freewheels through the diode D3. At T_0, the main switch S1 turns on and the current through S1 increases linearly until it reaches Io at T_1.

Mode2 (T_1-T_2) : When the current through S1 reaches Io, D3 turns off and Io flows through S1 and S4. During this mode the diode D3 remains in the OFF state and the voltage of the resonant capacitor C_{r1} is clamped at the input voltage Vs.

Mode3 (T_2-T_3) : At T_2, the auxiliary swith Sa1 turns on and C_r is discharged resonating with the resonant inductor L_{r1}. This mode continues until V_{cr} reaches –Vs at T_3. The voltage of C_r and the current through the auxiliary switch are obtained as

$$V_{cr1}(t) = V_s \cos(w_r(t - T_2)) \tag{1}$$

$$I_{Sa1}(t) = \frac{V_s}{Z_r}\sin(w_r(t - T_2)) \tag{2}$$

where, $w_r = \frac{1}{\sqrt{L_r C_r}}$ and $Z_r = \sqrt{\frac{L_r}{C_r}}$

Mode4 (T_3-T_4) : At T_3, the current through Lr1 changes its direction and diode Da1 begins to conduct. C_{r1} is charged through Da1 by resonance with L_{r1}. Even though there exists another charging path through the antiparallel diode of Sa1, C_{r1} is charged only through Da1, since the voltage drop of S1 counterbalances the voltage drop of Da1 providing lower impedance current path. During this mode, the current through the main switch decreases until it reaches zero. The voltage of Cr1 and the current of S1 are obtained as;

$$V_{cr1}(t) = -V_s \cos(w_r(t - T_3)) \tag{3}$$

$$I_{S1}(t) = I_o - \frac{V_s}{Z_r}\sin(w_r(t - T_3)) \tag{4}$$

Mode5 (T_4-T_6) : At T_4, the current through S1 reaches zero and the anti-parallel diode of Sa1 begins to conduct. When the current Sa1 reaches its negative peak value at T_5, the gate-drive signals for S1 and Sa1 are disabled at the same time and both switches are turned off with zero currents.

Mode6 (T_6-T_7) : Io flows through Da1 charging C_{r1}, and the voltage of Cr increases linearly until it reaches Vs at T_7.

Mode7 (T_7-T_8) : When the voltage of C_{r1} reaches Vs, Da1 turns off and D3 begins to conduct at T_7. During this mode, Io freewheels through D3 and L_{r1}. Since the voltage of C_{r1} is clamped at Vs, Da1 turns off with zero voltage.

III. DESIGN CONSIDERATIONS

In order to achieve zero current switching for S1 and S2, the following condition should be satisfied

$$I_{Lf\,peak}^{\max} = \frac{\sqrt{2}P_o}{V_{line}^{rms}} + \frac{1}{2}\Delta I_{Lf}^{peak} < \frac{V_s}{Z_r} \tag{5}$$

$$\Delta I_{Lf}^{peak} = \frac{\sqrt{2}\,V_{line}^{rms}}{L_f}\left(1 - \frac{\sqrt{2}\,V_{line}^{rms}}{V_s}\right)T_s \tag{6}$$

where T_s is the switching period and P_o is the output power.

For a proper resonant operation of the auxiliary circuit,

the duty ratio of the main switch should be always larger than resonance period Tr as;

$$T_r < D \cdot T_s \cong \frac{V_{line}}{V_s} \cdot T_s \tag{7}$$

In order to satisfy this condition, the gating signals should be disabled when the line voltage is around zero. The required dead angle is obtained as

$$\theta_{dead} = \sin^{-1}\left(\frac{V_s T_r}{\sqrt{2}\, V_{line}^{rms}\, T_s}\right) \tag{8}$$

As a rule of thumb, the proper resonance period Tr is given by [10] as

$$T_r = 2\pi\sqrt{L_{r1}C_{r1}} \cong (4-6)\cdot T_f \tag{9}$$

where T_f is the fall time of the switching device.

IV. SMALL SIGNAL ANALYSIS AND CONTROL

Fig. 4 shows the simplified conceptual circuit diagram of the PV inverter system. As can be seen, the inverter is simplified as a buck converter. The solar array voltage is regulated by V_{ref} which is generated by the peak power tracker. To regulate the solar array voltage, the voltage compensator controls the amplitude of the current reference i_{ref} which changes in a sinusoidal manner. Thus, the buck converter extracts an appropriate amount of solar array current in such a way to match the solar array voltage with V_{ref}. The PV inverter can be considered as a dual of power factor correction (PFC) Boost converter, which extract current from the main in a sinusoidal manner regulating the output voltage.

Fig. 5 shows the small-signal model of the PV inverter employing the PWM switch model. The small-signal model for the solar array consists of the solar array output impedance, rs, and a current source $\hat{i}_s$, as the input perturbing signal.

Fig. 6 represents the small-signal model block diagram of the PV inverter. The current loop Ti consists of power stage-duty cycle to inductor-current gain G_{id}, the current sensing network gain Ri, sampling gain He(s), modulator gain Fm, and the current compensator Hi(s). Hv(s) and Rs represent the voltage compensator and voltage sensing network gain, respectively.

The small signal transfer functions have been derived in [8,9] as ;

$$G_{vd} = \frac{\hat{V}_s}{\hat{d}} = -\frac{V_{line}}{D^2}\frac{(1+sR_c\cdot C)(1+s\frac{I_S L_f}{D V_{line}})}{(1+s/Qw_o+s^2/w_o^2)} \tag{10}$$

$$G_{id} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_{line}}{D^3 r_o}\frac{(1+s\,r_o C)}{(1+s/Qw_o+s^2/w_o^2)} \tag{11}$$

$$w_o = \frac{D}{\sqrt{L_f C}}\ , \quad Q = \frac{1}{w_o[(R_c+\frac{R_l}{D^2})C+\frac{L_f}{D^2 r_o}]} \tag{12}$$

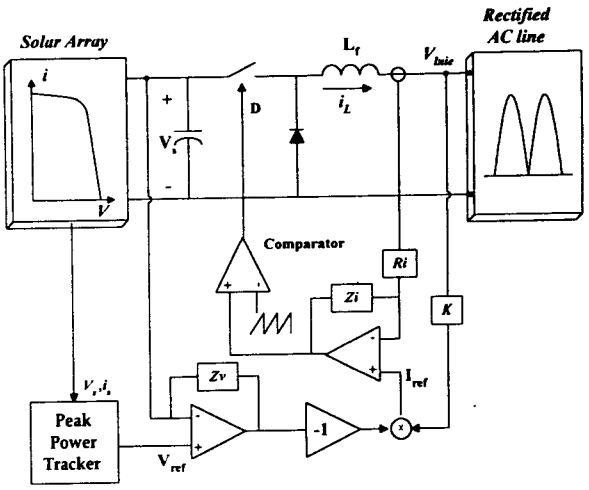

Fig. 4 Simplified circuit diagram of the PV inverter

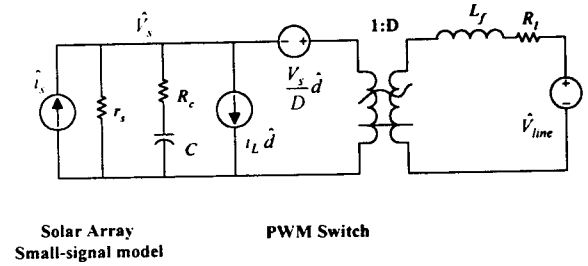

Fig. 5 Equivalent small-signal model of the PV inverter

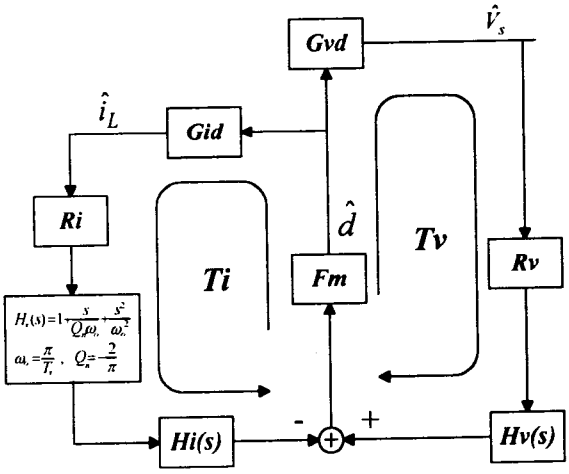

Fig. 6 Block diagram of the small signal model of the PV inverter

where ro=-rs.

Since the PV inverter is the dual of the PFC boost converter, the transfer functions are identical to the boost converter except for the direction of the dc current i_L. Thus G_{vd} has light half plane zero, instead of right half plane zero as in conventional boost converter. The dc gain of Gvd is negative, which requires a positive feedback loop as can be seen in Fig. 4.

4.1. Current loop design

To control the inductor current, average current mode control with a two-pole, one zero compensator is employed as;

$$G(s) = \frac{w_i}{w} \frac{1 + s/w_z}{1 + s/w_p} \quad (13)$$

For the design of the compensation pole, zero and integrator gain, the zero should be placed at least one decade below the switching frequency for a acceptable phase margin, and the high frequency pole w_p should be placed at or after half of the switching frequency to filter out the switching ripple of the sensed inductor current [11].

4.2 Voltage loop design

Since the inverter extracts current from the solar array in a form of sine squared function, there always exists 120 Hz ripple in the voltage of the output filter capacitor of solar array. Therefore, the bandwidth of the voltage feedback loop should be very low, well below 60 Hz to minimize the output current distortions caused by the 120 Hz ripple. The two-pole, one zero compensator of (13) is also used for the solar array voltage regulation. The high frequency pole should be placed at or below 60 Hz.

4.3 PPT loop design

Since the bandwidth of the voltage feedback loop is very low, the speed of the PPT loop should be slow enough well below the speed of voltage loop to guarantee the stability.

V. Experimental Results

The main parameters and components used for experiment are summarized in Table I. It is assumed that twenty solar array panels (SM-60, Samsung electronics) are connected in series. The mains voltage is 220V.

BLE I Utilized components and parameters

Components	Parameters
Vs	340 - 440V
V_{line}	220V (rms)
Lf	PE22EC90-Z , 1 mH
Lr1. Lr2	PQ2620, 20μH
Cr1, Cr2	10 nF ,polypropylene capacitor (600V)
C	450V/ 470 μF, electrolytic capacitor
S1,S2	IRGPC40UD2 (600V, 20A)
S3, S4	IRGPH50KD2 (1200V, 20A)
Sa1,Sa2	IRGPC30UD2 (600V, 20A)
Da1, Da2	MUR860 (600V, 8A)

Fig. 7 and 8 shows the current and voltage waveforms of the upper arm switch and the auxiliary switch, respectively. As can be seen, the upper arm switch and the auxiliary switch turn on and turn off with zero currents, which reduces the switching losses. Fig. 9 shows the gating signals of S1 and S4, and waveforms of the output inductor current and output current. Lower arm switch S4 operates at 60 Hz while, S1 operates at 40 kHz controlling the inductor current.

Fig. 10 shows the measured efficiency. The proposed circuit has higher efficiency than the hard switching inverter. The maximum efficiency is 97.5 % at full load and about 2 % of improvement of the efficiency is obtained.

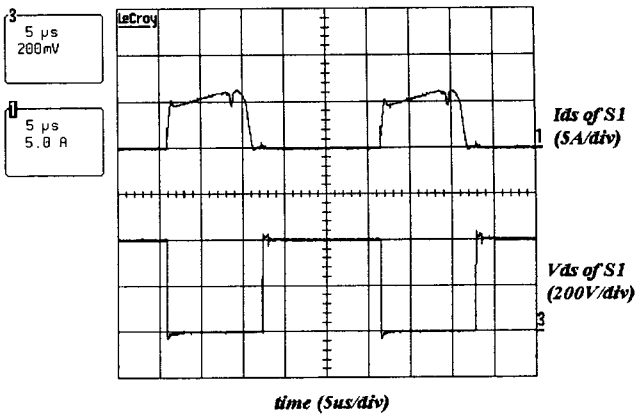

Fig. 7 Voltage and Current waveforms of the switch S1

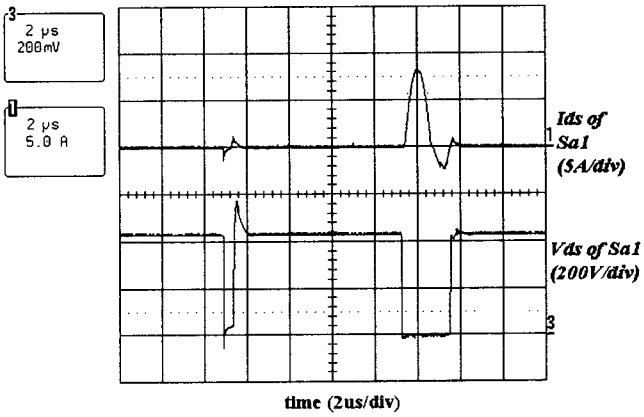

Fig. 8 Voltage and Current waveforms of the switch Sa1

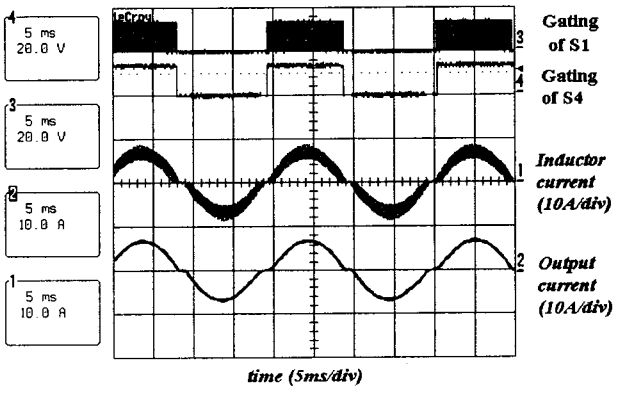

Fig. 9 Gating signals and the output current waveforms

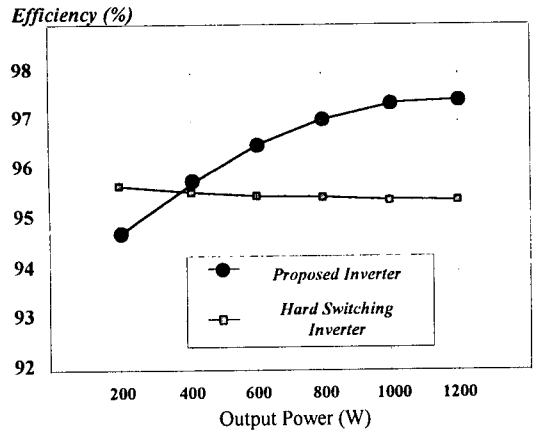

Fig. 10 Measured Efficiency

VI. CONCLUSION

This paper has presented a new zero current switching (ZCS) inverter for grid-connected photovoltaic system. The proposed circuit provides zero current switching condition for all the switches, which reduces switching losses significantly. It is controlled to extract maximum power from the solar array and to provide sinusoidal current into the mains. Analysis, small signal modeling and design procedure were presented. The validity of the proposed system was verified by experimental results from the 1.2 kW prototype inverter operating at 40kHz.

REFERENCE

[1] D. C. Martins, R. Demonti and I. Barbi, " Usage of the Solar Energy from the Photovoltaic Panels for the Generation of Electrical Energy", INTELEC 99', 17-3

[2] N. Kasa, H. Ogawa and T. Iida, "A Transformer-Less Inverter using Buck-Boost Type Chopper Circuit for Photovoltaic Power System", PEDS 99', pp.653-658.

[3] M. F. Rahman and L. Zhong, "A New, Transformerless, Photovoltaic Array to Utility Grid Interconnection", PEDS 97', pp.653-658.

[4] T. Tawara, T. Aoki and Y. Kawagoe, "An Efficienct Interactive Inverter for a Photovoltaic System", APEC 99', pp.1052-1056.

[5] J. Rajagopalan and B.H. Cho, "Space-Vector Modulated PWM Converters for Photo-voltaic Interface Applications : Analysis, Control and Power Management Issues", IEEE APEC 1995, pp.814-820.

[6] H. S. Choi and B.H. Cho "Zero Current Switching (ZCS) PWM Switch Cell Minimizing Additional Conduction Loss," KIPE Power Electronics Autumn Conference, pp.159–162, 2000.

[7] H. S. Choi and B. H. Cho "Novel Zero-Current-Switching (ZCS) PWM Switch Cell Minimizing Additional Conduction Loss", PESC 2001, pp.872-877

[8] P. Huynh and B.H. Cho, "Analysis and Design of a Microprocessor Controlled Peak Power Tracking System," Proceedings of the Intersociety Energy Conversion Engineering Conference, American Nuclear Society, Illinois, 1992, pp.1.63-1.78.

[9] S. J. Kim, J. R. Lee, B.H. Cho, "Large-Signal Analysis of Spacecraft Power System,"24th IECEC, 1989.

[10] K. Wang, G. Hua and F. C. Lee,"Analysis, design and ZCS-PWM Boost converters," IEEJ International Power Electronics Conference, pp.1202 –1207, 1995.

[11] L. Dixon, "Average current mode control of switching power supplies," Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-700, 1990.