

A Primary-Side-Assisted Zero-Voltage and Zero-Current Switching Three-Level DC-DC Converter

S. J. Jeon,
Dept. of Electronic Engineering
Pukyong National University
Pusan 608-737, KOREA

F. Canales, P. M. Barbosa and F. C. Lee
Center for Power Electronics System (CPES)
Bradley Dept. of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061-0178, USA

Abstract: A new primary-side-assisted zero-voltage and zero-current switching (ZVZCS) three-level DC-DC converter with flying capacitor is proposed. The three-level converters are promising in high voltage applications, and ZVZCS is a very effective means for reducing switching losses. The proposed DC-DC converter uses only one auxiliary transformer and two diodes to obtain ZCS for the inner leg. It has a simple and robust structure, and offers soft-switching capability even in short-circuited conditions. The proposed converter was verified by experiments in a 6KW prototype designed for communication applications and operating at 100 kHz.

Key Words: DC-DC Converter, Zero-Voltage and Zero-Current Switching, ZVZCS, Three-Level Converter, Primary-Side-Assisted ZVZCS

I. Introduction

Nowadays, power demand is continually increasing. The three-phase AC-DC converter operating with 380V or 440V lines is suitable as an input stage for a high power DC-DC converter [1,2]. In the three-phase AC-DC converter, a boost power factor corrector (PFC) is widely used to comply with such regulations as the IEC61000-3-2. In this converter, the DC-link voltage must be increased compared to the line voltage to meet the aforementioned standard. The three-level (TL) DC-DC converter is promising in cases of high DC-link voltage because it uses low-voltage switching devices [3-9]. The switching loss can be greatly reduced by using a zero-voltage switching (ZVS) method [3-6,8]. However, in wide range of ZVS, the conduction losses of ZVS converters are high during the freewheeling period. To solve these problems, zero-voltage and zero-current switching (ZVZCS) is proposed [9]. The secondary-side-assisted (SA) ZVZCS techniques used for full bridge converters are directly applicable to TL DC-DC converter [10-16]. However, the SA ZVZCS operations are heavily dependent on load voltage, so they lose soft switching capabilities at start-up or for a short-circuited load.

This paper proposes a new primary-side-assisted (PA) TL ZVZCS DC-DC converter, the auxiliary circuit of which consists of only one auxiliary transformer and two diodes. The proposed converter has a robust structure and does not lose soft-switching capability even in short-circuited conditions or at start-up.

II. Proposed Circuit

A. Operation Principle

The proposed PA ZVZCS TL DC-DC converter is shown in Fig. 1. It has three legs: an inner leg (S_1 and S_3), an outer leg

(S_2 and S_4) and a passive leg (D_{A1} and D_{A3}). The output power is controlled by the phase delay between the inner and outer legs. To obtain an appropriate phase delay, phase shift PWM (Pulse Width Modulation) is employed. The auxiliary circuit consists of only two diodes and a small three-winding auxiliary transformer. The primary winding of the auxiliary transformer is connected in series with the primary winding of the main transformer; two secondary windings of the auxiliary transformer are connected between the auxiliary diodes and the outer leg switches. The outer two switches operate in the ZVS condition with the assistance of reactive components C_2 , C_4 , C_{β} , L_{lk} and L_f . The L_{lk} is the sum of the leakage inductances of the main transformer and the auxiliary transformer. The C_2 and the C_4 provide Zero-Voltage turn-off for switches S_2 and S_4 . The L_{lk} and the L_f provide Zero-Voltage turn-on by changing the voltage across C_4 (or C_2) to $V_{DC}/2$ and the voltage across C_2 (or C_4) to zero, as well as causing the primary current to flow through freewheeling diode D_{22} (or D_{44}) prior to turn on of S_2 (or S_4). The flying capacitor (C_{β}) couples C_2 and C_4 during transition. The inner switches operate in the ZCS condition with the assistance of the auxiliary circuit, which provides resetting voltage and absorbs reactive energy trapped in the leakage inductor L_{lk} . The passive leg operates according to the primary current; diode D_{A3} is turned on when i_1 is positive, and diode D_{A1} is turned on when i_1 is negative.

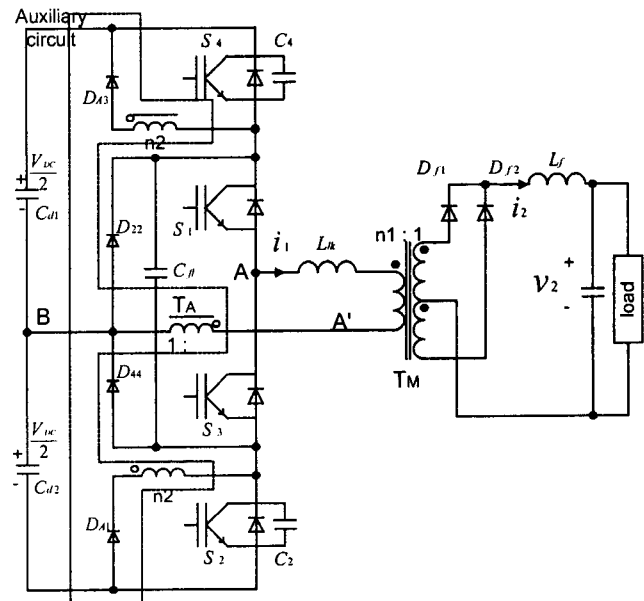


Fig. 1. Circuit diagram of the proposed PA ZVZCS TL DC-DC converter.

S. J. Jeon is with CPES as a visiting professor. This work was sponsored by Pukyong National University, KOREA, and in part by ERC Program of National Science Foundation under Award Number EER-9731677.

B. Operating Modes

Fig. 2 shows the operating waveforms; one cycle operation can be divided into five modes, as shown in Fig. 3. To simplify analysis, the magnetizing inductances of the main and auxiliary transformers are ignored, and the initial voltage across the flying capacitor is assumed to be $V_{DC}/2$.

1) **Mode1** ($t_1 < t < t_2$): During this mode, switches S_1 and S_4 are in conduction states and power is transferred to the load through both the main transformer and the rectifier diode D_{f1} . The secondary terminals of the auxiliary transformer are short-circuited by D_{A3} and S_4 . Accordingly, the terminal voltage of the auxiliary transformer is zero. The current flowing through S_4 is given by

$$i_{S4} = \left(1 + \frac{1}{n_2}\right) i_1 \quad (1)$$

2) **Mode2** ($t_2 < t < t_3$): This mode is initiated by turning off S_4 . A resonant circuit is constructed with C_2 , C_4 , C_{β} , L_{lk} and L_f . The C_{β} couples C_2 and C_4 and helps Zero-Voltage turn-on of S_2 . The equivalent circuit is shown in Fig. 3(f). The voltage across capacitor C_4 is given by

$$v_{c4} = \frac{n_2}{1+n_2} \left(\left(\frac{V_{DC}}{2} - n_1 V_2 \right) (1 - \cos \omega_o (t - t_2)) + I_1(t_2) Z_o \sin \omega_o (t - t_2) \right) \quad (2)$$

and the primary current i_1 is given by

$$i_1 = \frac{\frac{V_{DC}}{2} - n_1 V_2}{Z_o} \sin \omega_o (t - t_2) + I_1(t_2) \cos \omega_o (t - t_2), \quad (3)$$

where

$$\omega_o = \sqrt{\frac{1}{L_{eq} C_{eq}}}, \quad (4)$$

$$Z_o = \sqrt{\frac{L_{eq}}{C_{eq}}}, \quad (5)$$

$$L_{eq} = L_{lk} + n_1^2 L_f, \quad (6)$$

$$C_{eq} = \left(C + \frac{C C_{\beta}}{C + C_{\beta}} \right) \left(\frac{n_2}{1 + n_2} \right)^2, \text{ and} \quad (7)$$

$$C = C_2 = C_4. \quad (8)$$

The voltage across the capacitor C_2 is given by

$$v_{c2} = \frac{V_{DC}}{2} - \frac{C_{\beta}}{C + C_{\beta}} v_{c4}. \quad (9)$$

The primary current i_1 is nearly constant during this interval, since $n_1^2 L_f$ is large and this interval is short. The voltage across S_4 increases smoothly to $V_{DC}/2$, which results in Zero-Voltage turn-off of S_4 .

3) **Mode3** ($t_3 < t < t_4$): This mode is initiated after the voltage across S_4 reaches $V_{DC}/2$, and the primary current flows through D_{22} . Half of the input voltage is introduced to the secondary winding of the auxiliary transformer and reflected to the primary one, as shown in Fig. 3(c). The reactive energy trapped in the inductor L_{lk} is recovered to the DC-side. The primary current i_1 decreases to zero as

$$i_1 = I_1(t_3) - \frac{V_{aux}}{L_{lk}} (t - t_3), \quad (10)$$

where V_{aux} is the reflected voltage of the input DC-side through the auxiliary transformer, acting to reset the primary current, and given by

$$V_{aux} = \frac{V_{DC}}{2n_2}. \quad (11)$$

Assuming $C \ll C_{\beta}$, (9) determines that

$$v_{c2} = 0. \quad (12)$$

Hence, S_2 can be turned on with ZVS condition, which leads to the conclusion that C_{β} should be sufficiently large to ensure ZVS.

4) **Mode4** ($t_4 < t < t_5$): This mode is initiated after the primary current becomes zero. During this mode the primary current remains at zero, and the load current flows evenly through D_{f1} and D_{f2} , as shown in Fig. 3(d). Also in this mode, switch S_1 is turned off with ZCS condition.

5) **Mode5** ($t_5 < t < t_6$): This mode is initiated by turning on switch S_3 with ZCS condition. The primary current i_1 begins to flow through switches S_2 and S_3 . The secondary terminals of the auxiliary transformer are short-circuited by D_{A1} and S_2 . The primary current i_1 is given by

$$i_1 = -\frac{V_{DC}}{2L_{lk}} (t - t_5). \quad (13)$$

The load current flowing through D_{f1} diverts to D_{f2} as i_1 increases. This mode ends when the current flowing through D_{f1} becomes zero.

In this way, one switching cycle is completed. The next switching cycle begins with Mode 1, during which switches S_2 and S_3 are in conduction states.

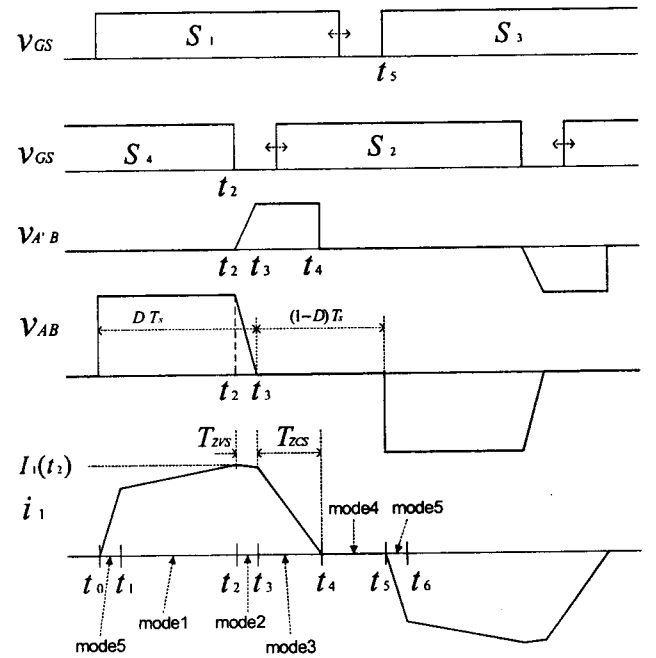


Fig. 2. The operational waveforms of the proposed circuit.

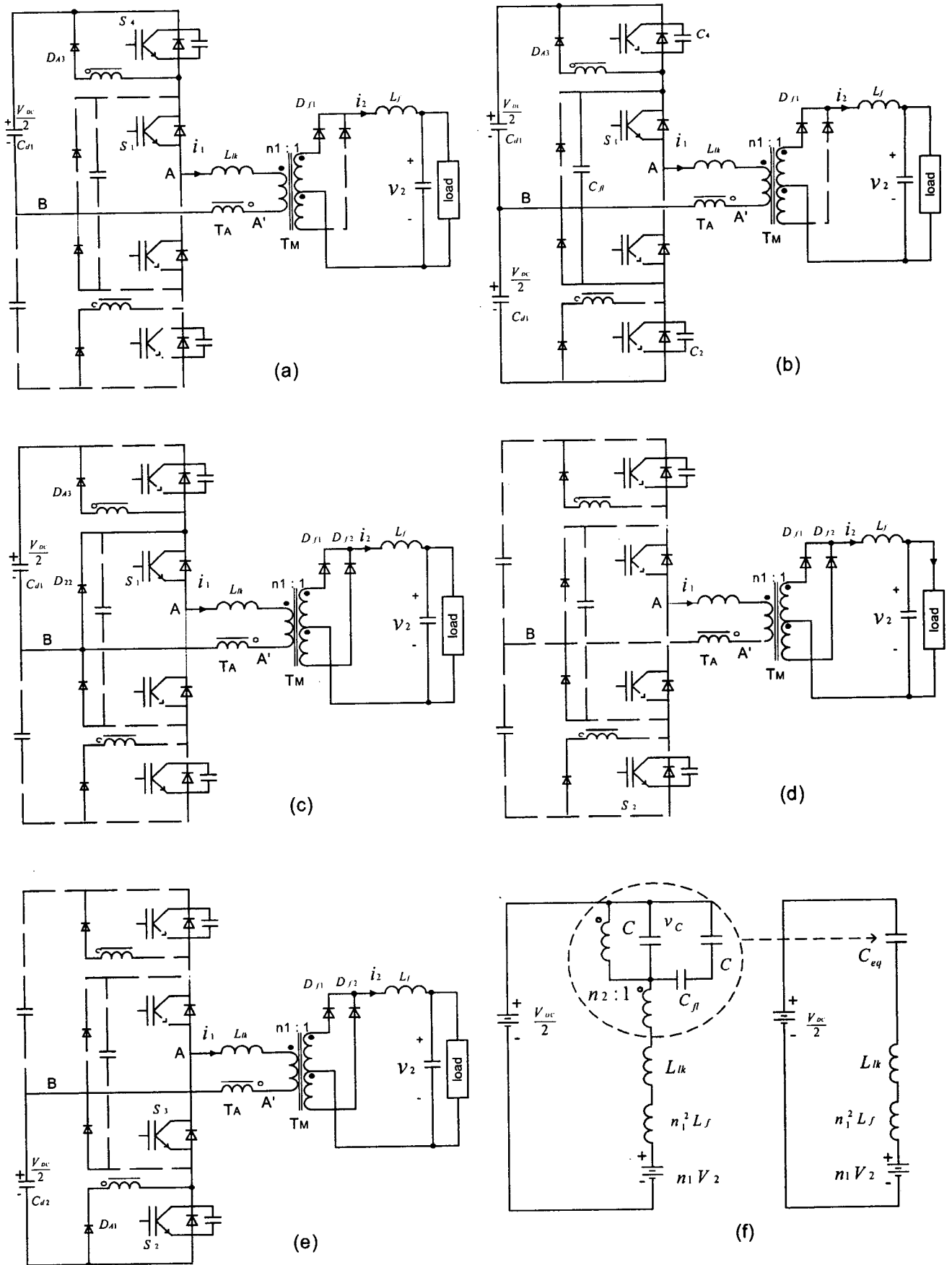


Fig. 3. Operating modes of the proposed circuit:
 (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; and (f) equivalent circuit for Mode 3.

C. Conditions for ZVZCS Operation

The Zero-Voltage turn-off of switch S_4 is natural, as C_{eq} is connected in parallel with S_4 . In full bridge DC-DC converter, if v_{C4} reaches the level of the DC-link voltage, the safe Zero-Voltage turn-on of S_2 can be attained. In this three-level DC-DC converter, however, one more condition is needed because although v_{C4} reaches $V_{DC}/2$ at the end of mode 2, v_{c2} is not exactly zero. Its final voltage depends on the ratio of C_{f1} to C . To achieve safe ZVS-on of S_2 , the final voltage of v_{c2} must be less than the on-voltage of the switch. The extra condition is given by

$$C_{f1} > C \left(\frac{V_{DC}}{2V_s} - 1 \right), \quad (14)$$

where V_s is the on-voltage of the switch.

The primary current i_1 is nearly constant during mode 2, since $n_1^2 L_f$ is large and the time interval is short. The time interval given to switches S_2 and S_4 for ZVS operation is given by (15), and is easily designed by selecting the appropriate C_{eq} .

$$T_{ZVS} = t_3 - t_2 = \frac{C_{eq} V_{DC}}{2I_1}. \quad (15)$$

During mode 3, Zero-Current turn-off operation in the inner switches is accomplished by eliminating the primary current prior to removing the gate pulse of S_1 . The approximate time interval required to eliminate the primary current is given by

$$T_{ZCS} = t_4 - t_3 = \frac{L_{lk} I_1}{V_{aux}}. \quad (16)$$

This ZCS operation does not depend on the output voltage, and can be obtained regardless of the output voltage if DC-link voltage is established. The T_{ZCS} is at its maximum when the current is at its maximum, and the maximum T_{ZCS} is given by

$$T_{ZCS \max} = \frac{L_{lk} I_{1 \max}}{V_{aux}}, \quad (17)$$

where $I_{1 \max}$ is the maximum current allowed.

The condition for safe ZCS operation is given by

$$T_{ZCS \max} < (1 - D_{\max}) T_s, \quad (18)$$

where D_{\max} is the maximum duty cycle and T_s is the switching period.

III. Experimental Results

A 6KW prototype of the proposed circuit was constructed and tested. It was designed for use in communication applications. The normal operating voltage is 800V, and the final voltage at holdup time is 660V. The operating frequency is 100 kHz. Circuit parameters and components used are shown in Table 1; results are shown in Figs. 4 - 7. Fig. 4 shows the measured efficiency curve. Maximum efficiency is about 95.5%. In Fig. 5 the top trace is the bridge output voltage v_{AB} ; the middle trace is the voltage v_{BC} of the secondary winding of the auxiliary transformer; and the bottom trace is the primary current of the main transformer. It can be seen that the two DC-link voltages are balanced, the inner switches operate in ZCS mode, and the resetting voltage is introduced during mode 3 and disappears when the primary current is reduced to zero. Fig. 6 shows the drain-to-source voltage of a outer switch and its gate signal. It can be seen that the voltage falls to zero prior to the turn-on of the gate signal, which means ZVS operation.

Table 1. Components and parameters used

S_1, S_4	APT60M90JN	C_{eq}	2.5nF
D_{A1}, D_{A3}	RHRP860CC	C_{f1}	4uF
D_{22}, D_{44}	BYV34-500	C_{d1}, C_{d2}	4uF
D_{f1}, D_{f2}	HFA140MD60C	L_{lk}	1.3uH
n_1	5	L_f	16uH
n_2	6		

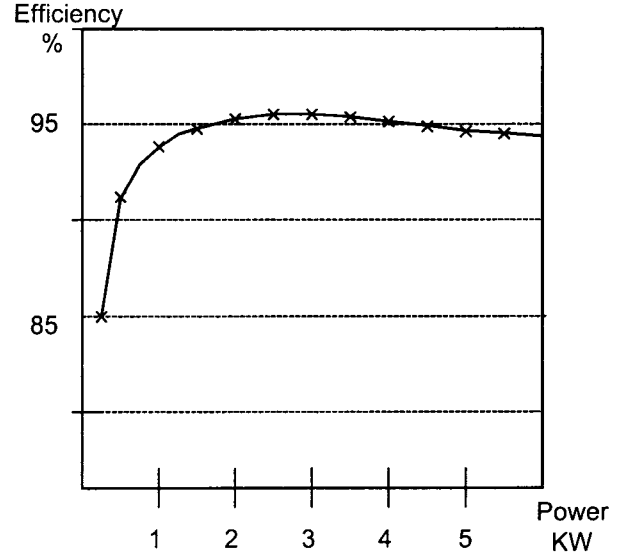


Fig. 4. Efficiency curve of the proposed PA ZVZCS TL DC-DC converter.

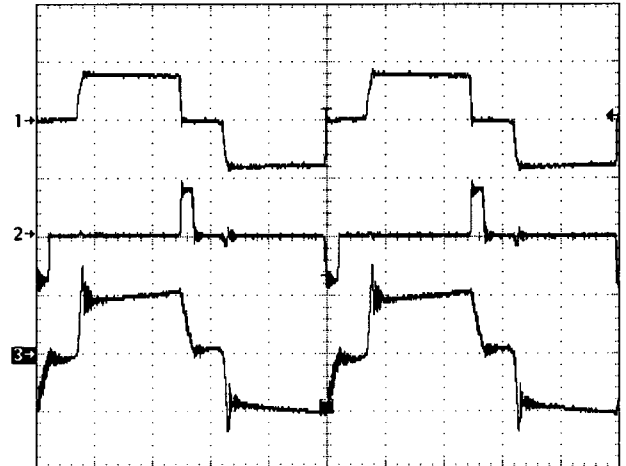


Fig. 5. Experimental waveforms of the primary side: bridge output voltage (top trace: 500V/div), primary voltage of the main transformer (middle trace: 500V/div), and primary current (bottom trace: 20A/div), all with a time base of 2usec/div.

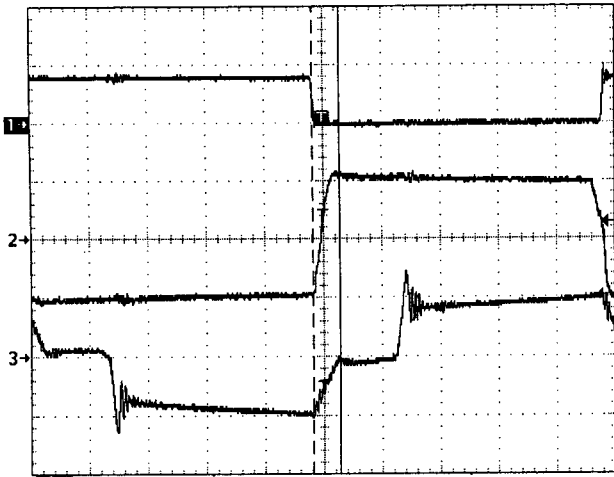


Fig. 6. Experimental waveforms of the outer leg switch: drain-to-source voltage (top trace: 500V/div), gate signal (middle trace: 10V/div), and the primary current (bottom trace: 20A/div), both with a time base of 1 μ sec/div.

IV. Conclusion

A new PA ZVZCS TL DC-DC converter with flying capacitor is proposed. The three-level converters are promising in high voltage applications and ZVZCS is a very effective means in reducing switching losses. The proposed DC-DC converter uses only one auxiliary transformer and two diodes to obtain ZCS for the inner leg. It does not lose soft-switching capability at start-up or at short-circuited load. The operation of the converter was verified by experiments in a 6 kW prototype operating at 100 kHz. Due to its simplicity and robustness, the proposed topology is thought to be suitable for high-voltage and high-power applications.

References

- [1] Y.S. Sun, S.H. Woo, C.H. Kang, J.S. Yoo, J.J. Lee and H.J. Kim, "A Development of the Large Capacity Telecommunications Rectifier System Using Series-Resonant Technology and Half-Bridge Topology," in *Proc. IEEE Telecommunications Energy Conference*, pp.13-2, 1999.
- [2] J. Elek, D. Knurek, "Design of a 200 Amp Telecom Rectifier Family Using 50 Amp DC-DC converters," in *Proc. IEEE Telecommunications Energy Conference*, pp.5-2, 1999
- [3] J.R. Pinheiro and I. Barbi, "The three Level ZVS PWM Converter: A New Concept in High-Frequency DC-DC Conversion," in *Proc. IEEE IECON*, pp.173-178, 1992
- [4] J.R. Pinheiro and I. Barbi, "Wide Load Range Three Level ZVS-PWM DC-to-DC Conversion," in *Proc. IEEE IECON*, pp.171-177, 1993
- [5] J.R. Pinheiro and I. Barbi, "Three Level ZVS-PWM DC-DC Converters- A Comparison," in *Proc IEEE IECON*, pp.914-919, 1995
- [6] J.R. Pinheiro and I. Barbi, "An Improved TL-ZVS-PWM DC-DC Converter," in *Proc IEEE IECON*, pp.907-912, 1995
- [7] R. Gules, R. Redl and N.O.Sokal, "DC/DC Converter for High Input Voltage," in *Proc. IEEE Power Electronics Specialist Conference*, pp.1-7, 1998
- [8] F. Canales, P.M. Barbosa, J.M. Burdío and F.C. Lee, "A Zero Voltage Switching Three Level DC/DC Converter," in *Proc. IEEE Telecommunications Energy Conference*, pp. 512-517, 2000
- [9] F. Canales, P.M. Barbosa and F.C. Lee, "A Zero Voltage and Zero Current Switching Three Level DC/DC Converter," in *Proc. IEEE Applied Power Electronics Conference*, pp. 314-320, 2000
- [10] J.G. Cho, G.H. Rim, and F.C. Lee, "Zero-Voltage and Zero-Current Switching Full Bridge PWM Converter Using Secondary Active Clamp," in *Proc. IEEE Power Electronics Specialist Conference*, pp.657-663, 1996
- [11] E.S. Kim, K.Y. Joe, M.H. Kye, Y.H. Kim and B.D. Yoon, "An Improved Soft Switching PWM FB DC/DC Converter for Reducing Conduction Losses," in *Proc. IEEE Power Electronics Specialist Conference*, pp.651-656, 1996
- [12] J.G. Cho, J.W. Baek, D.W. Yoo, C.Y. Jeong, H.S. Lee, and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching(ZVZCS) Full Bridge PWM Converter Using Transformer Auxiliary Winding," in *Proc. IEEE Power Electronics Specialist Conference*, pp.227-232, 1997
- [13] J.W. Baek, C.Y. Jeong, J.G. Cho, D.W. Yoo, H.S. Lee, and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching(ZVZCS) Full Bridge PWM Converter with Low Output Current Ripple," in *Proc. Telecommunications Energy Conference (INTELLEC '97)*, pp.257-262, 1997
- [14] J.G. Cho, J.W. Baek, C.Y. Jeong, D.W. Yoo, H.S. Lee, and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching(ZVZCS) Full Bridge PWM Converter Using A Simple Auxiliary Circuit," in *Proc. IEEE Applied Power Electronics Conference*, pp.834-839, 1998
- [15] E.S. Kim, K.Y. Joe, and S.G. Park, "An Improved soft switching PWM FB DC/DC Converter Using the Modified Energy Recovery Snubber," in *Proc. IEEE Applied Power Electronics Conference*, pp.119-124, 2000
- [16] J.G. Cho, J.A. Sabate, G. Hua and F.C. Lee, "Zero-Voltage and Zero-Current Switching Full Bridge PWM Converter for High Power Applications," in *Proc. IEEE Power Electronics Specialist Conference*, pp.102-108, 1994
- [17] S.J. Jeon and G.H. Cho, "Zero-Voltage and Zero-Current Switching Full Bridge DC-DC Converter for Arc Welding Machines," *IEE Electronics Letters*, Vol. 35, No. 13, pp.1043-1044, 1999
- [18] S.J. Jeon and G.H. Cho, "Zero-Voltage and Zero-Current Switching Full Bridge DC-DC Converter with Transformer Isolation," *IEEE Trans. on Power Electronics*, Vol. 16, No.5, pp., 2001
- [19] W. McMurray and D.P. Shattuck, "A Silicon-Controlled-Rectifier Inverter with Improved Commutation," *IEEE Trans. on Communications and Electronics*, Vol. 80, pp.531-542, 1961
- [20] I. Barbi, D.C. Martins, "A True PWM Zero-Voltage Switching Pole with Very Low Additional RMS Current Stress," in *Proc. IEEE IAS Annual Meeting*, pp.1228-1235, 1991
- [21] D.C. Martins, F.J.M. Seixas, J.A. Brilhante and I. Barbi, "A Family of DC-DC PWM Converter Using a New ZVS Commutation Cell," in *Proc. IEEE Power Electronics Specialist Conference*, pp.524-530, 1993
- [22] J.A. Lambert, J.B. Vieira, L.C. Freitas, L.R. Barbosa and V.J. Farias, "A Boost PWM Soft-Single-Switched Converter with Low Voltage and Current Stresses," *IEEE Trans. on Power Electronics*, Vol. 13, No.1, pp.26-35, 1998
- [23] L.R. Barbosa, J.B. Vieira Jr., L.C. Freitas and V.J. Farias, "An Improved Boost PWM Soft-Single-Switched Converter with Low Voltage and Current Stresses," in *Proc. IEEE Applied Power Electronics Conference*, pp.723-728, 2000