Internal Model Control of UPS Inverter using Resonance Model

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Abstract - In this paper, a new fully digital control method for single-phase UPS inverter, which is based on the double control loop such as the outer voltage control loop and inner current control loop, is proposed. The inner current control loop is designed and implemented in the form of internal model control and takes the presence of computational time-delay into account. Therefore, this method provides an overshoot-free reference-to-output response. In the proposed scheme, the outer voltage control loop employing P controller with resonance model implemented by a DSP is introduced. The proposed resonance model has an infinite gain at resonant frequency, and it exhibits a function similar to an integrator for AC component. Thus the outer voltage control loop causes no steady state error as regard to both magnitude and phase. The effectiveness of the proposed control system has been demonstrated by the simulation and experimental results respectively.

Key Words : UPS Inverter, Internal Model Control, Resonance Model, Load Current Prediction

1. INTRODUCTION

In recent years, UPS(Uninterruptible Power Supply) have been widely used to provide the pure sinusoidal ac voltage to the critical loads such as computers, factory automation systems, electronic equipments and communication systems against the poor utility power system. The output voltage of UPS inverter with LC filter must be a low-distortion waveform irrespective of load condition and transient. To achieve this, a high speed and accurate control capability of both the output voltage and the output current of inverter are required, therefore a double control strategy with an inner current control loop inside a outer voltage control loop is mostly employed[1]. One of the inner current control methods is the hysteresis current control, in which a hysteresis is used to determine the permitted deviation of the actual phase current from the reference value[2]. This method has a very fast response and is easy to implement. However, it has the drawback of high and non-constant switching frequency. Another is the PI synchronous reference frame control[3]. In this method, the output of PI controller is taken as the modulation signal, and a sine-triangular PWM(Pulse Width Modulation) scheme is applied. This method, though simple and giving fixed switching frequency, has difficulty in adjusting the controller parameters. Nowadays, a discrete control technique has been applied to PWM inverter because it essentially has no aging, high flexibility, reliability, smaller size and is easier to implement than analog control scheme. Predictive control is one of the typical digital control technique using a model of the inverter system and past samples of the current[4]. The principle of this method is that the error between the reference and actual current can be predicted at the next sampling instant. The repetitive control is another reliable digital control method[5]. In this scheme, the cyclic disturbance is calculated by the errors that are occurred in the previous cycle of the output voltage. This is the proper scheme for the control only under nonlinear loads, but can be unstable under non-cyclic disturbances. Deadbeat control is as known guarantees the best possible dynamic performances among the fully digital solutions[6]. The switching pulse width is adopted so that output current is been exactly equal to its reference without error and overshoot at the next sampling instant. An important advantage of deadbeat control is that it does not required line voltage measurement in order to generate the current reference. On the other hand, the inherent delay due to the calculation time is indeed a serious drawback in practical applications. As a good digital control scheme, a space vector control technique is frequently used for the three-phase inverter[7]. The plant model is transformed into dq rotationary reference frame, and the reference signal becomes constant, consequently the steady state error converges zero. However, the plant model transformed into dq rotationary reference frame has coupled components, and this method is used for only the three-phase inverter. The outer voltage control loop is designed for the output voltage to get no steady state error as regard to both magnitude and phase. A conventional PI controller can be used to achieve this purpose in the three-phase inverter because the reference signal is a dc quantity by a suitable dq coordinate transformation. However, if the reference signal is sinusoidal, the PI controller has the steady state error as regard to both magnitude and phase. Thus the PI controller is not suitable for a single-phase inverter.

In this paper, a new fully digital control method for single-phase UPS inverter, which is based on the double control loop such as the outer voltage control loop and inner current control loop, is proposed. The inner current control loop consists of two parts; an Internal Model controller and a modeling error feedback loop which incorporates an explicit representation of the UPS inverter system nominal[8]. This method provides a convenient way for parameterizing the controller in term of the nominal system model, including computational time-delays. In the proposed control system, overshoots and oscillations due to the computation time-delay is compensated by explicit incorporation of the time-delay in the current control loop transfer function. Therefore, this method has an essentially overshoot free reference-to-output response with a minimum possible rise time. In the proposed scheme, the outer voltage control loop employing P controller with resonance model implemented by a DSP is introduced. The resonance model has an infinite gain at resonant frequency, and the gain of resonance model is small except at the resonant frequency[9]. It exhibits a function similar to an integrator for AC component. In this case, the resonant frequency is set to the fundamental frequency of the reference voltage, and resonance model eliminates the

steady state error. Thus the outer voltage control loop causes no steady state error as regard to both magnitude and phase. The proposed control scheme are implemented without a dq coordinate transformation, therefore it can be suitable for single-phase UPS inverter to which such coordinate transformation is not applicable. The effectiveness of the proposed control system has been demonstrated by the simulation and experimental results respectively.

2. INTERNAL MODEL CURRENT CONTROL

The circuit configuration of single-phase UPS inverter with LC filter is shown in Fig. 1. The voltage equation of actual plant model in Fig. 1 is given by

$$L_f \frac{di_i}{dt} + R_f i_i = v_i - v_C \tag{1}$$

where, i_i and v_i are output current and voltage of inverter, and v_C is filter capacitor voltage, respectively. Parameters L_f and R_f represent respectively the filter inductor and the ESR of the filter inductor.

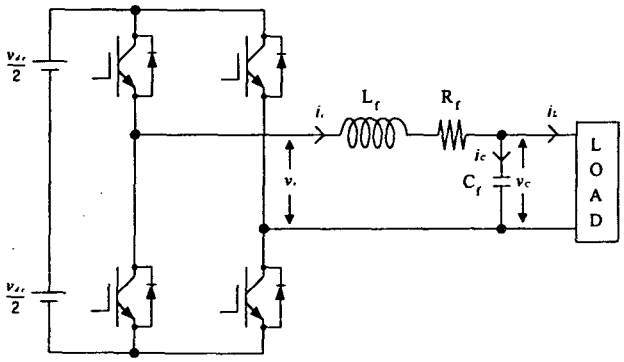

Fig. 1 Circuit configuration of single-phase UPS inverter

The voltage equation of nominal plant model is defined by

$$\tilde{L}_f \frac{di_i}{dt} + \tilde{R}_f i_i = v_i - v_C \tag{2}$$

where, parameters L_f and specially R_f are known with a limited accuracy, and are dependent on the frequency and operating conditions in practice. Therefore, a distinction is made between the actual parameter values and the nominal ones, by using "~" to denote the nominal values.

In the s-domain, Eq. (1) can be written as,

$$I_i(s) = G_{pc}(s)[V_i(s) - V_C(s)] \tag{3}$$

where, $G_{pc}(s) = \dfrac{1}{L_f s + R_f}$ (4)

The transfer function of nominal system is the same as the transfer function of actual system $G_{pc}(s)$, except that the actual parameter values are replaced by the nominal ones.

$$\tilde{G}_{pc}(s) = \frac{1}{\tilde{L}_f s + \tilde{R}_f} \tag{5}$$

As long as the control signal changes only at sampling times and stays constant between consecutive sampling points in digitally controlled systems, the zero-order-hold equivalent form of the transfer function $G_{pc}(s)$ is given by

$$G_{pc}(z) = \frac{b}{z-a} \tag{6}$$

where, $a = e^{-R_f T_{sc}/L_f}$, $b = \dfrac{1}{R_f}(1-a)$, and T_{sc} is the sampling period of the current control loop.

Similarly, the z-domain transfer function of nominal system is represented by

$$\tilde{G}_{pc}(z) = \frac{\tilde{b}}{z-\tilde{a}} \tag{7}$$

where, $\tilde{a} = e^{-\tilde{R}_f T_{sc}/\tilde{L}_f}$, $\tilde{b} = \dfrac{1}{\tilde{R}_f}(1-\tilde{a})$

The characteristics of digitally controlled system depend on the sampling time and the time delay caused by the computational time of the digital controller. A basic condition to improve the performance is to make the time delay and a sampling period shorter as far as possible. Hence, the essential requirements for digital control methods are compensation of the time delay and a simple control algorithm. To realize the above-mentioned requirements, the calculation time delay is modeled to a unit lag transfer function z^{-1} as if it is a part of the system model.

The block diagram of the proposed current control system is shown in Fig. 2. It consists of two parts; an Internal Model controller and a modeling error feedback loop which incorporates an explicit representation of the UPS inverter system nominal model. The output of the nominal plant model $\tilde{I}_C(z)$ is determined and is subtracted from the actual output $I_C(z)$, to yield a feedback signal $\hat{I}_C(z)$. The difference between the feedback signal and the current reference $I_C^*(z)$ is supplied to the internal model controller, which determines the control signal $V_L(z)$. If the actual and nominal model is exact, then the actual output $I_C(z)$ and the nominal output $\tilde{I}_C(z)$ are the same and the feedback signal $\hat{I}_C(z)$ is zero. Therefore, the current control system operates open-loop system, when there is no parameter uncertainty.

The reference-to-output transfer function including the calculation time delay is given from Fig. 2

$$\left[\frac{I_C(z)}{I_C^*(z)}\right]_{I_L(z)=0} = \frac{G_{cc}(z) z^{-1} G_{pc}(z)}{1 + G_{cc}(z) z^{-1}[G_{pc}(z) - \tilde{G}_{pc}(z)]} \tag{8}$$

Based on assumption that the actual and nominal model is exact, that is $G_{pc}(z) = \tilde{G}_{pc}(z)$, the actual output and the nominal output are the same and $\hat{I}_C(z) = 0$. In order to achieve zero steady state error, Eq. (8) must be

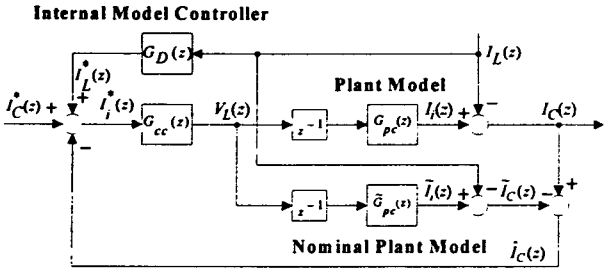

Fig. 2 Block diagram of current control loop

$$\left[\frac{I_C(z)}{I_C^*(z)}\right]_{I_L(z)=0} = G_{cc}(z)z^{-1}\tilde{G}_{pc}(z) = 1 \tag{9}$$

The transfer function $G_{cc}(z)$ is derived as following from the ideal condition in Eq. (9)

$$G_{cc}(z) = \frac{1}{z^{-1}\tilde{G}_{pc}(z)} = \frac{z(z-\tilde{a})}{\tilde{b}} \tag{10}$$

However, the above transfer function $G_{cc}(z)$ is not proper because its numerator has a greater order than the respective denominator. That is to say, this internal model controller is impossible to realize considering calculation time delay. Therefore, the transfer function $G_{cc}(z)$ is adopted to a second order deadbeat reference-to-output response which means that its response reaches the reference in two sampling time as following

$$G_{cc}(z) = \frac{1}{z^2}\frac{1}{z^{-1}\tilde{G}_{pc}(z)} = \frac{(z-\tilde{a})}{\tilde{b}z} \tag{11}$$

Under this condition, the reference-to-output transfer function including the calculation time delay in Eq. (9) is obtained as

$$\left[\frac{I_C(z)}{I_C^*(z)}\right]_{I_L(z)=0} = \frac{1}{z^2} \tag{12}$$

That is, the average current of filter capacitor is the exact replica of the reference current with a time lag of two sampling intervals. The frequency response of the reference-to-output transfer function is

$$\left[\frac{I_C(e^{j\omega T_{sc}})}{I_C^*(e^{j\omega T_{sc}})}\right]_{I_L(e^{j\omega T_{sc}})=0} = e^{-2j\omega T_{sc}} \tag{13}$$

which has unity gain and a phase lag of $2\omega T_{sc}$. The phase lag in correspondence of the two-sampling-period delay produces appreciable phase error between the reference and actual currents. To overcome this problem, an equal and opposite phase shift is added to the outer voltage control loop.

Similarly, the disturbance-to-output transfer function including the calculation time delay is given from Fig. 2

$$\left[\frac{I_C(z)}{I_L(z)}\right]_{I_C^*(z)=0} = \frac{G_D(z)z^{-1}G_{pc}(z) - G_{pc}(z)}{1 + G_{cc}(z)z^{-1}[G_{pc}(z) - \tilde{G}_{pc}(z)]} \tag{14}$$

The transfer function $G_D(z)$ is chosen such that the load current, which intervenes as a disturbance in the control loop, is eliminated by feed-forward under the same condition of Eq. (9).

$$\left[\frac{I_C(z)}{I_L(z)}\right]_{I_C^*(z)=0} = \tilde{G}_{pc}(z)[G_D(z)z^{-1} - 1] = 0 \tag{15}$$

The following transfer function $G_D(z)$ is sufficient from the ideal condition in Eq. (15)

$$G_D(z) = z \tag{16}$$

However, this transfer function $G_D(z)$ is not also proper in case of $G_{cc}(z)$. Hence, the value of $I_L(z)$ is predicted from its past and present values ahead of two sampling instant by extrapolation. A linear extrapolation used for such a purpose yields

$$i_L(k+2) \approx 3i_L(k) - 2i_L(k-1) \tag{17}$$

The feasible form of transfer function $G_D(z)$ is given by from Eq. (17)

$$G_D(z) = \frac{3z-2}{z^3} \tag{18}$$

Consequently, the internal model controller has the following form

$$V_L(z) = G_{cc}(z)[I_C^*(z) - \hat{I}_C(z)] + G_D(z)I_L(z) \tag{19}$$

3. VOLTAGE CONTROL USING RESONANCE MODEL

The voltage control loop using resonance model is shown in Fig. 3. In Fig. 3, the plant transfer function of voltage control loop is given by

$$G_{pv}(z) = \frac{T_{sv}}{C_f(z-1)} \tag{20}$$

where, C_f is the filter capacitor and T_{sv} is the sampling period of the voltage control loop, respectively.

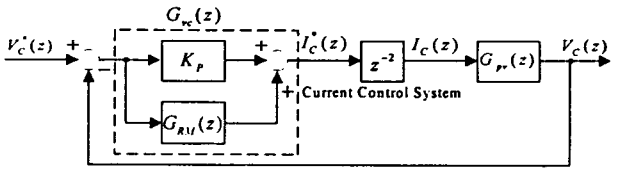

Fig. 3 Block diagram of voltage control loop

In the proposed voltage control loop, P controller with resonance model, which exhibits a function similar to an integrator for AC component, is employed to eliminate the steady state error. The s-domain transfer function of resonance model is given by

$$G_{RM}(s) = \frac{k_r\left(\cos\theta_r\omega_r s - \sin\theta_r\omega_r^2\right)}{s^2 + \omega_r^2} \tag{21}$$

where, k_r and ω_r are a control gain and resonant frequency of resonance model, respectively. θ_r is a parameter for the adjustment of the phase angle of the resonance model at the resonant frequency to compensate a phase error. Note that the value of $G_{RM}(s)$ goes to infinity when $s = j\omega_r$. In this case, the resonant frequency

is set to the fundamental frequency of the reference voltage, thus it eliminates the steady state error of the voltage control loop.

For the investigation of the effect of k_r, Bode plots of resonance model when $\theta_r = 0$ are shown in Fig. 4. From this figure, the control gain k_r is the bandwidth of resonance model. If k_r is large, the voltage control loop is achieved a faster transient response, but the resulting system is unstable. Therefore, the selection of k_r is a trade-off between transient response and stability of the voltage control loop. To meet this requirement, k_r is set to 0.4 in simulation and experiment.

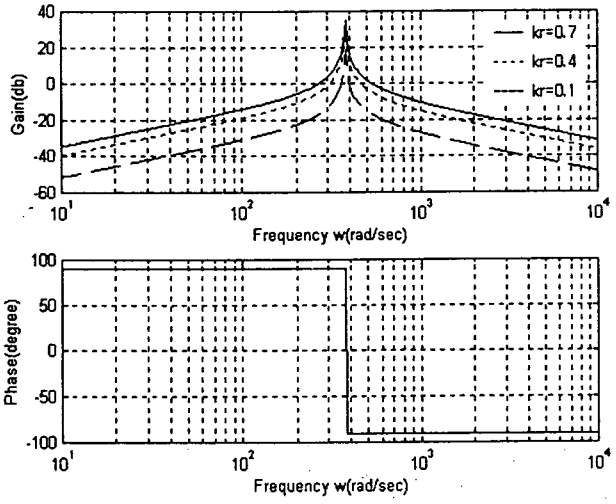

Fig. 4 Bode plots of resonance model when $\theta_r = 0$

For the convenience in the investigation of θ_r, we will consider resonance model with a finite quality factor. When the quality factor is Q, the transfer function of resonance model is given by

$$G'_{RM}(s) = \frac{k_r\left(\cos\theta_r \omega_r s - \sin\theta_r \omega_r^2\right)}{s^2 + \omega_r s/Q + \omega_r^2} \tag{22}$$

Substituting $s = j\omega_r$ in Eq. (22), we can obtain the characteristics of resonance model at the resonant frequency.

$$\left[G'_{RM}(s)\right]_{s=j\omega_r} = k_r Q(\cos\theta_r + j\sin\theta_r) \tag{23}$$

From this result, we can see that the phase angle of the transfer function given by Eq. (22) is θ_r at the resonant frequency ω_r. Resonance model whose transfer function in Eq. (21) is a special case in which the quality factor Q is infinity.

The zero-order-hold equivalent form of the transfer function $G_{RM}(s)$ is given by

$$G_{RM}(z) = \frac{k_r\omega_r\left\{\alpha z^2 - (\alpha\cos\omega_r T_{sv} + \beta\sin\omega_r T_{sv})z\right\}}{z^2 - 2\cos\omega_r T_{sv} z + 1} \tag{24}$$

where, $\alpha = \cos\theta_r$, $\beta = \sin\theta_r$.

The transfer function of the voltage control loop is derived as the following

$$\frac{V_C(z)}{V_C^*(z)} = \frac{\{G_{RM(z)} + K_P\}G_{cc}(z)G_{pv}(z)}{1 + \{G_{RM(z)} + K_P\}G_{cc}(z)G_{pv}(z)} \tag{25}$$

Substituting $z = e^{j\omega_r T_{sv}}$ in Eq. (25), we can obtain the following

$$\left[\frac{V_C(z)}{V_C^*(z)}\right]_{z=e^{j\omega_r T_{sv}}} = 1 \tag{26}$$

From the Eq. (26), we can see that the output voltage coincides exactly with its reference, thus the voltage control loop causes no steady state error as regard to both magnitude and phase.

The phase lag of the reference-to-output transfer function in Eq. (13) produces appreciable phase error between the reference and actual currents. Therefore, the phase angle of resonance model is set to an equal and opposite phase shift, the phase error of the reference-to-output transfer function is compensated automatically.

4. SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed system, simulation and experiment are carried out. Simulation and experiment are performed by PSIM and 1kVA prototype, respectively. The system parameters for simulation and experiment are listed in Table 1.

The simulation results of the reference and output voltage with resistor load are shown in Fig. 5. Note that the output voltage coincides exactly with its reference, thus the proposed system causes no steady state error as regard to both magnitude and phase. The simulation results of the load current and prediction load current with rectifier load are shown in Fig. 6. It is noted that the predicted load current is the exact replica of the load current with a time lag of two sampling intervals.

The experimental results of the output voltage and load current with resistor load, when resistor load is varied suddenly, and with rectifier load are shown in Fig. 7, Fig. 8, and Fig. 9, respectively. From the experimental results, the proposed system is achieved the robust characteristics to the calculation time delay and parameter variation as well as very fast dynamic performance.

5.CONCLUSION

In this paper, a new fully digital control method for single-phase UPS inverter, which is based on the double control loop such as the outer voltage control loop and inner current control loop, is proposed. The inner current control loop consists of two parts; an Internal Model controller and a modeling error feedback loop which incorporates an explicit representation of the UPS inverter system nominal. In the proposed scheme, the outer voltage control loop employing P controller with resonance model implemented by a DSP is introduced. The proposed control scheme are implemented without a dq coordinate transformation, therefore it can be suitable for single-phase UPS inverter to which such coordinate transformation is not applicable. The effectiveness of the proposed control

system has been demonstrated by the simulation and experimental results respectively. From the simulation and experimental results, the proposed system is achieved the robust characteristics to the calculation time delay and parameter variation as well as very fast dynamic performance, thus it can be effectively applied to the power supply for the critical load.

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Table 1 System Parameters

DC Link Voltage	200[V]
Output voltage	100[V](RMS), 60[Hz]
Switching Frequency	20[kHz]
Filter Inductance	1.2[mH]
ESR of Filter Inductance	0.7[Ω]
Filter Capacitance	10[μF]
Load Resistance	10[Ω]

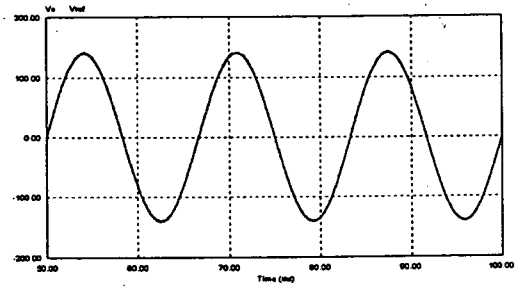

Fig. 5 Simulation results of the reference and output voltage with resistor load

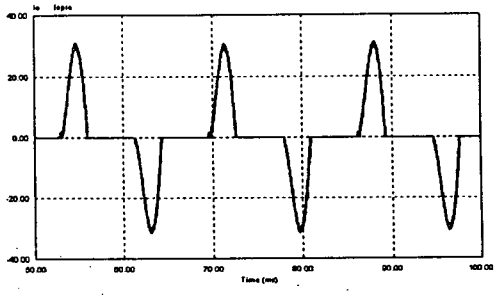

Fig. 6 Simulation results of the load current and prediction load current with rectifier load

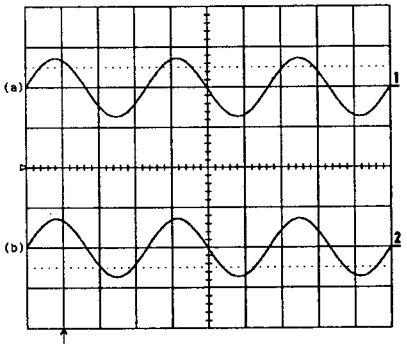

Fig. 7 Experimental results of the output voltage and load current with resistor load

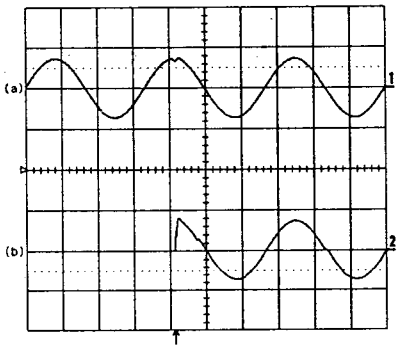

Fig. 8 Experimental results of the output voltage and load current when resistor load is varied suddenly

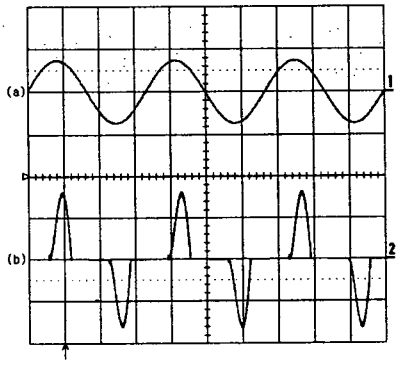

Fig. 9 Experimental results of the output voltage and load current with rectifier load