A New On-line Dead-Time Compensation Method Based on Time Delay Control Technique

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ABSTRACT - **In this paper, an on-line dead-time compensation method based on a time delay control approach is presented. The disturbance voltages caused by the dead time are estimated in an on-line manner by the time delay control without any additional circuits and off-line experimental measurements. And the estimated disturbance voltages are fed to voltage references in order to compensate the dead-time effects. The proposed method is applied to a PM synchronous motor drive system and implemented by using software of a digital signal processor (DSP) TMS320C31. Experiments are carried out for this system and the results well demonstrate the effectiveness of the proposed method.**

I. INTRODUCTION

In recent years, due to the development of high speed switching devices such as power transistors and insulated gate bipolar transistors (IGBT's), pulse width modulated (PWM) voltage source inverters (VSI's) are widely used in adjustable speed motor drives.

In a PWM VSI, because of a dead time which is inevitable to prevent the simultaneous conduction of two switching devices in each leg of the inverter, a distortion of the inverter output voltage, which is called as '*dead-time effects*', arises. The distortion of the inverter output voltage affects machine currents so that a phase current distortion, torque pulsations and degradations of control performance are caused [3]-[10].

In order to overcome the above problem due to the dead time, various approaches are presented. The one is based on modified PWM gate signals, where these signals are made from either hardware correction circuits [3]-[5] or a software correction circuit in [6]. The other is based on a feedforward approach, where the compensating voltages obtained from current polarities and prescribed values are fed to the voltage references [7]-[10]. Non-ideal switching characteristics of the power device such as finite switching times and voltage drops of switching devices are also considered in some approaches[8][9].

However, most previous approaches are only implemented by off-line manners. It is difficult to compensate the dead-time effects perfectly by off-line manners since the switching times and voltage drops of the power devices are varied with operating conditions such as the DC link voltage, phase currents, operating frequency, and motor speed [10]. Although an on-line method is proposed in [10], the method needs additional hardware circuits such as a zero crossing detector and a time counter together with off-line experimental measurements to set up a look-up table.

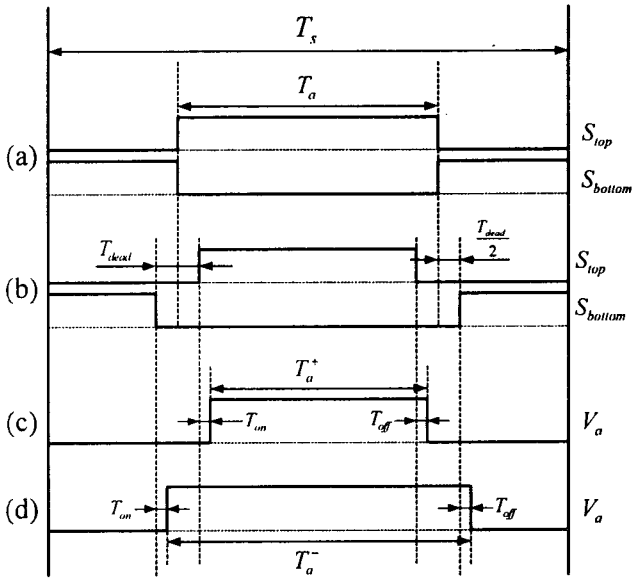

Fig. 1. Practical switching pattern. (a) ideal gate signal patterns. (b) practical gate signal pattern with consideration of dead time. (c) actual output voltage with consideration of dead time and switching time for $i_{as} > 0$. (d) actual output voltage with consideration of dead time and switching time for $i_{as} < 0$.

Thus, in this paper, a new on-line dead-time compensation method is proposed. The proposed method does not need any additional hardware circuits and off-line experimental measurements. The disturbance voltages caused by the dead time are estimated by a time delay control approach and fed to voltage references in order to compensate the dead-time effects. The proposed method is applied to a PM synchronous motor drive system and implemented in a digital manner using a digital signal processor (DSP) TMS320C31. The experiments are carried out for this system to show the effectiveness of the proposed method.

II. ANALYSIS OF DEAD-TIME EFFECT

Since a switching device has a finite switching time, a dead time should be considered in the PWM gate signals in order to prevent the simultaneous conduction of two switching devices in each leg of the inverter. In other words, a top switching of one phase leg should be turned off before a bottom switching the leg is turned on and vice versa. Although the dead time is very short as a few μsecs and guarantees a safe operation of the inverter, it adversely causes the performance degradation.

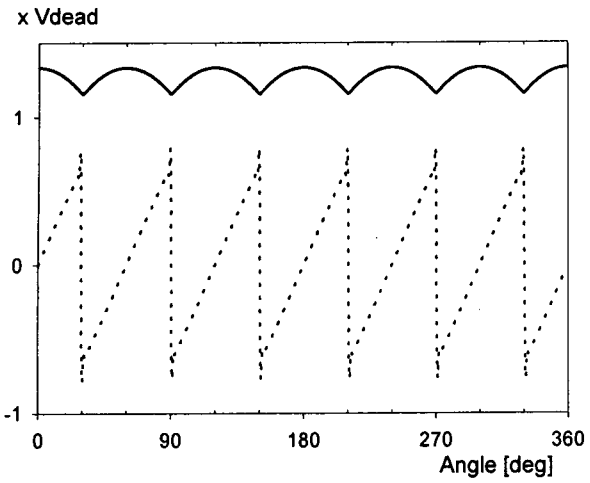

Fig. 2. Disturbance voltages in the synchronous reference frame (Solid line : q-axis disturbance voltage $V^r_{q,dead}$, Dotted line: d-axis disturbance voltage $V^r_{d,dead}$).

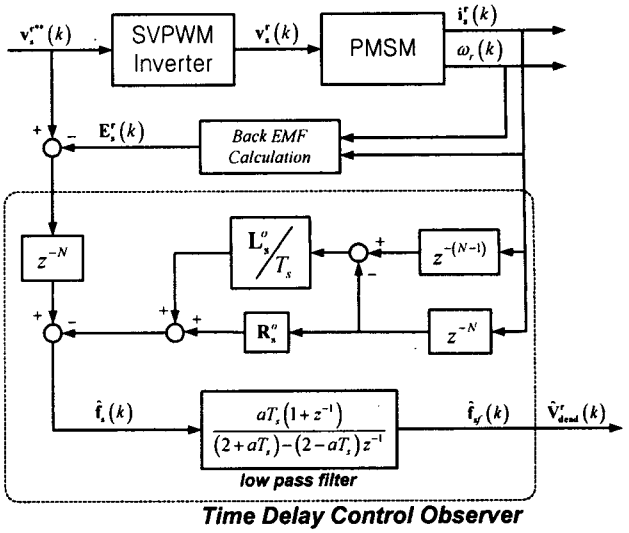

Fig. 3. Disturbance voltage estimation using time delay control.

It is convenient to analyze the dead-time effects from one phase leg of the inverter and extend the results to the other phase legs. During the dead-time period T_{dead}, both the main switching devices in the same leg are turned off and the output voltage therefore depends on the direction of the phase current i_{as}. Fig. 1(a) shows the ideal gate signal pattern and Fig. 1(b) shows the practical gate signal pattern considering the dead time. When the phase current is positive/negative, the phase current flows through the bottom/top diode during the dead-time period. Thus, during the dead-time period, the switching device in the bottom/top side is considered to be turned on, and Figs. 1(c) and (d) show the output voltage, respectively. From these figures, the output voltage errors caused by the dead time and switching time delays can be obtained as follows.

$$T_{a.err} = \left(T_{dead} + T_{on} - T_{off}\right) \cdot \mathrm{sgn}\left(i_{as}\right) \quad (1)$$

$$V_{a.dead} = \frac{T_{a.err}}{T_s} V_{dc} = V_{dead} \cdot \mathrm{sgn}\left(i_{as}\right) \quad (2)$$

where

$$\mathrm{sgn}\left(i_{as}\right) = \begin{cases} 1 & : i_{as} > 0 \\ -1 & : i_{as} < 0 \end{cases}, \quad V_{dead} = \frac{T_{dead} + T_{on} - T_{off}}{T_s} \cdot V_{dc}.$$

Additionally, the voltage drops of switching device can be considered as follow [9, 10]:

$$V_{dead} = \frac{T_{dead} + T_{on} - T_{off}}{T_s} \cdot \left(V_{dc} - V_{sat} + V_d\right) + \frac{V_{sat} + V_d}{2} \quad (3)$$

where V_{sat}, V_d are a saturation voltage drop of the active switch and a forward voltage drop of the freewheeling diode, respectively. In a similar way, the out put voltage errors of the other phases can be obtained. The output voltage errors caused by the dead time and the switching times can be considered as *'disturbance voltages'*.

The disturbance voltages in *abc* frame can be transformed to the synchronous reference *dq* frame as follows:

$$\begin{bmatrix} V^r_{q.dead} \\ V^r_{d.dead} \end{bmatrix} = V_{dead} \cdot \frac{2}{3} \begin{bmatrix} \cos(\theta_r) & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ \sin(\theta_r) & \sin\left(\theta_r - \frac{2\pi}{3}\right) & \sin\left(\theta_r + \frac{2\pi}{3}\right) \end{bmatrix} \cdot \begin{bmatrix} \mathrm{sgn}\left(i^r_{qs}\cos\theta_r + i^r_{ds}\sin\theta_r\right) \\ \mathrm{sgn}\left(i^r_{qs}\cos\left(\theta_r - \frac{2\pi}{3}\right) + i^r_{qs}\sin\left(\theta_r - \frac{2\pi}{3}\right)\right) \\ \mathrm{sgn}\left(i^r_{qs}\cos\left(\theta_r + \frac{2\pi}{3}\right) + i^r_{qs}\sin\left(\theta_r + \frac{2\pi}{3}\right)\right) \end{bmatrix} \quad (4)$$

By employing the concept of the field orientation, that is, d axis current i^r_{ds} is controlled to be zero, the disturbance voltages can be illustrated with respect to the electrical position θ_r as shown in Fig. 2.

The magnitude of the disturbance voltages in the synchronous reference frame is a function of V_{dead} in (3). While the dead time is fixed a value and the DC link voltage can be measured generally, the switching times and voltage drops of switching device are varying with the operating conditions such as the DC link voltage and currents. Moreover, are also varying with the operating condition. Moreover, the measurements of switching times and the voltage drops are very difficult. Thus, it is difficult to compensate the dead time in off-line manner perfectly.

III. ESTIMATION AND COMPENSATION OF DEAD-TIME EFFECT

The disturbance voltages due to the dead-time effects cause the inverter output voltage distortion, which results in the phase current distortion and torque ripple. Moreover, the magnitude of the disturbance voltages in (3) is a function of a dead time, switching-time delays, voltage drops of switching device, and a DC link voltage. While the dead time is a fixed value and the DC link voltage can be measured, the switching-time delays and voltage drops of the switching devices are varying with the operating conditions. Since it is very difficult to measure the

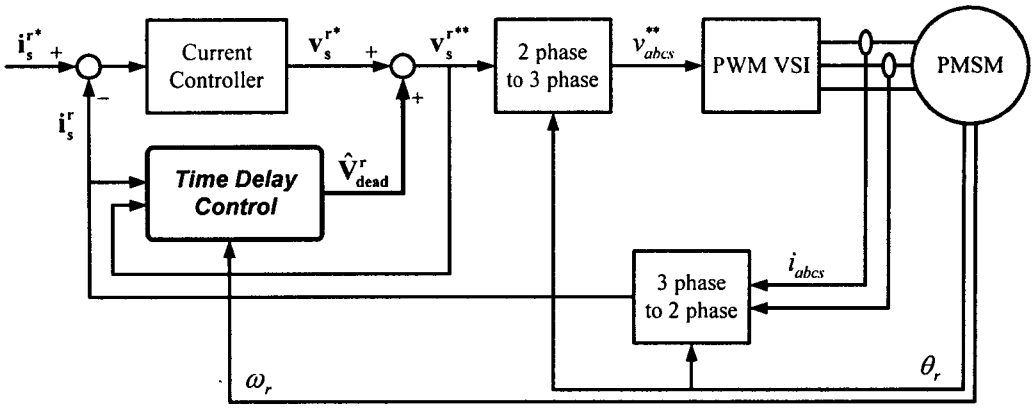

Fig. 4. Block diagram of the proposed compensation scheme.

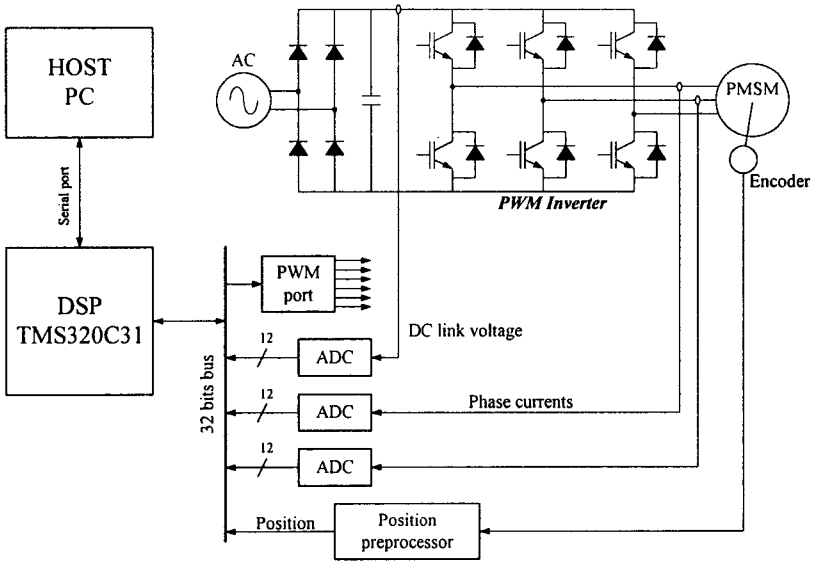

Fig. 5. Configuration of DSP-based control system for PM synchronous motor.

switching-time delays and voltage drops, the perfect dead-time compensation in an off-line manner is not easy.

To overcome the above problems, a new on-line dead-time compensation method is proposed. The proposed method consists of a simple observer and a feedforward loop, and does not require any additional hardware circuits and off-line experimental measurements. The disturbance voltages are estimated by a disturbance voltage observer based on a time delay control approach.

The electrical modeling in the discrete-time domain of the PM synchronous motor and inverter including the disturbance voltages due to the dead-time effects irepresented as follows:

$$\mathbf{v}_s^{r**}(k) = \mathbf{r}_s \mathbf{i}_s^r(k) + \mathbf{L}_s \frac{\mathbf{i}_s^r(k+1) - \mathbf{i}_s^r(k)}{T_s} + \mathbf{E}_s^r(k) + \mathbf{f}_s(k) \quad (5)$$

where

$$\mathbf{v}_s^{r**} = \begin{bmatrix} v_{ds}^{r**} & v_{ds}^{r**} \end{bmatrix}^T, \quad \mathbf{i}_s^r = \begin{bmatrix} i_{ds}^r & i_{qs}^r \end{bmatrix}^T,$$

$$\mathbf{E}_s^r = \begin{bmatrix} -L_q i_{ds}^r \omega_r & L_d i_{qs}^r \omega_r + \lambda_m \omega_r \end{bmatrix}^T,$$

and T_s is a sampling period and $\mathbf{f}_s$ is the disturbance voltages due to dead-time effects and parameter mismatching and represented as follows:

$$\mathbf{f}_s = \begin{bmatrix} f_{ds} & f_{qs} \end{bmatrix}^T = \begin{bmatrix} V_{d,dead}^r + \Delta V_{ds} & V_{q,dead}^r + \Delta V_{qs} \end{bmatrix}^T.$$

In order to estimate the disturbance voltages in the time delay control, it is assume that the variations of the disturbance voltages during a sampling period are nearly zero as follows [11], [12]:

$$\mathbf{f}_s(k) \cong \mathbf{f}_s(k-1). \quad (6)$$

By (6), the disturbance voltages at present time k can be approximated with those of one step previous time as follows:

$$\hat{\mathbf{f}}_s(k) \cong \mathbf{f}_s(k-1)$$

$$= \mathbf{v}_s^{r**}(k-1) - \left(\mathbf{r}_s \mathbf{i}_s^r(k-1) + \mathbf{L}_s \frac{\mathbf{i}_s^r(k) - \mathbf{i}_s^r(k-1)}{T_s} + \mathbf{E}_s^r(k-1) \right) \quad (7)$$

where the symbol '$\wedge$' denotes the estimated value.

TABLE I
SPECIFICATIONS OF EXPERIMENTAL SYSTEM

DC link voltage	310 [V]	Sampling period	150 [μsec]
Dead time	3.6 [μsec]	Switching device	IGBT module
Turn-on time*	0.8-2.0 [μsec]	Turn-off time*	2.0-2.9 [μsec]
Saturation voltage*	1.8-2.7 [V]	Diode forward voltage*	2.2-3.3 [V]

*: Data book (Mitsubishi)

TABLE II
SPECIFICATIONS OF TEST MOTOR

Motor type	PMSM	Number of poles	8
Rated power	750 [W]	Rated speed	3000 [rpm]
Rated torque	2.4 [Nm]	Linkage flux	0.0667 [Wb]
Stator resistance	4.9 [Ω]	Stator inductance	6.9 [mH]

Because of the numerical difference term between the measured currents which may include high frequency noises, it is difficult to use directly the estimated disturbance voltages in (7). Thus, a low pass filter is employed to reduce the effects of the measurement noises. A simple first order low pass filter in the discrete-time domain can be represented as follows:

$$G(z)=\frac{aT_s\left(1+z^{-1}\right)}{\left(2+aT_s\right)-\left(2-aT_s\right)z^{-1}} \qquad (8)$$

where a is a cut-off frequency of the low pass filter. Using (8), the filtered estimates for the disturbance voltages can be obtained as follows:

$$\hat{\mathbf{f}}_{sf}(k)=\frac{2-aT_s}{2+aT_s}\hat{\mathbf{f}}_{sf}(k-1)+\frac{aT_s}{2+aT_s}\left(\hat{\mathbf{f}}_s(k)+\hat{\mathbf{f}}_s(k-1)\right). \quad (9)$$

The disturbance voltage observer is based on a time delay control as shown in Fig. 3. And the estimated disturbance voltages are fed to voltage references in order to compensate the dead-time effects as shown in Fig. 4.

IV. EXPERIMENTAL RESULTS

The proposed compensation method is realized in a DSP-based control system of the PM synchronous motor as shown in Fig. 5. The processor is the floating-point DSP (TMS320C31-40) with a clock of 40MHz. Hall effect devices are used to measure phase currents and a DC link voltage, and the measured signal are converted to digital values by using analog-to-digital converters (ADC's) with a resolution of 12 bits. An absolute encoder with a resolution of 11-bit/rev and a position preprocessor are employed to obtain the position information on the rotor. The three-phase PWM inverter is constructed by using the intelligent power module including six IGBT's, gate drives, and protection circuits. The sampling time of the system is set as 150 μsec. An 8-pole PM synchronous motor is used for the test motor. The other specifications of the experimental system and the test motor are shown in Table 1 and 2, respectively.

Fig. 6 shows the estimated dq-axis disturbance voltages in the synchronous reference frame, when the motor is operated at 150 rpm. The estimated disturbance voltages show the nearly same waveforms as the simulation results as shown in Fig. 2. The levels of the estimated disturbance voltages are some different from the results of simulation in Fig. 2. However, it is due to the operating condition of the PWM inverter.

Fig. 7 shows the dq-axis current waveforms of the three schemes for the step change of the current reference (q-axis current: 0 → 3A). In the no compensation scheme, the dead time causes the undesired current pulsations about six times of electrical frequency in the dq-axis currents and the distortion in the phase current as shown in Fig. 7(a). Moreover, the dynamic behavior of current control is very slow as over 20msec. In the proposed scheme, the dq-axis current pulsations and the distortion in the phase current waveform are remarkably reduced and the dynamic behavior becomes fast as shown in the Fig. 7(b).

The phase current waveforms and their spectra where the motor is operated at 150 rpm are shown in Fig. 8. In the proposed scheme as shown in Fig. 8(b), the phase current has less 5th and 7th harmonics components than the phase current in the no compensation scheme as shown in Fig. 8(a).

V. CONCLUSIONS

A new on-line dead-time effects compensation method is proposed. The previous approaches are based on the additional hardware circuits or off-line experimental measurements. However, the magnitude of the disturbance voltages is varying with the operating condition and an on-line measurement of the magnitude is very difficult. Thus, in this paper, a new on-line dead-time compensation method is proposed. The proposed method compensates in on-line manner the effects caused by the dead-time and non-ideal switching characteristics of the power devices without additional circuits and off-line experiments. The

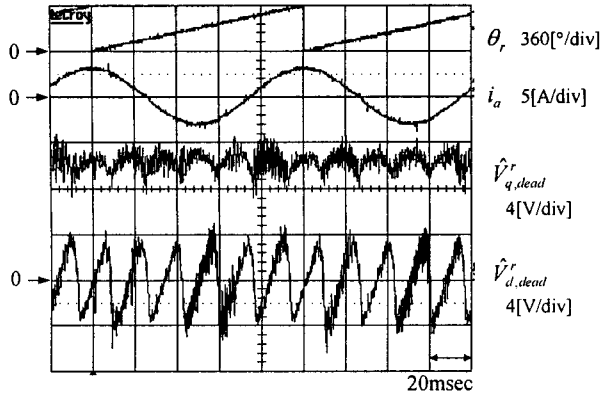

Fig.6. Estimation of disturbance voltages.

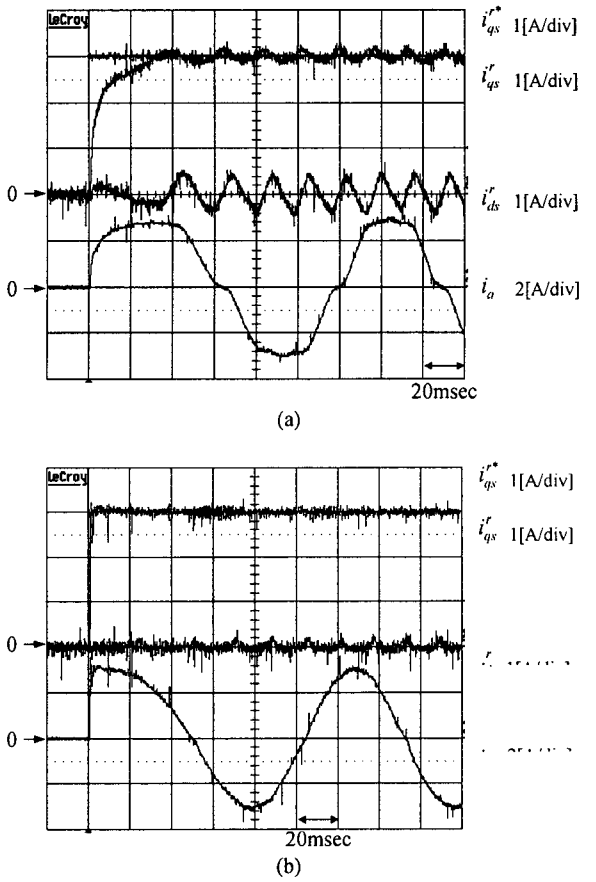

Fig. 7. Step response of current control. (a) without dead time compensation. (b) with dead time compensation using proposed method.

disturbance voltages are estimated by using a time delay control approach and fed to the voltage references.

To show the effectiveness, the simulations and experiments are carried out in the PM synchronous motor drive system. The simulation and experimental results show the better performance of the proposed method and verify its validity. The proposed method can be applied to the high precision PM synchronous motor drive system.

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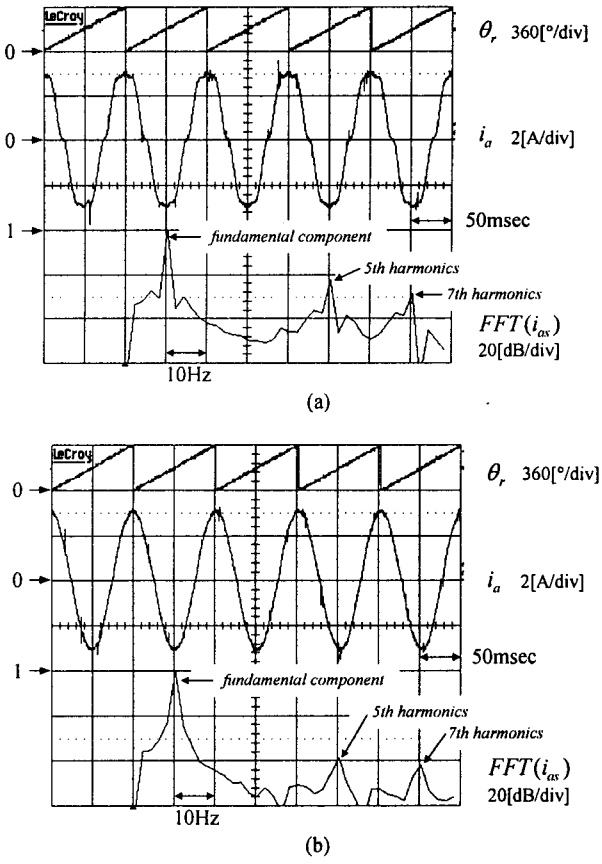

Fig. 8. Phase current waveforms and spectra. (a) without dead time compensation. (b) with dead time compensation using proposed method.

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