Design of Deadbeat DSP Controlled PWM Inverter With Two-Level Switching Pattern

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Abstract

In this paper, a two-level switching algorithm of the deadbeat to control PWM inverter is proposed. A modified algorithm of the deadbeat is suitable for the UPS system. Two levels in the pulse pattern are used. This scheme allows the use of higher switching frequency for a given computation time delay, which results in lower total harmonic distortion at the output. The proposed control scheme is implemented using TMS320F240 DSP chip for controlling on inverter.

1. Introduction

Recent developments in power semiconductor device technology are able to be of faster switching capability at high power. Applications of switching devices such as the IGBT and MOSFET achieve very high switching frequency PWM(Pulse Width Modulation) inverters [1][2]. With the availability of high-frequency switching devices, IFC(Instantaneous Feedback Control) was developed. This technique has good transient response. Although the IFC is an analog real-time control and it has the disadvantage concerned with large harmonic amplitudes relatively.

A digital feedback approach using μ-processor deadbeat control scheme was proposed[3]. The analog values in the PWM inverter have to be converted into a discrete time system, and deadbeat control is applied with state feedback. This type of approach has very fast transient response and compensates well for load disturbances. The disadvantage of the digital approach is that the width of the pulse is limited.

DSP's(Digital Signal Processors) are now being applied for the control of power electronics and drive systems. A DSP has much faster speed characteristics than a general microprocessor. A digital controller(the Texas TMS320F240) was used to implement the control algorithm and provide switching signals to the power circuit[4].

2. State model

In Fig. 1, a basic circuit for the deadbeat controlled PWM inverter with two-level switching pattern is shown.

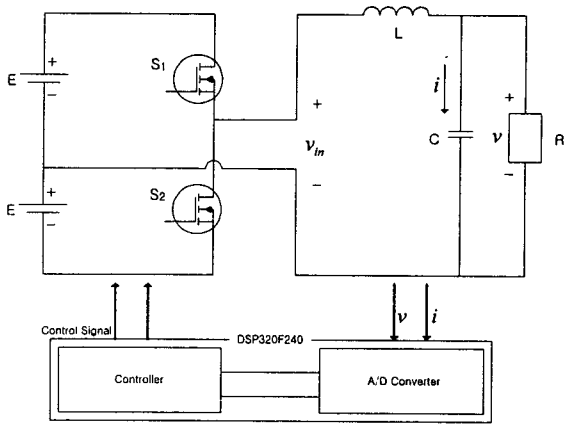

Fig. 1. Circuit diagram of two-level deadbeat controlled PWM inverter

The inverter, LC filter and resistive load are considered as the "plant" of a closed-loop digital feedback system with a sinusoidal reference. The PWM pattern is determined at every sampling instant by controller, based on the output measurements and the reference.

A basic block diagram of a deadbeat controller for the PWM inverter is shown in Fig. 2. This is the equal diagram of the Fig 1. The load voltage and the capacitor current are set as state variables, and then the required pulse width is computed.

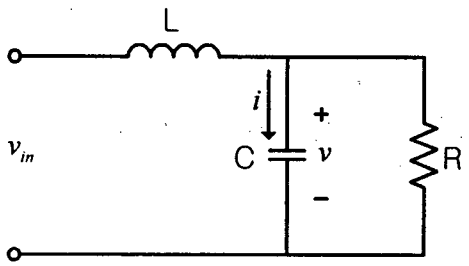

Fig. 2. State model

The circuit shown in Fig. 2 is modeled as a second-order system with the state vector $[v \quad i]'$, where v is the load voltage and i is the capacitor current, The state equation becomes

$$\begin{bmatrix} \dot{v} \\ \dot{i} \end{bmatrix} = A \cdot \begin{bmatrix} v \\ i \end{bmatrix} + B \cdot v_{in} \tag{1}$$

where

$$A = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{1}{RC} \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} \tag{2}$$

3. Two level deadbeat control

The continuous-time domain state eq. (1) can be written as

$$\dot{x} = Ax + Bu \tag{3}$$

where x is a state vector, u is a scalar input, and A is a nonsingular matrix. And the closed-form solution is[5]

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_0 e^{A(t-\tau)}Bu(\tau)d\tau \tag{4}$$

where $x(t_0)$ is the initial state at $t = t_0$.

If the input u is constant for $t_0 \le t \le t_1$, then eq. (4) at $t = t_1$ becomes

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + A^{-1}(e^{A(t_1-t_0)} - 1)Bu \tag{5}$$

Only two switching devices are required to produce two values $+E$ and $-E$ to the filter for a single-phase system. To drive a discrete time model, the PWM pulse pattern shown in Fig. 3 is considered, which is the waveform of v_{in} within a sample interval T. Using eq. (5), the discrete-time system equation with the input in Fig. 3 is derived as follows.

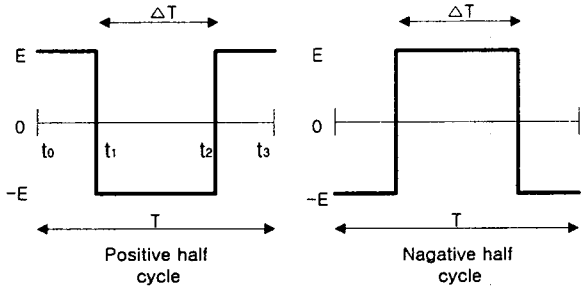

Fig. 3. Two-level PWM pattern

1) For $t_0 \le t \le t_1$, $u = E$, thus at $t = t_1$

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + A^{-1}(e^{A(T-\Delta T)/2} - 1)BE \tag{6}$$

2) For $t_1 \le t \le t_2$, $u = -E$, thus at $t = t_2$

$$x(t_2) = e^{A(t_2-t_0)}x(t_0) + e^{A\Delta T}A^{-1}(e^{A(T-\Delta T)/2} - 1)BE - A^{-1}(e^{A\Delta T} - 1)BE \tag{7}$$

3) For $t_2 \le t \le t_3$, $u = E$, thus at $t = t_3$

$$x(t_3) = e^{AT}x(t_0) + e^{A(T-\Delta T)/2}e^{A\Delta T}A^{-1}(e^{A(T-\Delta T)/2} - 1)\cdot BE - e^{A(T-\Delta T)/2}A^{-1}(e^{A\Delta T} - 1)BE + A^{-1}(e^{A(T-\Delta T)/2} - 1)BE \tag{8}$$

4) After a short calculation with assumptions

$$e^{A\Delta T/2} \approx 1 + A\Delta T/2 + A^2(\Delta T/2)^2/2 \tag{9}$$

$$e^{AT} \approx 1 + AT/2 + (AT)^2/2 + (AT)^3/6 \tag{10}$$

and then eq. (8) becomes

$$x[(k+1)T] = e^{AT}x(kT) - 2e^{AT/2}BE\Delta T + (T + AT^2/2 + A^2T^3/6)BE \tag{11}$$

where

$$(k+1)T = t_3, \quad kt = t_0$$

This is the discrete-time system of eq. (3).
Rewriting eq. (11) gives

$$\begin{bmatrix} v(k+1) \\ i(k+1) \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix} \cdot \begin{bmatrix} v(k) \\ i(k) \end{bmatrix} - \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \cdot \Delta T(k) + \begin{bmatrix} h_1 \\ h_2 \end{bmatrix} \tag{12}$$

where

f_{ij} is the corresponding element of e^{AT}

g_{ij} is the corresponding element of $2e^{AT/2}BE$

h_i is the corresponding element of $(T + AT^2/2 + A^2T^3/6)BE$ and $v(k)$, $i(k)$ and $\Delta T(k)$ represent their values at the sampling time $t = kT$

One cycle of the 60Hz reference sine waveform is divided into N equal intervals of duration T as shown in Fig. 4. In this paper, it is divided by 75. So intervals of duration T is approximately 222[μs].

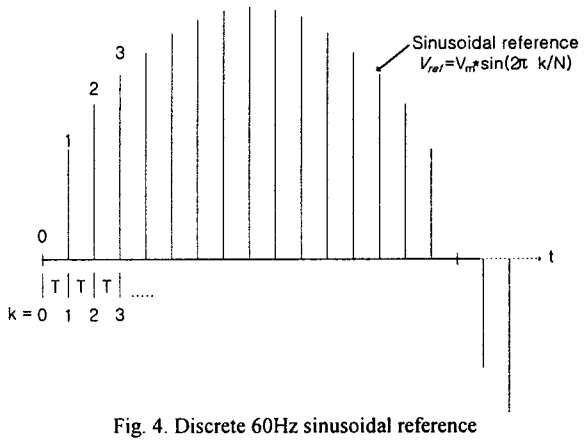

Fig. 4. Discrete 60Hz sinusoidal reference

Taking the first element of eq. (12), the output voltage $v(k+1)$ is

$$v(k+1) = f_{11} \cdot v(k) + f_{12} \cdot i(k) - g_1 \cdot \Delta T(k) + h_1 \quad (13)$$

The required pulse width $\Delta T(k)$ can be computed to make the output voltage $v(k+1)$ equal to the desired reference voltage $v_{ref}(k+1)$ at $t = k+1$. Replacing $v(k+1)$ with $v_{ref}(k+1)$ in eq. (13) and solving for $\Delta T(k)$ gives

$$\Delta T(k) = -v_{ref}(k+1)/g_1 + f_{11}/g_1 \cdot v(k) + f_{12}/g_1 \cdot i(k) + h_1/g_1 \quad (14)$$

This is the deadbeat control rule for the proposed two-level scheme.

4. Computer simulation

To prove the proposed deadbeat control rule with eq. (14). Psim is used for computer simulation[6]. In Psim, the controller is composed as Fig. 5.

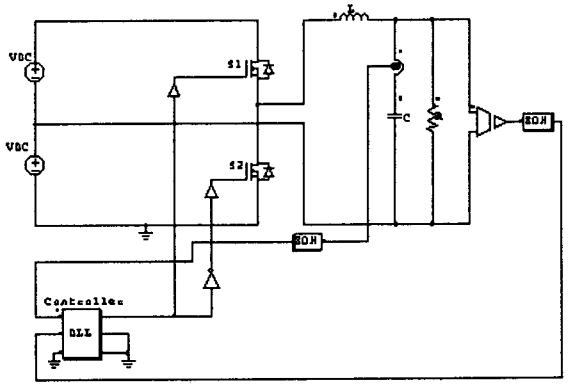

Fig. 5. Configuration of proposed controller

The controller computes the many matrixes using C language.

The simulation parameters in table 1 were used in computing the pulse width .

Table 1. Simulation parameter

DC Voltage	20[V]
L	1[mH]
C	100[μF]
Load	2[Ω]
N(T)	75(222[μs])

Fig. 6 shows switching signal S1 and S2 of proposed controller circuit.

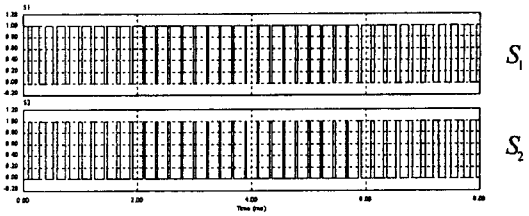

Fig. 6. Switching signal S1 and S2

Fig. 7 shows the output voltage and current waveforms with full-load. The simulated output waveforms are very close to sinusoidal waveforms.

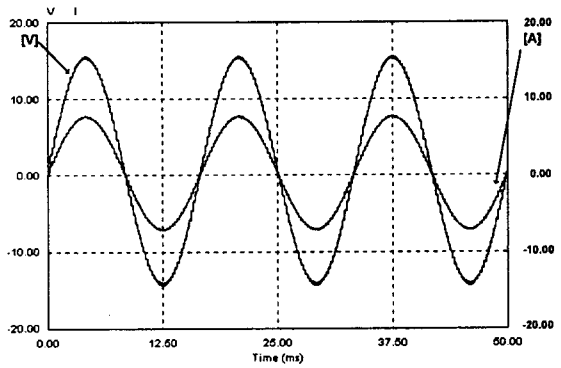

Fig. 7. Simulated output voltage and current waveforms

Fig. 8 shows the simulated output waveforms for load changing with firing angle of 85° . The output voltage drops after the firing instant. The worst waveform at the output for a load changing occurred when firing angle was near the peak of the output. Fig. 8 shows the waveforms recover within 2[ms] and that the controller has very fast response with load changing.

The voltage drop at the output can be improved by decreasing the inductance and increasing the capacitance of the output filter.

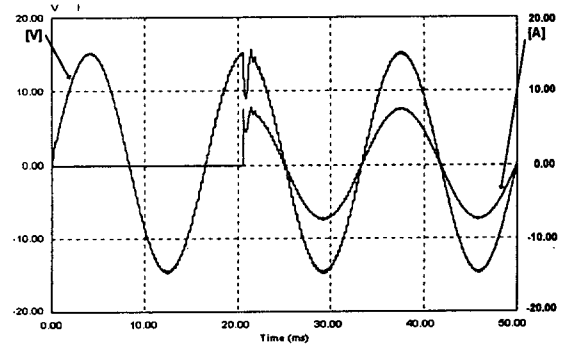

Fig. 8. Simulated output voltage and current waveforms with load changing

5. Experimental results

We design the controller with TMS320F240 which is 16bit Digital Signal Processor(DSP) from Texas Instruments Co. TMS320F240 has two A/D converters. With measured values, the controller decides pulse width. To avoid a arm short, a small deadtime is considered whenever the switching is changed.

Fig. 9 shows the experimental output voltage and current waveforms. The parameters are same in the table 1. We can see that the sinusoidal outputs are similar to simulation results.

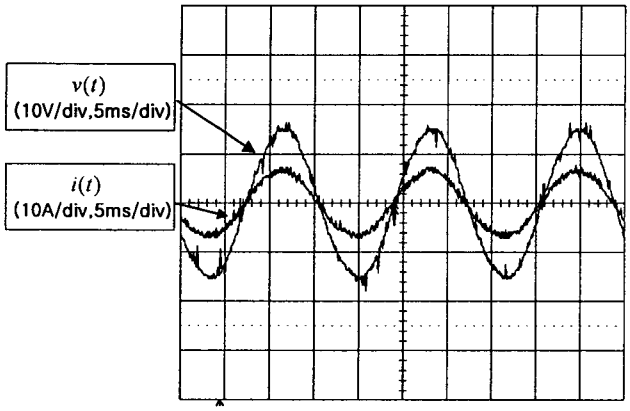

Fig. 9. Experimental output voltage and current waveforms

Fig. 10 shows the output voltage and its FFT result. We can see that the fundamental waveform is dominative.

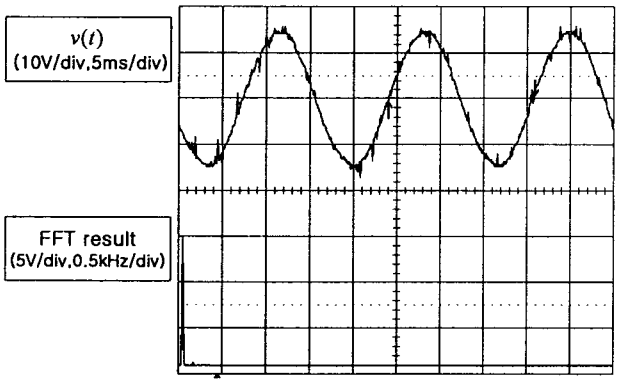

Fig. 10. Output voltage and its FFT result

Fig. 11 shows the output waveforms for load changing. The load is changed with firing angle about 90° . About one and a half it is no-load operating, after that it operates the full-load. And Fig. 11 shows that simulation and experimental results are very close.

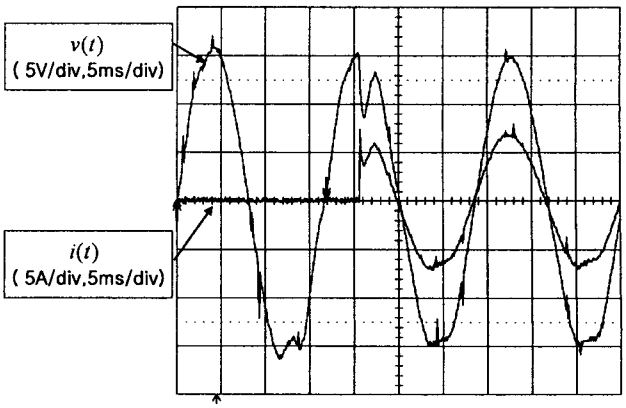

Fig. 11. Experimental waveform with load disturbance

6. Conclusion

A two-level deadbeat controller is proposed to produce a low THD sinusoidal voltage for a single-phase PWM inverter. Two levels are used in the switching pattern. The half-bridge inverter is required a two-supply system ($+E$, $-E$). However, the half-bridge inverter uses fewer switching devices than the full-bridge inverter. The proposed algorithm can be easily expanded to the three-phase inverter. The performance of the two-level deadbeat controlled PWM inverter was theoretically analyzed, simulated by Psim and finally demonstrated experimentally using a TMS320F240. The experimental results are very close to the computer simulation results. The proposed control algorithm has very fast response for load disturbances.

References

[1] Bimal K. Bose, "Power Electronics and Variable Frequency Drives," Ieee Press, 1996

[2] Daniel W. Hart, "Introduction to power electronics," PRENTICE HALL, 1997

[3] K. P. Gokhale, A. Kawamura, and R. G. Hoft, "Deadbeat microprocessor control of PWM inverter for sinusoidal output waveform synthesis," IEEE Trans. Ind. Applicat., Vol. IA-23 No. 2, pp. 901-909, 1987 Sept./Oct.

[4] Texas Instruments, "TMS320C2xx User's Guide," 1995

[5] Chi-Tsong Chen, "Linear System Theory and Design," Oxford University Press, 1999

[6] Powersim Technologies Inc., "PSIM User Manual," 1999 April