Simulations for Square Pulse Generators

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Abstract - The design of square pulse generators using pulse forming lines (PFLs) made up of identical L and C, was reviewed in this study. 14 different types of PFLs were analyzed utilizing PSpice simulation results. These PFLs were characterized with respect to their distinct features: the number of forming lines (single or double), the circuit relationship between PFL and load (parallel or series), the types of energy storage (voltage source, current source or a combination of both).

The characteristic impedances, output parameters such as pulse width, voltage and current magnitudes, and powers were derived for each scheme. The merits and demerits of the output parameters were also included.

I. INTRODUCTION

There are two reasons for using pulse forming lines (PFLs): one is storing the exact amount of energy required for a pulse and the other is discharging this energy into the load in the form of a pulse with a specified pulse shape.

In this study two features are summarized. Firstly, for the single PFLs, the power delivered to a load can be two times different depending on the topology.

Secondly, in the case of double PFLs, the output pulse voltage can be four times different. The choice of the best possible PFL for a given application still remains to be discussed. The PFLs with current sources have important advantages. But, so far the availability of a suitable switch with adequate lifetime and capable of high power operations, still remains a problem. Only some semiconductor switches such as MOSFETs, IGBTs, GTOs, and IGCTs can be used in limited low power applications.

II. ANALYSIS AND CHARACTERIZATION OF PFLs

To generate high power square pulses, pulse forming lines consisting of identical ladder types of L and C element combinations in cascades are generally used. The most widespread are voltage-fed PFLs with capacitive energy storages (CES), in which energy is stored as electric field in the capacitances in single [C-1] or double [C-2] PFL in Table 1 and 2. The stored energy is discharged into load through a closing switch K.

The following nomenclatures are used in study :

U_0 : Source voltage of PFL
U_L : Amplitude of load voltage
I_o : Source current of PFL
I_L : Amplitude of load current
ρ : Characteristic impedance of PFL
P_L: Pulse power on the load
δ : One-way transmission time of PFL
t_p : Pulse duration of the load

PSpice circuit model and simulation result for the pulse generator [C-1] is shown in Fig. 1(a) and (b), respectively.

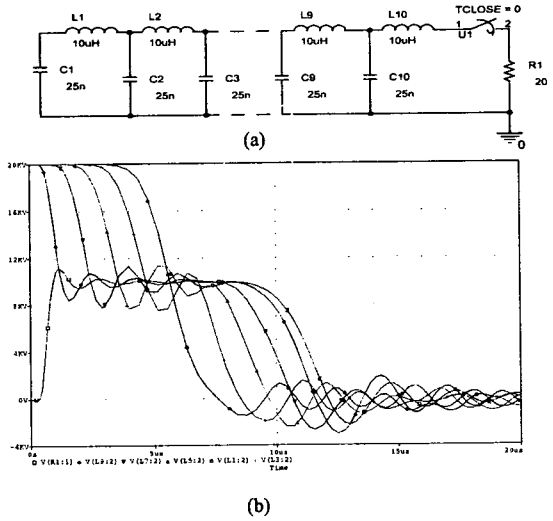


Fig. 1. CES based single PFL with parallel load.

The pulse generator with single PFL, in which output is connected to its input in parallel, is shown in Table 1 referred to as [C-3]. This PFL provides double pulse power on the load with pulse duration of half compared to that of [C-1]. Note that the load resistances are $\rho/2$ for [C-3] and ρ for [C-1]. Hence, the pulse load current is as large as two times.

After connecting the load, the discharging process of the PFL capacitors starts simultaneously from both input and output. Thus, the pulse duration on the load t_p is determined by one-way transmission time of the line as δ. The load resistance for this simulation is equal to half of the characteristic impedance of the PFL. Fig. 2(a) and (b) show the simulation circuit model and result.

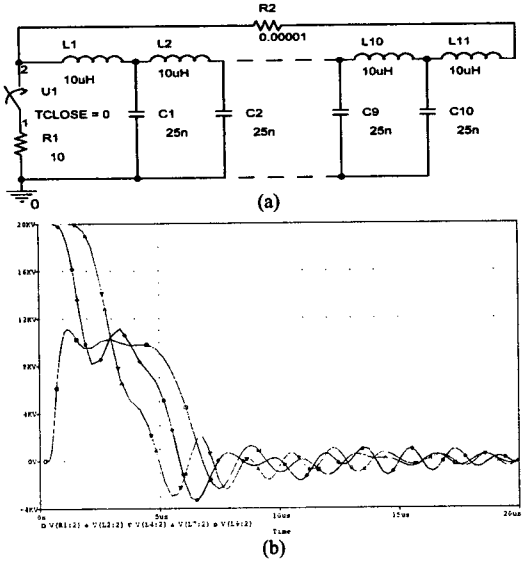
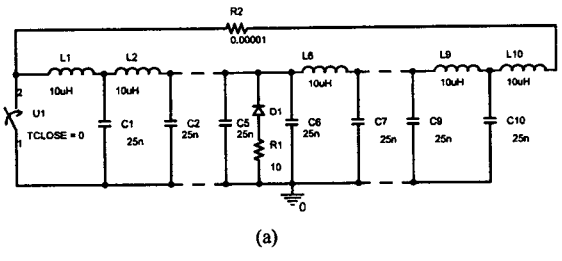


Fig. 2. CES based single PFL with double input.

The pulse generator with single PFL in which output is connected in series with its input and the load through closing switches K1 and K2 is [C-4] in Table 1. By doubling the load voltage, this also provides double pulse power on the load, compared with [C-1], at the cost of half-decreased pulse duration. The load resistance is chosen as two times of the PFL characteristic impedance. However, there is a demerit for this pulse generator: the decay of the pulse load voltage due to series connection of load and the PFL inductances.

The pulse generator with double PFL in which the input of the first PFL is also fed to the second PFL input in parallel and the load in series with a high voltage diode is connected with both PFLs [C-5]. The PFL doubles the load current and the load voltage is half of the source voltage. The pulse power and the pulse duration are equal to Uo/2ρ and 2δ, respectively. The load resistance in this scheme is chosen to be equal to half of the PFL characteristic impedance. PSpice analysis for the pulse generator is shown in Fig. 3.



Inductor energy storages (IES) can also be used for PFLs. The merits of the IES are higher energy density and capability of transforming low source voltage to high pulse load voltage. Opening switches are required for the use of the IES.

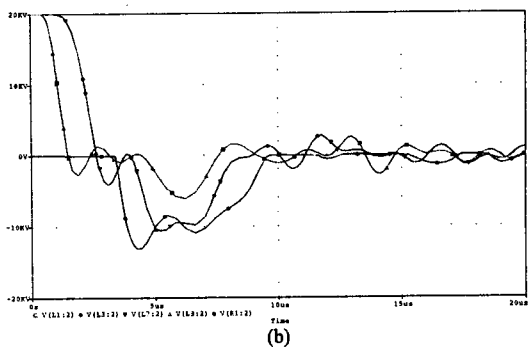


Fig. 3. CES based double PFL with parallel load.

Forming of high-voltage square pulses by a pulse generator based on a single PFL with an IES is shown in [C-6]. The inductors of the PFL are charged by a current source up to I_0 through an opening switch K. A pulse voltage is formed on the load of which resistance is equal to the PFL characteristic impedance. The pulse current, pulse voltage, pulse duration, and pulse power on the load are given as $I_0/2$, $I_0\rho/2$, 2δ, and $I_0^2\rho/2$, respectively. One forth of the initially stored energy in the PFL inductance is transferred on the load. The Pulse duration of PFL capacitor voltages is equal to or less than (particularly, the capacitor next to the PFL output) the pulse duration on the load. Therefore, energy densities of the capacitors in the IES based PFLs may be significantly higher than those of PFLs with CES [C-1]-[C-5]. Corresponding PSpice analyses for the PFL are shown in Fig. 4.

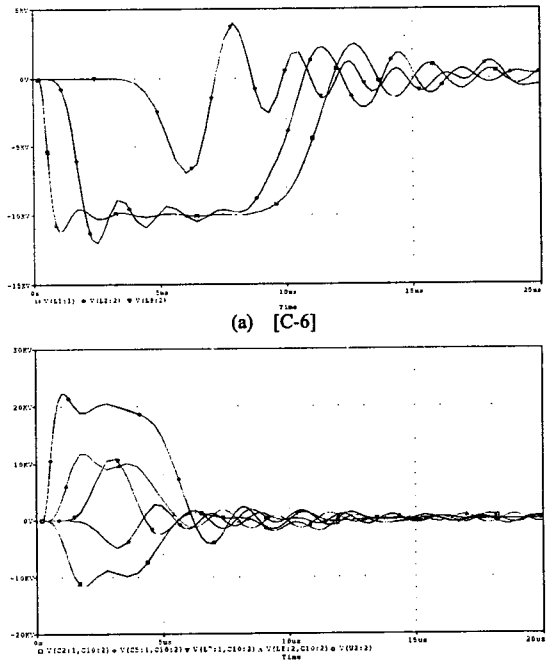
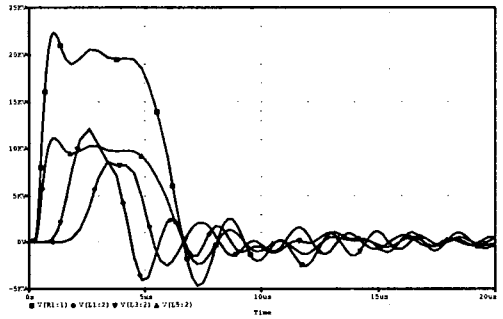


Fig. 4. IES based single PFL.

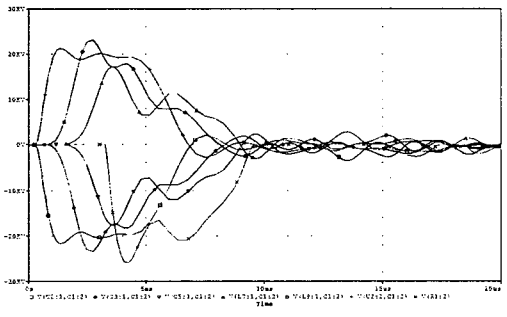
The pulse generator based on single PFL with open-chain ends provides double pulse power on the load is shown [C-7] in Table 1. Power source with an opening switch is connected in parallel with the PFL and the load. Compared with the pulse generator [C-6], the pulse duration is halved and is equal to δ, the one-way transmission time of the PFL. In the moment of opening the switch K voltage polarity is reversed and voltage drops of $\Delta U = \pm I_0 \rho / 2$ are obtained simultaneously on the input and output of the PFL. These are transmitted along the PFL and meet on the load achieving $U_L = 2\Delta U = I_0 \rho$. The output voltage is two times higher than that of [C-6].

The same pulse power with double current magnitude on the load can be achieved using the pulse generator based on the IES with double PFL [C-8]. One end of the second PFL is shorted and the load is connected between PFLs in parallel. The pulse duration on the load is equal to 2δ. The load resistance is chosen to be equal to half of the PFL impedance.

To achieve double amplitude of the load voltage (accordingly with decreased load pulse current), two generators based on double PFL with an IES such as [C-9] and [C-10] can be used. The load is connected between two PFLs in series. The load resistance is to be equal to 2δ, that is, two times of PFL characteristic impedance. PSpice analyses for these [C-9]-[C-10] are shown in Fig. 5(a) and (b). The pulse power on the load can be increased using the stored energy alternately in electric field of capacitors and magnetic field of inductances of PFLs.



(a) [C-9]

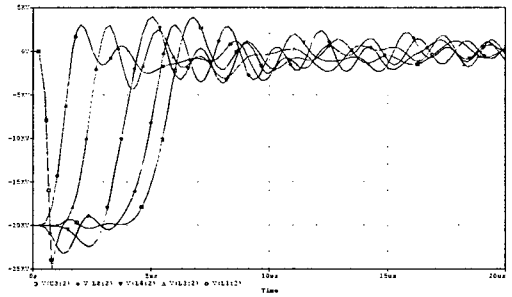


(b) [C-10]

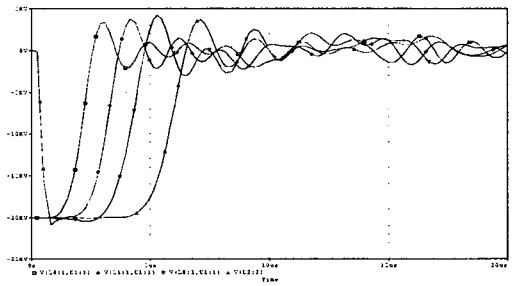
Fig. 5. IES based double PFL.

Scheme [C-11] shows a pulse generator with single PFL. The output of the charging voltage source is the input to the PFL and the current source with an opening switch K2 in series. The current source is connected to the end of the PFL and this is applied to the load R_L through a closing switch K2. In this case the load resistance is equal to the PFL characteristic impedance. The amplitude of the load voltage is equal to the capacitor source voltage U_0 and the load current is equal to the inductor charging current I_0. The pulse duration is equal to the one-way transmission time of the PFL.

The pulses on the load with the same parameters can be formed by a pulse generator based on single PFL by connecting the load parallel to a current source with an opening switch and the PFL as shown [C-12]. Simulation results for the pulse generators [C-11] and [C-12] are shown in Fig. 6.



(a) [C-11]



(b) [C-12]

Fig. 6. CES and IES based single PFL.

To increase the output pulse power on the load twice of the pulse generators [C-1] and [C-2] with keeping the same pulse duration, the CES and IES based double PFLs, [C-13] and [C-14] can be used. The pulse generator [C-13] with the load connected in parallel provides a double pulse load current, whereas [C-14] with the load connected in series provides a double pulse load voltage on the loads.

III. SUMMARY

Pulse forming lines are widely used to generate square pulses. But, in spite of their long history and wide spread

use, they are not yet characterized as a whole. This study highlighted the features of 14 different PFLs. Some of PSpice simulation circuit models and results are also contained for the purposes of verification and comparison.

The PFLs are categorized in Table 1 and 2 with respect to :

i) Number of PFLs: single or double
ii) Energy storage elements: inductors, capacitors or combinations of these
iii) Relative connection of loads and sources: in parallel or in series
iv) Switches: closing, opening

TABLE 1. Single PFLs

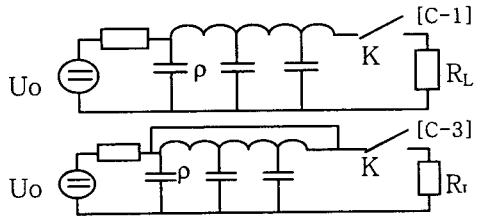
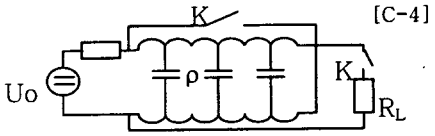
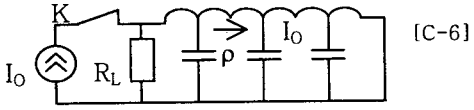
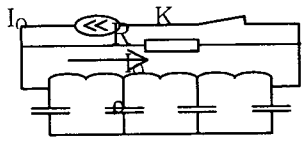
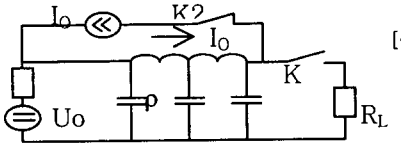
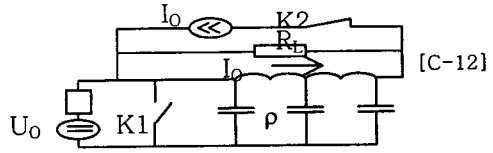
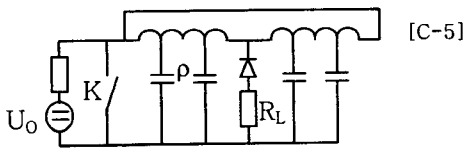
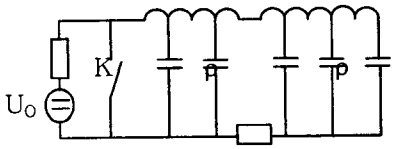
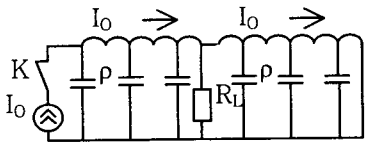
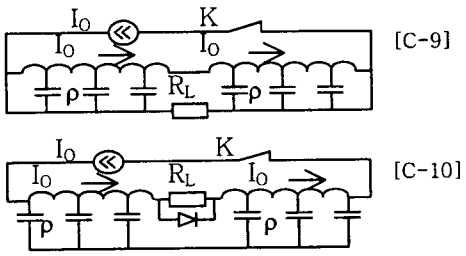
	The load in parallel with PFL	The load in series with PFL
CES		
IES		
CES + IES		

TABLE 2. Double PFLs

	The load in parallel with PFL	The load in series with PFL
CES		
IES		
CES + IES