IGBT Mesh-Topology Modeling And Its Application To Latch-Up Performance

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Abstract — **A new mesh-topology model of IGBT is presented. It can be applied to the research of IGBT's static and dynamic latch-up (du/dt latch-up, overheat latch-up, overload latch-up, overvoltage latch-up) as well as the switching on-off behavior of the device. The overcurrent latch-up is analyzed.**

Keywords— **latch-up, mesh-topology, IGBT**

I. INTRODUCTION

A lot of IGBT mesh models are developed including LIGBT, HIGBT model [1], SPICE model [2], IG-SPICE model [3], the electrothermal model [4] and the comprehensive charge model [6]. These models work well in IGBT's on-state and switching on-off characteristics but are devoid of the latch-up, which is considered a main factor damaging the transistors. The mesh-topology new model of IGBT based on its physical structure is established to determine the latch-up performance; as a result, thereby it is applied to the overcurrent latch-up analysis.

II. ESTABLISHING THE MODEL

The schematic cross-sectional view of IGBT is illustrated in Fig.1, in which the internal parasitic elements are denoted. Fig.2 shows the mesh-topology model. R_A, R_{on}, R_{PB} are the anode-connected resistance, the MOS channel resistance, the resistance of P_2-base and j_3 short circuit zone, respectively; C_{j_1}, C_{j_2}, C_{j_3} are the barrier capacitances; C_{D_1}, C_{D_2}, C_{D_3} are the diffusion capacitances; U_1, U_2, U_3 are the junction voltages; I_{S_1}, I_{S_3}, I_{S_2} are the saturation currents; I_1, I_2, I_3 are the transfer current sources actually the transfer currents caused by the interaction of the parasitic PNP and NPN transistors.

All parameters are ascertained as follows.

1. The three P-N junctions are regarded as the ideal diodes and the currents through are expressed by

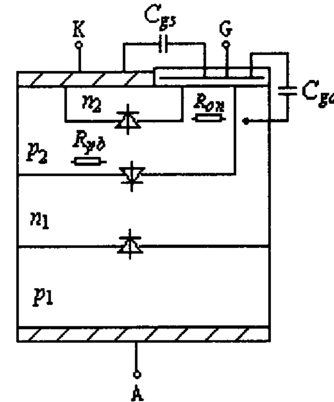

Fig. 1

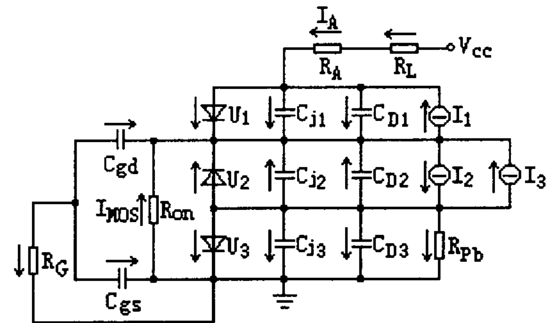

Fig.2

$$i_{D(i)} = I_{s(i)}[\exp(\frac{qU_i}{mkT}) - 1] \quad (i = 1,2,3) \qquad (1)$$

m is the injection level factor ranging between two and four. The saturation currents are influenced by the impurity concentrations and the minority carriers' lifetime.

$$I_{s(i)} = A \cdot q \cdot n_i^2 (\sqrt{\frac{D_P}{\tau_P}} N_D^{-1} + \sqrt{\frac{D_n}{\tau_n}} N_A^{-1}) \qquad (2)$$

A is the effective area of the P-N junction.

2. I_1, I_2, I_3

I_1 is the current component of the MOSFET channel electrons that flows into the N_1-base and then is transported to j_1.

$$I_1 = \beta_{PNP} \cdot I_{MOS} \cdot M_1$$

I_2 is the electron current injected by j_3. It passes through the P_2-base of the NPN transistor and is terminated at j_2.

$$I_2 = \beta_{NPN} \cdot i_{D3} \cdot M_2 \qquad (4)$$

I_3 is the hole current from j_1 to j_2 via the N_1-base of

the PNP transistor.

$$I_3 = \beta_{PNP} \cdot i_{D1} \cdot M_2 \quad (5)$$

β, the base transportation coefficient, is calculated as

$$\beta_{PNP} = \begin{cases} \{1+K_{N_1}[1-W_{N_1}(1+\frac{U_2}{U_{D_2}})^{\frac{1}{m_r}}]^2\}^{-1} & (U_2 < 0.1U_{D_2}) \quad (6) \\ \{1+K_{N_1}[1-W_{N_1}(0.9)^{\frac{1}{m_r}}]^2\}^{-1} & (U_2 \geq 0.1U_{D_2}) \quad (7) \end{cases}$$

$$\beta_{NPN} = \begin{cases} \{1+K_{P_2}[1-W_{P_2}(1+\frac{U_2}{U_{D_2}})^{\frac{1}{m_r}}]^2\}^{-1} & (U_2 < 0.1U_{D_2}) \quad (8) \\ \{1+K_{P_2}[1-W_{P_2}(0.9)^{\frac{1}{m_r}}]^2\}^{-1} & (U_2 \geq 0.1U_{D_2}) \quad (9) \end{cases}$$

m_r is valued 2 for the abrupt junction and 3 for the graded junction; U_{D_2} is figured to be the built-in potential of j_2. $M_{(i)}$ is the avalanche multiplication factor.

$$M_{(i)} = \frac{1}{1-[\frac{U_{(i)}}{U_{B(i)}}]^n} \quad (i=1,2,3) \quad (10)$$

$U_{(i)}$ and $U_{B(i)}$ refer to the impressed voltage and the avalanche breakdown voltage, respectively; n is constant.

3. $C_{j_{(i)}}$

$$C_{j_{(i)}} = \begin{cases} \frac{C_{j0(i)}}{(1-\frac{U_i}{U_{D(i)}})^{\frac{1}{m_r}}} & (U_i < 0.1U_{D_{(i)}},\ i=1,2,3) \quad (11) \\ \frac{C_{j0(i)}}{(0.9)^{\frac{1}{m_r}}} & (U_i < 0.1U_{D_{(i)}},\ i=1,2,3) \quad (12) \end{cases}$$

$C_{j0_{(i)}}$ is the barrier capacitance of zero bias.

4. $C_{D_{(i)}}$

$$C_{D_{(i)}} = g_{(i)} \frac{W_{b(i)}}{2D_{(i)}} \quad (i=1,2,3) \quad (13)$$

The junction conductance is given by $g_{(i)} = \frac{qI_{(i)}}{kT}$; $\frac{W_{b(i)}}{2D_{(i)}}$ is the base transition time, which is capable of being displaced by the lifetime of minority carriers.

5. C_{gd}, C_{gs}

Compliance with the general theory regarding MOSFET is applied.

$$C_{gd} = \frac{2}{3}C_G\{1-\frac{(U_{GS}-U_T)^2}{[2(U_{GS}-U_T)-U_{DS}]^2}\} \quad (14)$$

$$C_{gs} = \frac{2}{3}C_G\{1-\frac{U_{DS}^2}{3[2(U_{GS}-U_T)-U_{DS}]^2}\} \quad (15)$$

where $C_G = W \cdot L \cdot C_{ox}$. C_{ox} is defined as the S_iO_2's capacitance of unit area.

6. R_{on}

The channel resistance of MOSFET in IGBT approximates to its on-state resistance [6].

$$R_{on} = \begin{cases} \frac{V_{DS}}{I_{DS0}} & (off\ area) \quad (16) \\ \frac{1}{g_d} = \frac{1}{\beta(U_{GS}-U_T)} & (linear\ area) \quad (17) \\ \frac{1}{g_{d(sat)}} = \frac{L^2}{\mu_{ch}C_{dst}(U_{GS}-U_T)} & (saturation\ area) \quad (18) \end{cases}$$

where $\beta = \frac{W\mu_{ch} \cdot C_{ox}}{L}$; C_{dst} is the electrostatic coupling capacitance between the drain and the channel; I_{DS0} is the leakage current between the drain and the source of MOSFET approaching the whole leakage current of IGBT.

7. R_A

R_A consists of the Ohmic contact resistance (R_O) and the PNP transistor's internal resistance. It varies with the device's state.

$$R_A = \begin{cases} \frac{U_{AK}}{I_{AK0}} + R_O & (off-state) \quad (19) \\ R_O & (on-state) \quad (20) \end{cases}$$

I_{AK0} is the leakage current of IGBT.

8. temperature dependences

The on-state resistance R_{on}, the built-in voltage $U_{D_{(i)}}$, the base transverse resistance R_{Pb}, the avalanche breakdown voltage of P-N junction $U_{B(i)}$, the transportation coefficient of the PNP transistor β_{PNP}, the reverse saturation current of P-N junction $I_{S_{(i)}}$, the threshold voltage of MOSFET U_T with relations to the temperature are considered.

$$R_{on}(T) = R_{on}(T_0)(\frac{T}{T_0})^{1.5} \quad (21)$$

$$\begin{cases} U_{D_{(i)}}(T) = U_{D_{(i)}}(T_0) + \frac{dU_{D(i)}(T)}{dT}(T-T_0) \\ \frac{dU_{D(i)}(T)}{dT} = -2\,(mV/K) \end{cases} \quad (22)$$

$$R_{Pb}(T) = R_{Pb}(T_0)[1+\frac{n_i(T_0)}{N_{Pb}(T_0)}]^{-1}(\frac{T}{T_0})^{2.3} \quad (23)$$

$$U_B(T) = \frac{U_B(T_0)}{[1+\frac{n_i(T)}{N_D(T)}]^{0.75}}(\frac{T}{T_0})^{1.125} \quad (24)$$

$$\beta_{PNP}(T) = 1 - \frac{W_B^2}{2D_P(T_0)\tau_P(T_0)}(\frac{T}{T_0})^{-0.8} \quad (25)$$

$$\begin{cases} I_s(T) = I_s(T_0)(1+\frac{T-T_0}{k_0}) \\ k_0 = 0.1 \end{cases} \quad (26)$$

$T_0 = 300K, \quad i=1,2,3$

III. APPLICATION TO LATCH-UP

The current nodal equations corresponding to Fig.2 are built.

$$\begin{cases} -I_A - I_1 - i_{D_1} + i_{C_{j1}} + i_{C_{D_1}} = 0 \\ -i_{D_1} - i_{C_{j2}} - i_{C_{D_2}} + I_1 - I_3 + I_2 - i_{C_{j1}} - i_{C_{D_1}} - i_{D_2} - i_{MOS} - i_{C_{gd}} = 0 \\ i_{D_2} + i_{C_{j2}} + i_{C_{D_2}} - I_2 + I_3 - i_{C_{D_3}} - i_{C_{j3}} + i_{D_3} + i_{R_{Pb}} = 0 \\ i_{RG} - i_{C_{gd}} - i_{C_{gs}} = 0 \end{cases} \quad (27)$$

Equation [27] suitably serves the simulations of the latch-up, of which the overcurrent latch-up is discussed. The overcurrent latch-up usually takes place in two cases----the overdrive by the gate drive circuit, as a consequence of high gate voltage triggered by the high disturbing voltage, and the short circuit of the load.

(1) latch-up caused by gate overdrive

The gate overdrive voltage $U_{GS}^* = U_{GS} + \Delta U_{GS}$. ΔU_{GS} results from the gate return disturbance or Miller effect. The corresponding current deduced from Equation [27] is described by

$$\begin{cases} I_A^* = I_A(1+\frac{\Delta U_{GS}}{U_{GS}-U_T})^2 & (28) \\ I_A = (\beta_{PNP}+1)I_{MOS} & (29) \end{cases}$$

The overdrive latch-up happens on condition that

$$U_{R_{Pb}} = I_A^* \cdot R_{Pb} \geq U_{D_3} \quad (30)$$

R_{Pb} is selected according to Reference [6] for the square-celled IGBT. The $\Delta U_{GS} - U_{R_{Pb}}$ curve, as illustrated in Fig.3, is plotted ($U_{D_3} = 0.8769V$). As can be easily seen, the latch-up begins where the curve crosses over the horizon of U_{D_3} (B_1, B_2, B_3) and within limited scope the higher is the temperature, the less ΔU_{GS} produces the latch-up, which is ascribed to the temperature dependence of R_{Pb}.

(2) latch-up caused by load short circuit

The variation of the load can be expressed by part or full short circuit of the load resistor R_L. At the normal operation state and the load short circuit state, the current is given by

$$I_A = \frac{E_a - U_{on}}{R_L + R_L} \quad (31)$$

$$I_A^* = I_A[1 - \frac{\Delta R_L}{R_L + R_A}]^{-1} \quad (32)$$

where $E_a = V_{CC}$. The prerequisite of the overload latch-up is $U_{R_{Pb}} = I_A * \cdot R_{Pb} = I_A \cdot R_{Pb} \cdot [1 - \frac{\Delta R_L}{R_L + R_A}]^{-1} \geq U_{D_3}$ (33)

The analysis on $\Delta R_L - U_{R_{Pb}}$ relation is described by Fig.3 ($R_{Pb} = 616\Omega$, $R_L = 100\Omega$, $R_A = 1\Omega$, $\Delta R_L = 10 - 90\Omega$). A_1, A_2, A_3, the cross points of $\Delta R_L - U_{R_{Pb}}$ curve and U_{D_3} horizon, are thought of as the start of the latch-up. The arrival of $\Delta R_L / R_L$ at 0.5 leads to the latch-up at 400K and, however, very low or very high temperature improves the value of $\Delta R_L / R_L$ due to that the fluctuations of temperature changes R_{Pb}.

Both cases are carried out to single cell with parameters concluded in Table I.

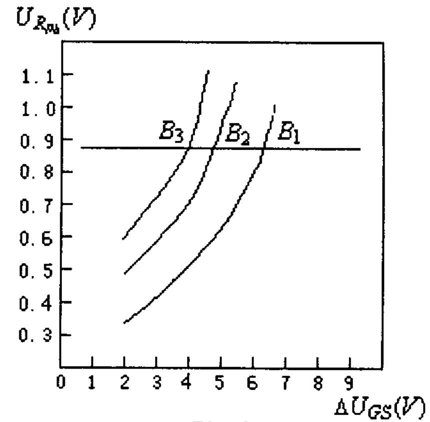

Fig. 3

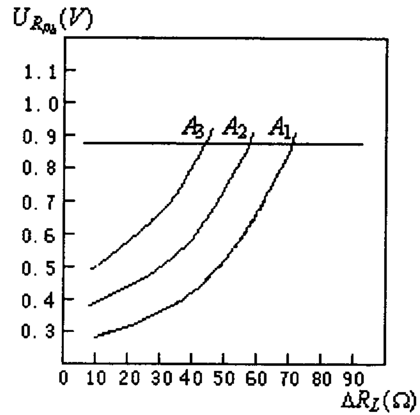

Fig. 4

TABLE I

size of square P⁻-well	12μm
width of N_2 zone	4μm
junction depth of P^- zone in P_2 layer	3μm
block resistance of P^- zone in P_2 layer	2100Ω/□
channel length	2μm
R_{Pb} (T=300K)	340Ω
R_{Pb} (T=400K)	616Ω
I_{MOS}	0.74mA

IV. CONCLUSION

A new mesh-topology model of IGBT based on the physical structure is developed. It is able to simulate the latch-up aroused by overcurrent, overvoltage, fast du/dt, overheat and additionally the on-state performance, the

block characteristics, the switching behavior. Simulations and experimental results confirm the validity of the model.

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