Novel Devices for Sub-100 nm CMOS Technology

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Abstract

Beginning with a brief introduction on near 100 nm or below CMOS devices, this paper addresses novel devices for future sub-100 nm CMOS. First, key issues such as gate materials, gate dielectric, source/drain, and channel in Si bulk CMOS devices are considered. CMOS devices with different channel doping and structure are introduced by explaining a figure of merit. Finally, novel device structures such as SOI, SiGe, and double-gate devices will be discussed for possible candidates for sub-100 nm CMOS.

Introduction

Silicon CMOS has grown tremendously over the past 25 years due to the excellent scaling properties of MOS transistors. The scaling down of MOS devices has been resulting in consistent improvement in density, performance, and power. Now the gate lengths of MOS transistors are near and well below 100 nm in research and development phase. It seems that CMOS technology will be faced with some physical limits in the near future. So it is now needed to review the state-of-the-art of CMOS technology and consider novel devices that may be applied to the scaled sub-100 nm CMOS regime.

In this paper, we will review briefly key device issues such as gate material, gate dielectric, source/drain, and channel. Then schematic MOS structures are examined. Finally, we address novel devices to be applicable in sub-100 nm CMOS technology. They are silicon-on-insulator (SOI), SiGe MOSFET, and double-gate MOSFET.

Key Device Issues

Since state-of-the-art CMOS technology has been the subjects of many recent articles and reviews [1]-[3], the issues related to devices are considered briefly to keep main goal of this paper.

A. Gate Materials

Heavily doped poly-Si has been used as a gate material predominantly, but now suffering from poly-depletion effect (PDE) which degrades g_m and drain current. Poly-Si depletion and loss of drive voltage in poly-Si becomes more severe with oxide thickness scaling. Ultrathin(~2 nm) oxide need a poly-Si doping density above 2×10^{20} cm^{-3} to suppress the poly-depletion. With supply voltage scaling, the loss of gate voltage in the depleted poly-Si becomes a larger percentage of V_{supply}. Recently poly-SiGe has been applied as a gate material. Sheet resistance in boron doped poly-SiGe is smaller than in boron doped poly-Si[4]. Boron ions diffuses in poly-SiGe more slowly than in poly-Si, so the boron penetration through thin gate oxide can be alleviated [6]. Fig. 1 shows dopant concentration and flat band voltage shift (ΔV_{FB}) in both poly-Si and poly-$Si_{0.8}Ge_{0.2}$. Poly-SiGe gate shows less PDE and less boron penetration.

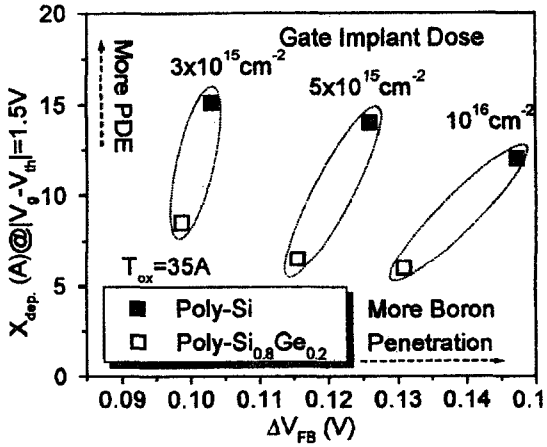

Fig. 1. Poly depletion thickness (X_{dep}) (at $|V_g-V_T|$=1.5 V) versus ΔV_{FB} (with respect to no boron penetration case). Reduced PDE and boron penetration can be obtained simultaneously by using poly-$Si_{0.8}Ge_{0.2}$ gate, as compared to poly-Si gate at the same gate doping level [6].

On the other hand, metal gate provides no PDE and low gate resistance in scaled MOSFETs, but shows less compatibility with conventional CMOS process. However, the metal gate can be achieved in damascene gate FET [8] where gate formation process is different from conventional approach. We can adopt a metal gate with mid-gap work function so that the channel doping level can be lowered while keeping reasonable threshold voltage (V_T).

B. Gate Dielectric

SiO_2 gate oxide scaling is now in the physical limit (1.5 – 2.0 nm), since the tunneling leakage current is becoming too large for oxide thickness below 2.0 nm. According to the SIA roadmap [9], devices with 50 nm L_G and T_{ox} of < 1 nm are anticipated to be produced in 2012. As alternative gate dielectrics, high-K dielectrics can potentially extend scaling

to thinner equivalent oxide thickness. Although nitride in SiO_2 or oxynitride provides compatibility with established technologies, a diffusion barrier for boron, the reduction of tunneling current, and improvement in hot carrier reliability, it still shows limitations in extent of further scaling. Of other key high-K dielectrics proposed, TiO_2/Si_3N_4[10], Ta_2O_5/NH_3-based interface layer[11], HfO_2 (K=~30) [12], and ZrO_2 (K=~25) [13] have good characteristics. Since TiO_2/Si_3N_4, Ta_2O_5/NH_3-based interface layer are unstable on Si, they need special interfacial layer, which may deteriorate scalability and process simplicity. Oxides of Zr and Hf are attracting much attention recently. Especially, Hf can reduce the native SiO_2 to form HfO_2 that is the most stable among high-K materials and becomes a good barrier for impurity diffusion [14]. Fig. 2 shows dielectric leakage current density versus equivalent oxide thickness (EOT). Reliability and insulator/ semiconductor interface properties may remain important concerns for such new materials.

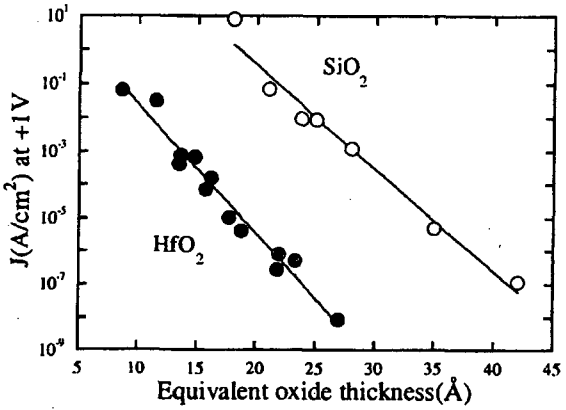

Fig. 2. Leakage current density (@ applied bias of +1 V) versus EOT. At the same EOT, HfO_2 films show lower leakage current than conventional SiO_2 [14].

C. Source/Drain (S/D)

Requirements in S/D region are suppression of short channel effect (SCE), low S/D resistance, low junction leakage current, and small junction capacitance. Especially, as devices are scaled down, the role of S/D extension region becomes more important in obtaining low S/D resistance and in suppressing SCE. By decreasing the junction depth (x_j) of the S/D extension, SCE can be suppressed, but the sheet resistance (Rs) of the extension increases significantly. According to the roadmap, the x_j and the Rs of the S/D extension region are 8-13 nm and 100-400 Ω/sq, respectively, at 50 nm technology node, which is extremely difficult to implement. Also future generations of devices require ever steeper doping profiles of the S/D extension region, let alone the shallow x_j. For example, the sub-50 nm regime will apparently require profiles of order < 5 nm/decade [3]. It seems that new S/D formation method or device structure modification is strongly needed to overcome the challenge.

D. Channel

With device scaling down, doping level of channel region should be increased to keep reasonable V_T and to suppress SCE. However, the surface concentration in the channel region should be kept as low as possible to reduce V_T fluctuation due to random dopant distribution and to alleviate channel mobility degradation due to impurity scattering. The high-V_{DS} I-V of narrow width devices are asymmetric upon reversing the source and the drain terminals, indicating that the placement of dopants near the S/D regions plays a significant role in determining device characteristics. The effects of random dopants become more important as the channel length and width are scaled down [15]. The low surface concentration can be achieved by adopting super steep retrograde doping profile [16]. Halo or pocket is very useful to control the SCE, low junction capacitance, and low junction leakage current, so it is a fashion to adopt halo or pocket implantation in near and below 100 nm CMOS devices. In sub-100 regime, Sb halo is effective for PMOSFET, but In halo is not necessarily effective for NMOSFET due to low activation efficiency (~2×10^{18} cm^{-3}) and transient enhanced diffusion [17].

Device Structure Review and Novel Devices

In this section, several MOSFET structures are considered as competitive candidates for the application of near and sub-100 nm regime. While conventional CMOS is scaling down, alternative technologies cannot compete since every three years sees a two times increase in performance and a four times increase in the number of devices per chip (Moor's law). With the perceived scaling limits of conventional CMOS, advantages inherent in other technologies and design approaches may have great impact, though more expensive. Fig. 3 shows relative device performance versus year for several device structures. From around 2000, conventional bulk CMOS shows saturation in its performance and need

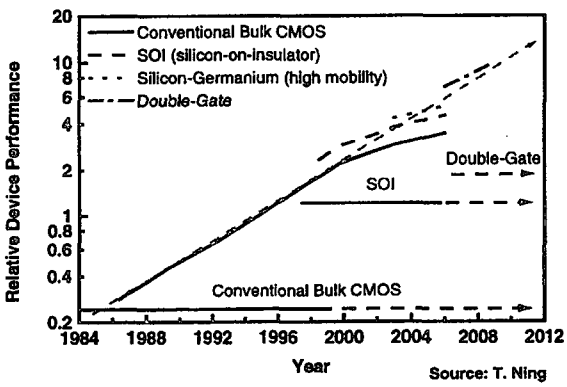

Fig. 3. Relative device performance versus year [18].

structure change to keep the performance.

Fig. 4 shows simple schematic cross-sectional views of several MOSFETs with different doping profiles and structures.

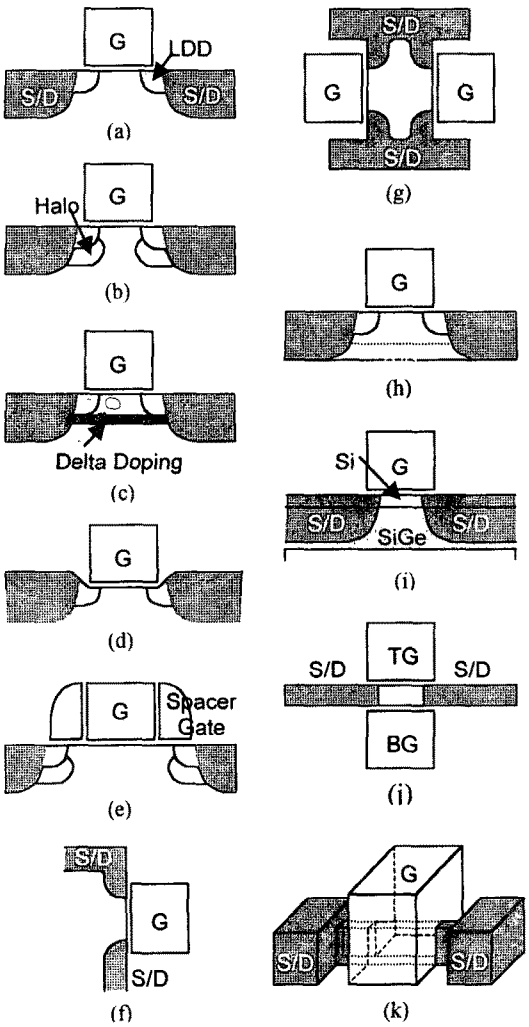

Fig. 4. Simple schematic cross-sectional views of several device structures. (a) Conventional bulk LDD CMOS. (b) Halo (or pocket implanted) CMOS [17]. (c) Delta-doped MOSFET [19]. (d) Recessed channel MOSFET [20]. (e) Spacer-gate MOSFET [21]. (f) Vertical trench MOSFET [23]. (g) Vertical pillar MOSFET [24]. (h) PD [25] (or FD [26] if the body region under dotted line) SOI MOSFET. (i) SiGe channel MOSFET [22], [23]. (j) Standard double-gate MOSFET [27], [28]. (k) Fin-FET (or modified double-gate MOSFET) [29], [30].

Fig. 4 (a) shows a conventional LDD MOSFET that has been adopted as a main technology in the industry. As CMOS devices are scaled down to sub-100 nm regime, halo (or pocket) implantation is necessarily used to suppress SCE as shown in (b). Delta-doped MOSFET was proposed to suppress SCE, has a heavily doped region in the channel as represented by thick solid line in (c). As these devices are scaled down beyond 100 nm, they are have been suffered from SCE. Recessed channel scheme (self-aligned) was proposed to suppress SCE while keeping low S/D extension resistance (due to relatively deep x_j). Fig. 4 (d) shows new planar CMOS device structure which has good device characteristics at about 50 nm regime. This structure has floating spacer gate to induce electrically S/D junction that is very shallow and has low resistance. The floating gate has a different work function from main gate. If the gate material has a mid-gap work function, the surface channel concentration can be lowered while satisfying reasonable V_T and drain induced barrier lowering (DIBL). Fig. (f) and (g) show representative vertical MOSFETs: trench and pillar types. Vertical trench MOSFET is suitable to the high-density (gigabit range) memory technologies. Vertical pillar MOSFET has complex process steps and can be applied high performance logic and memory applications. MOSFET with around 50 nm can be achieved by the vertical pillar structure [24]. Normally vertical devices have channel thickness determined by lithography and etch, and large gate to S/D overlap capacitance. Fig. 4 (h) represents partially depleted (PD) SOI MOSFET if the body region under the dashed line is neutral. Then device design translates well between bulk and PD SOI. The SCE can be controlled by adopting halo as in the case of bulk device shown in (b). PD SOI devices give reduced junction capacitance, but suffer from dynamic floating body effect. In Fig. 4 (h), the body region under the dashed line is fully depleted, we call it FD (fully depleted) SOI where the SCE can be controlled by geometry. V_T is sensitive to Si film thickness and back interface. Subthreshold swing (SS) of FD SOI is steeper than that of PD SOI. Fig. (i) stands for representative SiGe MOSFET which has higher carrier mobility. For example, tensilely-strained Si surface layer grown on relaxed SiGe layer shown in (i) increases both electron and hole mobility. Separate, buried electron (tensile Si) and hole (compressive SiGe) channels greatly increases both electron and hole mobility. Concerns remained are material quality of SiGe epi layer, temperature stability, and compatibility with CMOS. Fig. (j) shows standard double-gate MOSFETs that are considered the most promising devices for CMOS scaling to deep sub-100 nm gate lengths [28],[32],[33]. The double-gate MOSFET should have a uniform and thin (10 – 25 nm) Si channel, low source/drain resistance, and perfectly aligned scalable top and bottom gates [28]. Nearly ideal double-gate MOS structure has been published and shown simulation results and good experimental results of key process steps [29]. Recently, Fin-FET has been published and demonstrated successfully18 nm gate length PMOS [30]. The Fin-FET is a kind of double-gate

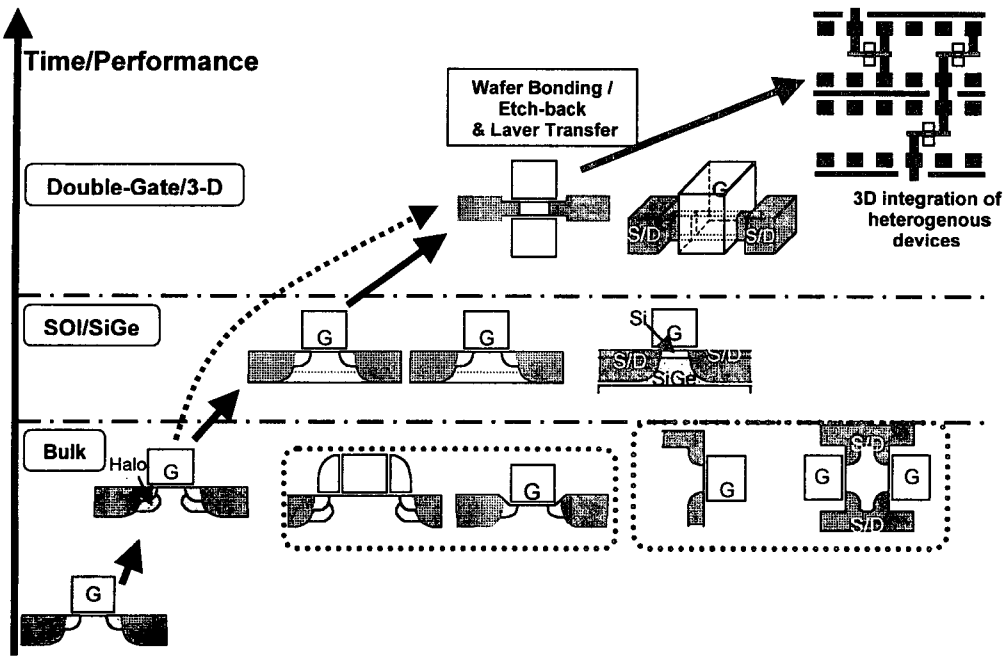

Fig. 5. Device evolution beyond bulk CMOS.

and also looks like a promising candidate for future sub-50 nm CMOS technology. Normally, the process flow to implement the double-gate MOSFET is relatively complex.

Fig. 5 shows the road beyond bulk CMOS. The x-axis represents time and five device groups are discriminated by vertical dash-dot lines. Vertical CMOS is not counted as a group, since vertical device structure looks like a transient or special purpose technology. Final goal of CMOS technology is to implement 3-dimensional integration of heterogeneous devices. It seems that the device technology, starting from bulk CMOS, will pass through the double-gate CMOS and arrive at 3D device integration.

Conclusion

This paper has been reviewed briefly the research trend of gate material, gate dielectrics, source/drain (especially, extended source/drain), and channel as CMOS devices are scaled down into sub-100 nm regime. From the review, it is concluded that future devices require extremely tight process parameters. By considering V_T/V_{supply}, extended source/drain, and channel, novel device structures are strongly needed to overcome problems with the device scaling. So several key device structures published to date are also reviewed. Among them, it seems that double-gate structure is the most promising candidate for the future devices.

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