System Development and IC Implementation of High-performance Image Downscaler using Phase-correction Digital Filters

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위상 교정 디지털 필터를 이용한 고성능/고화질 이미지 축소기 시스템 개발 및 IC 구현

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Abstract

In this paper, we propose an algorithm, an optimized architecture, and an implementation for an improved performance of image downscaler. The proposed downscaler uses two-dimensional digital filters for horizontal and vertical scalings, respectively. It also improves scaling precisions and decreases the loss of data, compared with the 1/32 scaler [1]. In order to achieve the optimization, the digital filters are implemented by the multiplexer -adder type scheme [2]. The scaler is designed by using the Verilog-HDL. It is synthesized into gates by using the Samsung 0.35 um STD90 TLM library.

I. INTRODUCTION

Image scaling is widely used in multimedia video applications, such as PC video, camcorder, and so on [3-4]. A simple pixel drop and an upsampler with decimation have been taken into account for downscaling in general. However, when the scaling ratio is a non-integer the pixel drop method results in the loss of data. The upsampling method that needs the clock much faster than that of input data increases the hardware complexity and is sometimes infeasible due to the requirement of a very high-speed signal processor. [1] showed some improvements by using 2-D digital filters having 1/16-line and 1/32-pixel precisions for vertical and horizontal directions, respectively (called the 1/32 scaler). The 3dB bandwidth (BW) is about 3.6MHz that is relatively narrow to pass most of video signals of upto 6MHz components. Thereby, an improvement is required somehow to enhance the precision of the scaler while preserving a higher BW and a low hardware complexity.

This paper proposes a high performance image downscaler having 1/32-line and 1/64-pixel precisions for vertical and horizontal scalings (called the 1/64 scaler). The theory and algorithm are discussed in Section II. The architecture and the implementation are presented in Section III. The experimental results are described in Section IV and the conclusions are summarized in Section V.

II. THEORY AND ALGORITHM

The proposed 1/64 scaler in this paper uses the concept that valid scaled pixels (or lines) between adjacent pixels (or lines) can be calculated by shifting the group delays of digital filters. Fig. 1 shows the procedure of the scaler using two dimensional phase -correction digital filters. The role of the filters is similar to an all pass filter for gain, while the group delays of digital filters vary

according to the scaled points. This can be achieved by changing filter coefficients based on the scaling ratios. Since video signals are generally band-limited in frequency, a low pass filter which passes the bandlimited signals and shifts group delays to the assumed positions is enough to play the role of the two dimensional phase-correction digital filters [1].

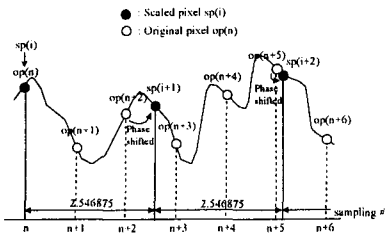
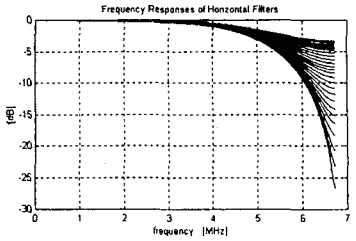


Fig. 1 Proposed high performance downscaler with scaling ratio=1/2.546875

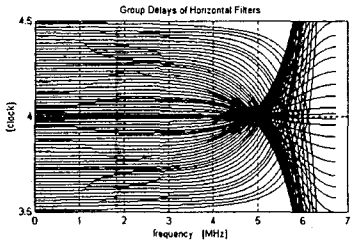
A 3-tap digital filter having 32-poly phases is chosen for the vertical scaler since one can use incoming, one-line delayed, and two-line delayed data through the line memory. The precision of the scaler is a 1/32 line due to the 32 phases in vertical direction.

A 5-tap 64-phase digital filter is used for the horizontal scaler. The operating pixel clock is 13.5MHz in frequency to meet the ITU-R BT. 601 [5].

All the coefficients used the filters can be simply implemented by using shifters and adders since $252 = 2^7+2^6+2^5+2^4+2^3+2^2$. The gain normalization factor of the filter is 1/512. The horizontal filter is cascaded with a compensation filter of a 5-tap FIR to boost high frequency components up. The characteristics of the horizontal filter with the compensation filter are shown in Fig. 2. Fig. 2(a) shows overall frequency responses where the 3dB BW is about 6.0MHz in frequency, which is wide enough to pass most of video signals. Fig. 2(b) shows the group delays calculated by the 64 combinations of the filter coefficients. The delays are located within ±0.5 clock centered at 4 clocks. Thus, the 1/64-pixel horizontal precision is achieved. The 13.5MHz clock is used through entire downscaler. Thereby, the proposed downscaler can be implemented with much less hardware compared with the upsampling.



(a) Frequency responses



(b) Group delays

Fig. 2 Characteristics of the horizontal scaler

III. ARCH. AND IMPLEMENTATION

Fig. 3 shows the block diagram of the downscaler. It consists of the following four blocks: (i) line memory, (ii) vertical scaler, (iii) horizontal scaler, and (iv) FIFO memory.

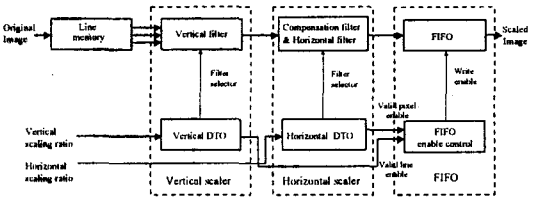


Fig. 3 Block diagram of the proposed downscaler

The line memory contains two horizontal delay memories. The vertical scaler is comprised of a vertical filter and a vertical discrete time oscillator (DTO). The horizontal scaler is composed of a compensation filter, a horizontal filter, and a horizontal DTO. The FIFO stores valid downscaled data only.

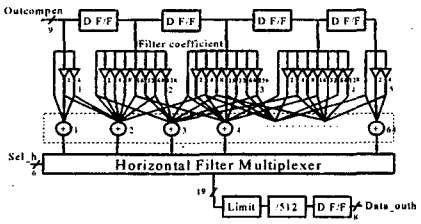
In the line memory, the first memory delays the data for a 1H time that is about 63.5us for NTSC video. The second memory accepts the 1H delayed data and delays the data for additional 1H time. The input, the 1H, and the

2H delayed data will be used in the following vertical scaler.

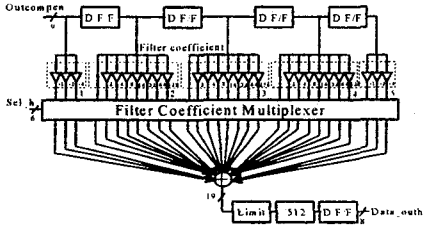
The basic algorithms and architectures for the vertical and horizontal scalers are the same. Thus, the horizontal scaler is described in this paper.

The horizontal DTO is to generate a enable_signal and select_signal for the horizontal filter.

Fig. 4 shows the architecture of the horizontal filter. The Outcompen is the output for the compensation filter. When one designs digital filters, each filter output is first calculated and is then selected based on the scaling ratio through multiplexers (called Arch 1). It is shown in Fig. 4(a). Notice that the Arch 1 uses sixty-four full adders and one 64-to-1 multiplexer. In general, the gate counts of a 1bit full adder is about two times bigger than that of a multiplexer. Thus, an optimized hardware needs to be developed to reduce the number of used full adders. An approach is that the filter coefficients are multiplexed based on the scaling ratios and the outputs are, then, summed to produce the scaled data (called Arch 2). It is shown in Fig. 4(b). Notice that the Arch 2 uses only one full adder and one (5 coefficient sets)-to-1 multiplexer. Thus, one may expect that the Arch 2 will require a much smaller hardware.



(a) Adder-mutiplexer type (Arch 1)



(b) Multiplexer-adder type (Arch 2)

Fig. 4 Architectures of the horizontal filter

The scaler is modeled by using the Verilog-HDL and the models are verified by using the Synopsys simulator. After the verifications are done, the models are synthesized into gates by using the Samsung 0.35 um STD90 TLM library.

Each block of the scaler is synthesized in gates and the results are, then, listed in Table 1. The memories (Sram1, Sram2, and FIFO) are not compared since one uses macro cells generated by the memory compiler in real IC implementation. The first column lists the top modules of the scaler and the second column lists the submodules in the design. The third column represents the gate counts of each submodule by using the Arch 1 and the fourth column represents the gate counts by using the Arch 2.

Table 1 Gate counts of the proposed downscaler

		Sub_module	Arch. 1	Arch. 2
Top-module	Time alignment	-	281	281
	MACRO	Sram1	-	-
		Sram2	-	-
		FIFO	-	-
	Vertical scaler	Sram control	236	236
		Delay	311	311
		Vertical DTO	467	467
		Vertical filter	4,716	1,458
	Horizontal scaler	FIFO control	53	53
		Horizontal filter	625	625
		Horizontal filter	19,386	3,945
		Compensation filter	1,568	1,568
Total gate counts (except macro cell area)			27,643	**8,944**

As one can see, the Arch 2 reduces the gate counts of the horizontal filter from 19,386 to 3,945 that is 79.65% reduction in the hardware complexity. It is caused by the reduction of the number of used full adders from 64 to 1. The total gate count is reduced from 27,643 to 8,944 by using the optimized architecture proposed in this paper that is about 68% reduction.

IV. EXPERIMENTAL RESULTS

In order to verify the performance of the 1/64 scaler, a test image is used: circular zone plate (CZP) having 300×300 pixels with the components of 0Hz to 6.75MHz frequencies. The 13.5MHz clock is used to quantize the

source. Fig. 5 shows the original CZP image having 300×300 pixels. The scaling ratio of 2.546875 is used for vertical and horizontal reductions. The images are now reduced to 118×118 pixels. Fig. 6(a) is obtained by using the 1/32 scaler. Fig. 6(b) is obtained by using the 1/64 scaler. Notice that Fig. 6(b) contains much higher frequency components in horizontal direction compared with Fig. 6(a).

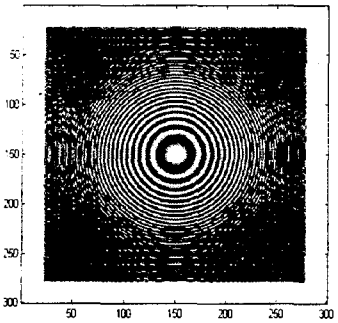
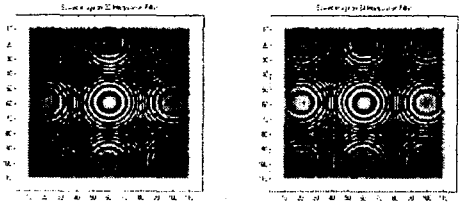


Fig. 5 Original image of CZP (300×300 pixels)



(a) 1/32 scaled image (b) 1/64 scaled image
Fig. 6 Scaled CZP images (118×118 pixels)

Fig. 7 shows the physical layout of the proposed downscaler. The synthesized scaler is placed and routed by the Mentor with the IDEC-C632 0.65um DLM library for further IC implementation. The IC master is fixed in size by 4.500mm×4.500mm. The active layout size of the proposed scaler is 2.528mm×3.237mm.

V. CONCLUSIONS

This paper proposed the improved performance of the downscaler. The proposed scaler provided higher precisions of a 1/32 line and a 1/64 pixel in vertical and horizontal directions, compared with the 1/32 scaler [1]. It also decreased the loss of data since it provided the wider BW of 6MHz. It was also shown that the scaler could simply implemented by using the multiplexer-adder type scheme, which reduced about 68% in the hardware complexity.

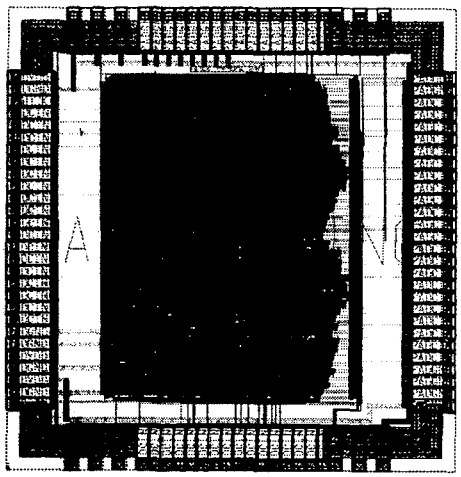


Fig. 7 Scaler64 layout plot

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