Modified CMOS Composite Transistors

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Abstract

In this paper, we propose two new CMOS composite transistors with an improved operating region by reducing a threshold voltage. The proposed composite transistor **1** and **2** employ a P-type folded composite transistor and an electronic zener diode in order to decrease the threshold voltage, respectively. The simulation has been carried out using 0.25㎛ n-well process with 2.5V supply voltage.

I. Introduction

A low voltage low power analog circuit has become a highly important design criteria in the area of analog VLSI circuits. This trend is driven by three main factors simultaneously. First of all, there is a tendency for chip components to be made with smaller dimensions. A component with these smaller dimensions is subject to breakdown at relatively lower voltage[1]. Thus, the supply voltage must be reduced to low voltage. Second, due to the enormous growth in popularity of battery-operated portable equipment such as wireless telecommunication sets, the supply voltage has been gradually reduced to as low as 1.5V to satisfy these needs. Third, a mixed analog-digital signal processing is required to meet high-quality and economic needs[2].

However, with reduction of the supply voltage, analog circuits have poor gain, bandwidth, dynamic range, etc. Many research studies have been performed to solve these problems.

OTA(Operational Transconductance Amplifier), analog multipliers, and analog filters have been widely used in analog signal processing. These circuits often use a composite transistor, which combines one NMOS and one MOS transistor in series[3], as shown in Fig. 1. The equivalent threshold voltage of this transistor is given by

$$V_{Teq} = V_{Tn} + |V_{Tp}| \quad (1)$$

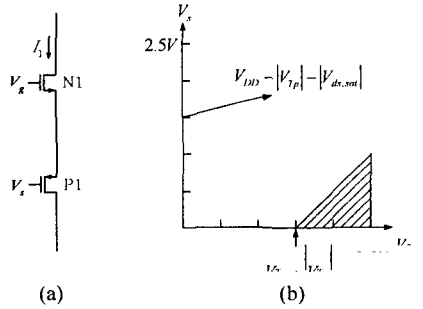
where V_{Tn}, V_{Tp} are the threshold voltages of NMOS and PMOS transistors, respectively. The operating region of the conventional composite transistor is limited because of the large threshold voltage.

To extend the operating region, a LV(Low Voltage) CMOS composite transistor has been developed[4] and is shown in Fig. 2. The equivalent threshold voltage of this transistor is given by

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2(I_B - I_1)}{K_{n2}}} \quad (2)$$

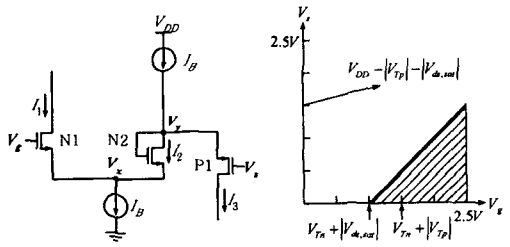
where K_{n2} is the transcondutance parameter of a diode-connected transistor N2.

From Eq.(1) and (2), the LV CMOS composite transistor has the reduced threshold voltage compared to the conventional one. As a result, the operating region of composite transistor is extended as shown in Fig. 2(b), and still this composite transistor has room for improvement. In this paper, the threshold voltage is further reduced by using a P-type fold composite transistor and an electronic zener diode.



(a) (b)

Fig. 1. (a) Conventional composite transistor (b) its operating region



(a) (b)

Fig. 2. (a) Low voltage composite transistor (b) its operating region

In section 2, the proposed composite transistors are presented. The simulation results of the proposed composite transistors are discussed in section 3. Finally, in section 4 concluding remarks are given.

Ⅱ. Proposed Composite Transistors

2.1 Composite transistors with negative threshod voltage

The proposed composite transistor **1** is shown in Fig. 3. A P-type folded composite transistor is added in this composite transistor to the diode-connected transistor N2 of Fig. 2. If all transistors in Fig. 3 are in the saturation region, the gate to source voltage of each transistor can be written by

$$V_g - V_x = \sqrt{\frac{2I_1}{K_{n1}}} + V_{Tn} \tag{3}$$

$$V_y - V_x = \sqrt{\frac{2I_2}{K_{n2}}} + V_{Tn} \tag{4}$$

$$V_z - V_y = \sqrt{\frac{2I_3}{K_{p2}}} + |V_{Tp}| \tag{5}$$

$$V_z - V_s = \sqrt{\frac{2I_4}{K_{p1}}} + |V_{Tp}| \tag{6}$$

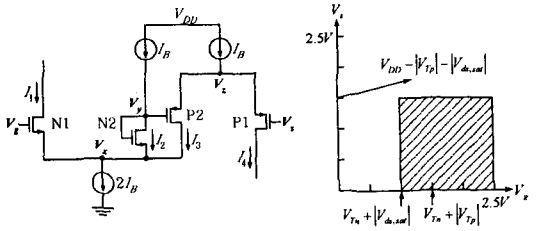
Using the above equations, the V_{gs} becomes

$$V_{gs} = \sqrt{\frac{2I_1}{K_{n1}}} - \sqrt{\frac{2I_2}{K_{n2}}} - \sqrt{\frac{2I_3}{K_{p2}}} + \sqrt{\frac{2I_4}{K_{p1}}} \tag{7}$$

Since $I_B = I_2$, $2I_B = I_1 + I_2 + I_3$, $I_B = I_3 + I_4$, and $I_B = I_1 + I_3 = I_3 + I_4$, I_1 can be written as

$$I_1 = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \tag{8}$$

where the equivalent transcondctance parameter K_{eq} and the threshold voltage V_{Teq} of the proposed composite



(a) (b)

Fig. 3. (a) The proposed composite transistor **1** (b) its operating region

transistor **1** are given by

$$\frac{1}{\sqrt{K_{eq}}} = \frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \tag{9}$$

$$V_{Teq} = -\left(\sqrt{\frac{2I_B}{K_{n2}}} + \sqrt{\frac{2(I_B - I_1)}{K_{p2}}}\right) \tag{10}$$

From Eq.(1), (2), and (10), we can find that the proposed composite transistor **1** has the smallest threshold voltage. The conditions for operation in saturation are $V_g \geq V_{ds,sat,2IB} + V_{Tn}$ and $V_s \leq V_{DD} - V_{ds,sat,IB} - |V_{Tp}|$ where $V_{ds,sat,2IB}$ and $V_{ds,sat,IB}$ denote the drain to source saturation voltage of current sources. The minimum value of V_{gs} is expressed as

$$\begin{aligned} V_{gs,\min} &= V_{g,\min} - V_{s,\max} \\ &= V_{ds,sat,2I_B} + V_{Tn} - V_{DD} + V_{ds,sat,I_B} + |V_{Tp}| \end{aligned} \tag{11}$$

Assuming that $V_{Tn} = |V_{Tp}| = V_T$, $V_{ds,sat,2IB} = V_{ds,sat,IB} = V_{ds,sat}$, then,

$$V_{gs,\min} = 2(V_{ds,sat} + V_T) - V_{DD} \tag{12}$$

In order to obtain the operating region as shown in Fig. 3(b), the minimum V_{gs} of Eq.(12) must be larger than the threshold voltage defined in Eq.(10).

The proposed composite transistor **1** is required to $2I_B$, which causes high power consumption. One way of reducing the power consumption is to use an electronic zener diode instead of a diode-connected transistor N2 of Fig. 2; a circuit with the electronic zner diode is shown in Fig. 4. Similarly, referring to the proposed composite transistor **1**, the drain current I_1 of the proposed composite transistor **2** can be obtained as follows:

$$I_1 = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \tag{13}$$

where K_{eq} and V_{Teq} of the proposed composite transistor

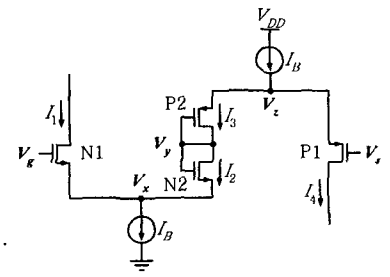


Fig. 4. The proposed composite transistor **2**

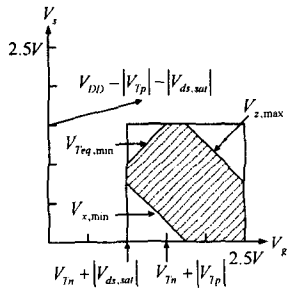


Fig. 5. The limitation of the operating region by current sources.

2, are given by

$$\frac{1}{\sqrt{K_{eq}}}=\frac{1}{\sqrt{K_{n1}}}+\frac{1}{\sqrt{K_{p1}}} \tag{14}$$

$$V_{Teq}=-\left(\sqrt{\frac{2(I_B-I_1)}{K_{n2}}}+\sqrt{\frac{2(I_B-I_1)}{K_{p2}}}\right) \tag{15}$$

Eq.(10) and (15) show that each composite transistor has a different threshold voltage. However, by assuming $I_B \gg I_1$, both equations are equal.

2.2 The limitation of the operating region by current sources.

In practice, the operating region of each proposed composite transistor is limited by current source. The transistors implementing the current source I_B are forced to be in the linear region when the sum of V_g and V_s is relatively high and low.

The drain to source voltages of the current sources(V_x, V_z) in Fig. 4 are given by

$$V_x=\frac{V_g+V_s-\sqrt{2I_1}\left(\frac{1}{\sqrt{K_{n1}}}-\frac{1}{\sqrt{K_{p1}}}\right)}{2} - \frac{\sqrt{2(I_B-I_1)}\left(\frac{1}{\sqrt{K_{n2}}}+\frac{1}{\sqrt{K_{p2}}}\right)+2V_{Tn}}{2} \geq V_{ds,sat,I_B} \tag{16}$$

$$V_z=\frac{V_g+V_s-\sqrt{2I_1}\left(\frac{1}{\sqrt{K_{n1}}}-\frac{1}{\sqrt{K_{p1}}}\right)}{2} + \frac{\sqrt{2(I_B-I_1)}\left(\frac{1}{\sqrt{K_{n2}}}+\frac{1}{\sqrt{K_{p2}}}\right)+2|V_{Tp}|}{2} < V_{DD}-V_{ds,sat,I_B} \tag{17}$$

With $K_{n1}=K_{p1}$ and using Eq.(15), the above equations are simplified as follows:

$$V_x=\frac{V_g+V_s+V_{Teq}-2V_{Tn}}{2} \geq V_{ds,sat,I_B} \tag{18}$$

$$V_z=\frac{V_g+V_s-V_{Teq}+2|V_{Tp}|}{2} \leq V_{DD}-V_{ds,sat,I_B} \tag{19}$$

From the above equations, there are two possible operating regions for V_g+V_s.

$$V_g+V_s \geq 2(V_{ds,sat,I_B}+V_{Tn})-V_{Teq} \tag{20}$$

$$V_g+V_s \leq 2(V_{DD}-V_{ds,sat,I_B}-|V_{Tp}|)+V_{Teq} \tag{21}$$

Assuming that V_{DD}, V_{SS}, V_{Tn}, V_{Tp}, and $V_{ds,sat,IB}$ are constant, $(V_g+V_s)_{min}$ and $(V_g+V_s)_{max}$ are inversely proportional to V_{Teq} due to the negative threshold voltage of Eq.(15). This means that $V_{x,min}$ and $V_{z,max}$ are limited by V_{Teq}. As a result, there is a tradeoff between the minimum saturation voltage of current sources($V_{x,min}$, $V_{z,max}$) and $V_{Teq,min}$, which is shown in Fig. 5.

III. Simulation Results

All composite transistors are simulated by HSPICE using a *0.25㎛ n-well CMOS process with* V_{Tn}=0.556V, V_{Tp}=0.601V, I_B=150㎂, and V_{DD}=2.5V. The transistors N1, P1, N2, and P2 use W/L=1㎛/1㎛, 3㎛/1㎛, 30㎛/0.25㎛, and 90㎛/0.25㎛, respectively.

Fig. 6 shows the simulated DC characteristics of all composite transistors for V_s=0.7V.

Fig. 7(a) and 8(a) show DC characteristics of the proposed composite transistor **1** and **2**. If the minimum saturation voltage of current source is 0.25V, the solid lines represent the operating region shown in Fig. 5.

Fig. 7(b) and 8(b) show AC characteristics of the proposed composite transistor **1** and **2** with *Vs* stepped from 0V to 1.0V, 0.2V steps and V_g=2.0V.

IV. Conclusion

In this paper, we propose two new CMOS composite transistors with an improved operating region by reducing

a threshold voltage. The restriction of the operating region due to current source is described and verified. Simulation results show that the proposed composite transistors have a lower threshold voltage than the conventional composite transistors.

The proposed composite transistors are useful in low voltage analog circuit applications.

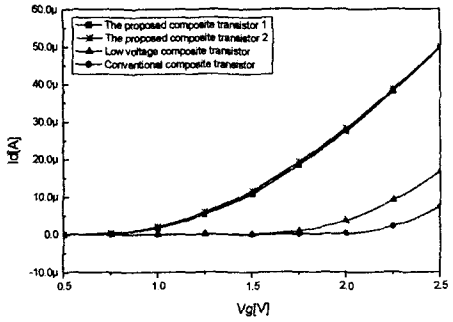
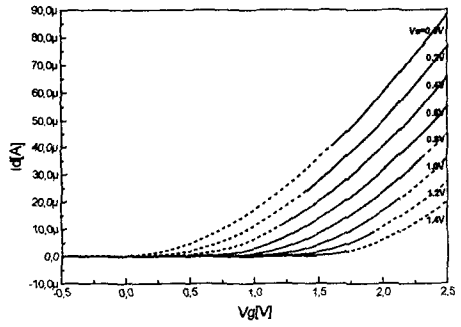
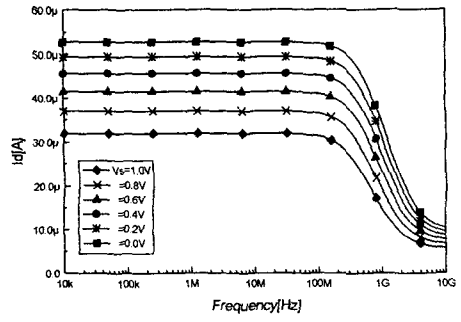


Fig. 6. DC characteristics of composite transistors

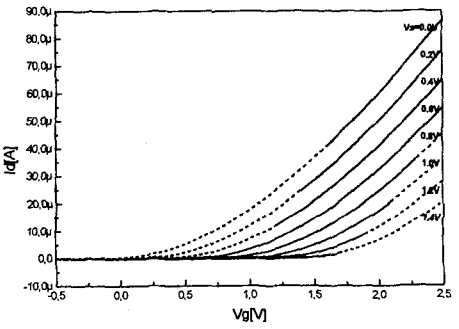


(a)

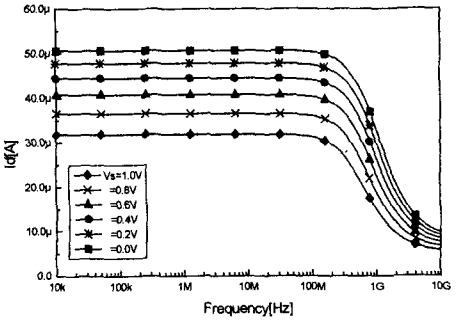


(b)

Fig. 7. (a) DC and (b) AC characteristics of the proposed composite transistor 1



(a)



(b)

Fig. 8. (a) DC and (b) AC characteristics of the proposed composite transistor 2

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