RF circuit simulation for high-power LDMOS modules

Tooru fujioka, Yoshikuni Matsunaga, Masatoshi Morikawa, and Isao Yoshida
Semiconductor & Integrated Circuits Hitachi, Ltd
Kokubunji, Tokyo, 185-8601, Japan
Tel : +81-42-323-1111, Fax : +81-42-327-7652
E-mail:tfujioka@cm.musashi.hitachi.co.jp

Abstract: This paper describes on RF circuit simulation technique, especially on a RF modeling and a model extraction of a LDMOS(Lateral Diffused MOS) that has gate-width (Wg) dependence [1]. Small-signal model parameters of the LDMOSs with various gate-widths extracted from S-parameter data are applied to make the relation between the RF performances and gate-width. It is proved that a source inductance (Ls) was not applicable to scaling rules. These extracted small-signal model parameters are also utilized to remove extrinsic elements in an extraction of a large-signal model (using HP Root MOSFET Model). Therefore, we can omit an additional measurement to extract extrinsic elements. When the large-signal model with Ls having the above gate-width dependence is applied to a high-power LDMOS module, the simulated performances (Output power, etc.) are in a good agreement with experimental results. It is proved that our extracted model and RF circuit simulation have a good accuracy.

1. Introduction

At present, Si power-amplifier modules are used in most of the GSM handset-phones. A conventional method used in the development of these modules is to optimize the module structure by repeatedly producing modules. Recently, the application of a computer-aided design (CAD) has been desired, to the reduction of fast development and development cost. A RF circuit simulation of a high-power LDMOS module used in the CAD requires models of active and passive elements. And precision of the models influences the precision of the RF circuit simulation. It is difficult however, to generate perfect models of active and passive elements, and spending a long time generating perfect models is nor compatible with speedy development. A large-signal model of a LDMOS exerts an especially big influence on the RF circuit simulation of the module design. In generating the large-signal model used in the RF circuit simulation, it is important to generate intrinsic region of the LDMOS precisely. Therefore a method of exact easy removing of extrinsic elements of the LDMOS is required. And a scaling is also important, that is, it is necessary that the performance of LDMOSs with various sizes can be predicted by using the model extracted from a single LDMOS, when the model is applied to a RF circuit simulation. However, the error by scaling of the model was a problem in a conventional RF circuit simulation.
At this time, we extract extrinsic elements by generating small-signal model parameters of LDMOSs with various gate-widths. We pay attention to a consideration of source inductance (Ls) that is one of reasons causing the gate-width dependence of LDMOS and we propose a new scaling technique of LDMOSs in a RF circuiit simulation of the module. As a result, the large-signal model has practical accuracy even in the simulation of the module in a wide bias range.

2. Small-signal model

The generation of a small-signal model is useful for characteristic analysis and for the extraction of extrinsic elements. Each parameter of this model is extracted by using the S-parameter data of the LDMOS that was measured using the TRL (Thru-Reflect-Load) calibration method. The equivalent circuit of this small-signal model is shown in Fig. 1. This model is considered about the pad for a bond-wire and the frequency dependencies of the gate resistance and drain resistance. When we evaluated the small-signal model with the S-parameter set

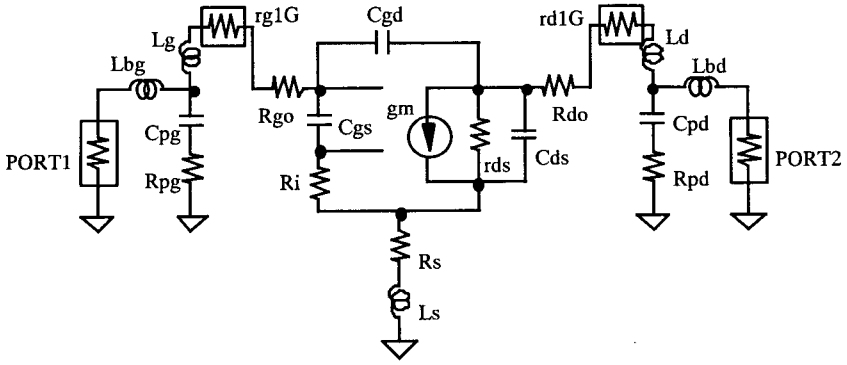

Fig 1. An equivalent circuit of a small-signal model

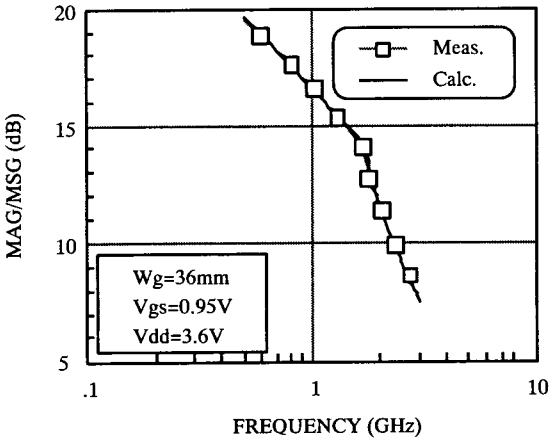

Fig 2. Calculated and measured values of MAG/MSG

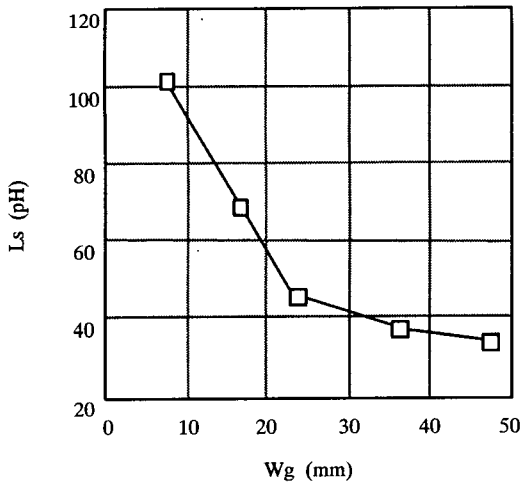

Fig 3. A gate-width(Wg) dependence of Source Inductance (Ls)

at 900 MHz, the error was within 2.9%. The calculated and measured values of MAG/MSG (Maximum Available power Gain/Maximum Stable power Gain) of the LDMOS (Wg= 36 mm) at a drain voltage 3.6 V, and a gate voltage 0.95 V are shown in Fig. 2. Good agreement is shown at frequencies from 0.5 to 3 GHz. The gate-width dependence of the LDMOS shows up when the gate width becomes big. It is not easy to influence this characteristic on the model. Therefore we extracted the small-signal model parameters of LDMOS with different gate-widths, and evaluated the gate-width dependence of each parameter. The gate-width dependence of Source Inductance (Ls) is shown in Fig. 3. The value of Ls is not proportional to gate-width, so it is difficult to use a model when the actual gate width differs from that of the model.

3. Large-signal model

We made a large-signal model of the LDMOS that we used to generate the small-signal model parameters. The large-signal model of the LDMOS that was extracted has a gate width of 4 mm. A source and a bulk of the LDMOS are connected to the GND at the back of wafer. The GND condition of the chip in a high-power LDMOS module differs from that determined in on-wafer measurements. Therefore, the substrate that we used for the measurements were the same mutilayer ceramic used in the actual module. A wide-pitch probe for RF was used in these measurements. We used a HP Root MOSFET Model for a large-signal model. It is important to remove extrinsic elements precisely, to raise the accuracy of the model. In this work we utilized extrinsic parameters of

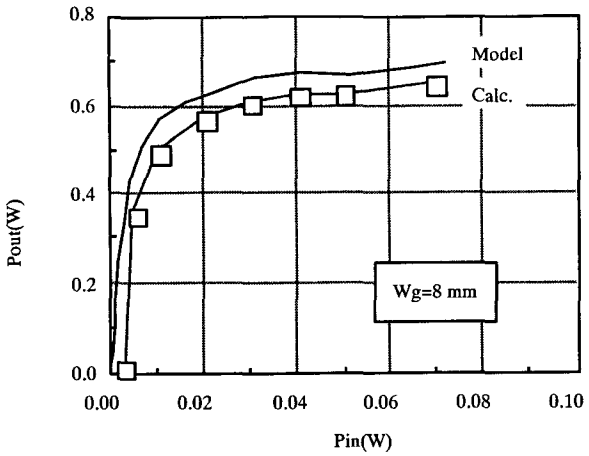

Fig 4. Measured and calculated values of the Pin–Pout characteristics

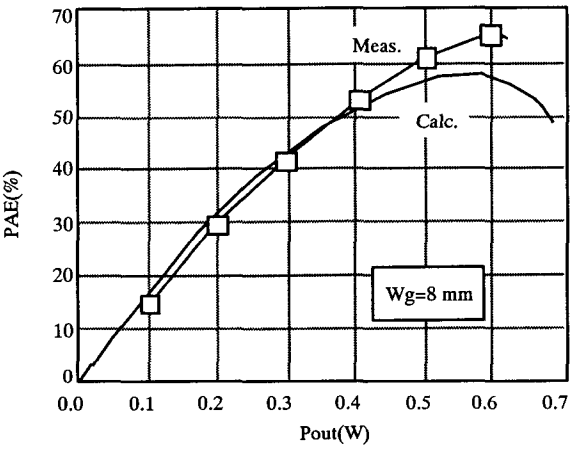

Fig 5. Measured and calculated values of the Pout–PAE characteristics

the small-signal model parameters. The measured and calculated values of the Pin-Pout characteristics (Wg=8 mm) are compared in Fig. 4. The calculated saturation power is 0.03 W higher than the measured value, and this corresponds to a proportional difference of about 4.5%. The measured and calculated values of the Pout-PAE characteristic are compared in Fig. 5. This model is clearly useful in the design and the analysis of the module.

4. Experimental results

The model of the LDMOS (Wg=4 mm) that was extracted was applied to the high-power LDMOS module.

A circuit configuration of the module is shown in Fig. 6. This module is a 3-stage high-power amplifier for a GSM handset-phone. There are in the module terminals for input and output, a drain bias, and an output power control signal. LDMOSs are attached to cavities of the module and the gate and drain are connected to the pads on the surface of a multilayer substrate. The source of the LDMOS is connected to the GND through via holes. The final-stage circuit is a DD-CIMA (Divided-Device and Collectively Impedance-Matched Amplifier) for improving the output power and efficiency [3]. Chip elements are attached to the surface of the substrate and bias lines are arranged in the inner layers so that the module can be made as small as possible. In the RF simulation of the module, we take the gate-width dependence of source inductance (Ls) in the model of the LDMOS and chip elements etc. were generated models to intend to improve the accuracy.

The input power in the simulation was 0 dBm, drain voltage was 3.6 V, and the frequency was 880 MHz. The measured and calculated dependences of the output power of the module on the Vc (Control voltage) are shown in Fig. 7. When the Vc is low, the output power changes a lot when Vc changes a little, and the gain is small. When the Vc is large, it has little effect on the output power. Even in the big change of the gate voltage, the calculation result was practical accuracy. It is proved that the scaling rule of a source inductance(Ls) is important when the actual gate width differs from that of the large-signal model.

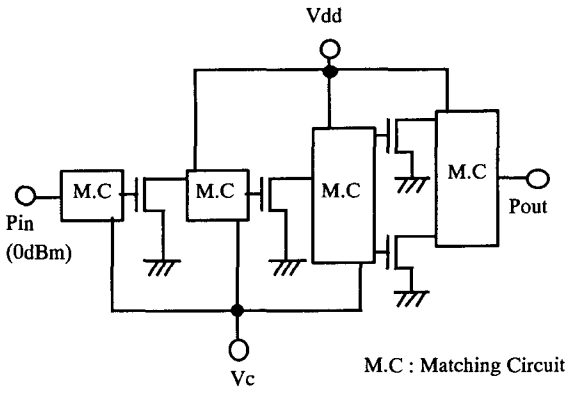

Fig 6. A circuit configuration of the high-power LDMOS module

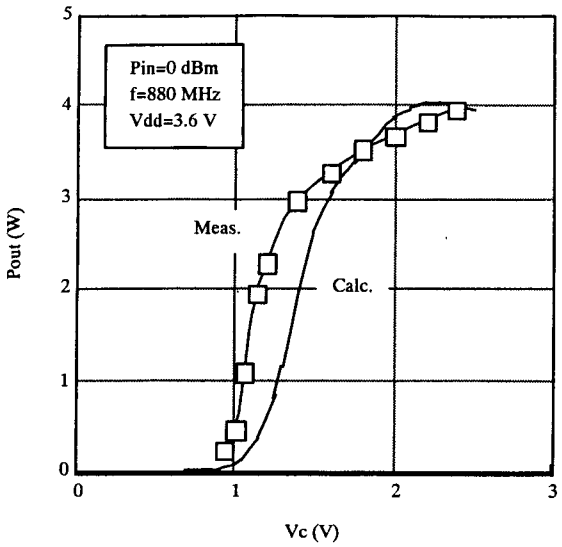

Fig 7. Measured and calculated dependences of the output power(Pout) of the module on the Vc

5. Conclusion

We made small-signal and large-signal models of the LDMOS that is used in the high-power LDMOS module of GSM handset-phones. When we evaluated the small-signal model with the S-parameter set at 900 MHz, the error was within 2.9%. And the small-signal model parameters that were extracted were utilized in making a large-signal model. The large-signal model with Wg=4 mm was generated by using the HP Root MOSFET Model. We compared the calculated and measured values of Pin-Pout characteristics at Wg=8 mm, and we found the calculated saturation power to be 0.03 W higher than the measured value. This is a proportional difference of about 4.5%. The model was applied to he high-power LDMOS module in consideration of the gate-width dependence of the source inductance (Ls). The calculation was practical accuracy, even if gate voltage is changed largely. This means that it is effective to use the model in consideration of the gate-width dependence of a source inductance (Ls).

References

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[3] Yoshida, I., et al., "Si power MOS linear amplifier for PCN mobile telephones," Proc. of 1995 ESSDERC, B1-2, p. 97, Sept., 1995.