An Ultra-Low Power Expandable 4-bit ALU IC using Adiabatic Dynamic CMOS Logic Circuit Technology

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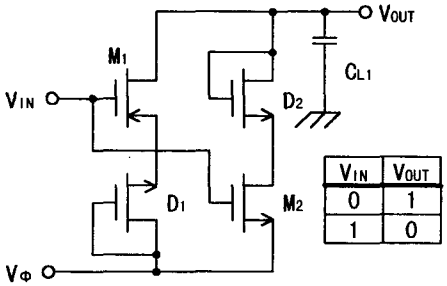
Abstract: This paper describes expandable 4 bit ALU IC using adiabatic and dynamic CMOS circuit technique. It was designed so that the integrated circuit may have the function which is equivalent to HC181 which is CMOS standard logic IC for the comparison, and it was fabricated using a standard 1.2 μ CMOS process. As the result, the IC has shown that it operates perfectly on all function modes. The power dissipation is 2 order lower than that of HC 181.

1. Introduction

With refinement and high integration of large scale integrated circuit, the circuit technique which offers the logic circuit which operates with less power dissipation than that of the conventional CMOS circuit is desired. The adiabatic logic circuit[1] is proposed as one of the circuit techniques which realize it. The principle of basic logic circuit using the technology has features like the following. That is to say, (1) the thermal loss of the energy by the resistance is suppressed by doing charging and discharge of the capacitive load using the power which repeats increase and decrease of the voltage at the fixed gradient, and again, (2) the energy used for the charging is recycled. As a practical adiabatic logic circuit, adiabatic and dynamic CMOS logic (ADCL) circuit with circuit characteristic which contains both advantages of CMOS logic and adiabatic logic (ADL) circuit is reported[2]. In this paper, the effectiveness of ADCL circuit technique is verified by carrying out design, trial manufacture and evaluation using ADCL circuit technique actually, in respect of expandable 4-bit ALU integrated circuit.

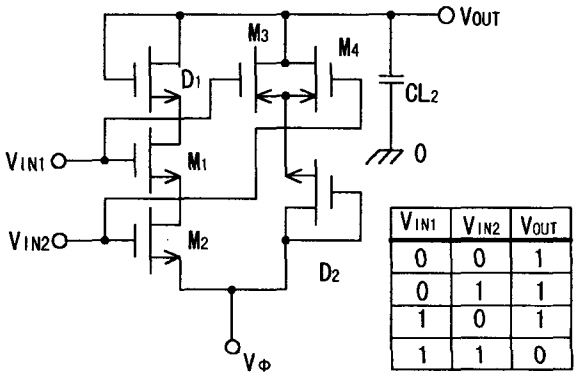
2. Basic logic circuits for the ADCL 4-bit ALU

As basic logic circuit of the ADCL4 bit ALU, NOT(Inverter), 2 input NAND and 2 input NOR circuit are used. Complicated logic gates like exclusive OR, etc. have been constructed using these basic circuits. Basic logic circuits of NOT, 2 input NAND and 2 input NOR are shown in Fig.1 to Fig.3. For the basic logic circuit, the



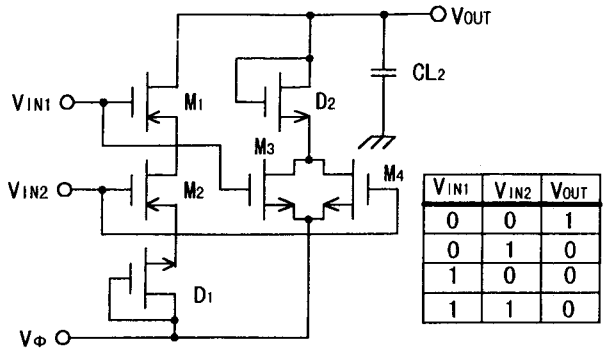
VIN	VOUT
0	1
1	0

Fig.1 ADCL inverter(NOT) circuit.



VIN1	VIN2	VOUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig.2 ADCL 2 input NAND logic circuit.



VIN1	VIN2	VOUT
0	0	1
0	1	0
1	0	0
1	1	0

Fig.3 ADCL 2-input NOR logic circuit.

sine wave voltage V_Φ is used as the supply voltage. In the ADCL circuit, by using the sine wave voltage instead of the DC voltage as energy source, the adiabatic operation can be done. Relationships among Vin, Vout and $V_\Phi$of the ADCL inverter circuit are illustrated in Fig.4.

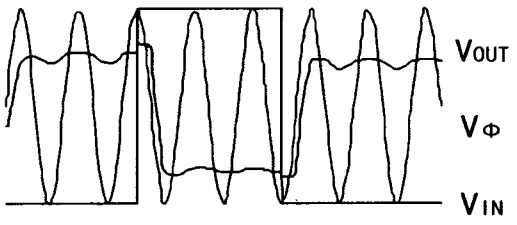


Fig.4 Waveforms of Vin, Vout and $V_\Phi$of the ADCL inverter circuit.

As known from Fig.4, the output voltage of ADCL logic circuit synchronizes with sine wave source voltage. As the result, in basic inverter circuit, the output voltage is delayed from input voltage by 0.5 period of sine wave source voltage. When more complex logic gates are constructed without considering the fact, the case of the malfunction occurs. In this work, in order to avoid such a malfunction, ADCL inverter circuit is used as delay buffer circuit for adjusting the arrival time of signal to the objective logic gate. In case of the ADCL 5-input NAND gate, two cascade connected ADCL inverter circuits are used as buffer circuit for getting one period delay of sine wave supply voltage. The ADCL 5-input NAND gate is shown in Fig.5. In the logic circuit, the signal of V_{IN5} passes two gates of G1 and G3 (or G2 and G3) until the signals of V_{IN1}, V_{IN2},

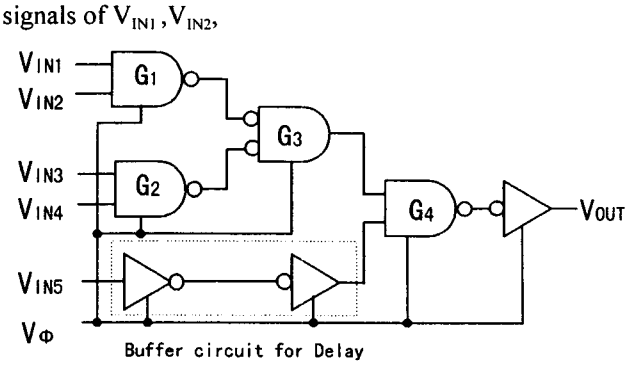


Fig.5 ADCL 5-input NAND logic circuit.

V_{IN3} and V_{IN4} reach the input terminal of G4. In this case, in order to adjust the timing of the arrival of the signal from V_{IN5} to the timing of the arrival of the signal from V_{IN1}, V_{IN2} V_{IN3} and V_{IN4}, the buffer circuit constituted by two ADCL inverter circuits is inserted.

3. ADCL 4-bit ALU Explanation

The ALU using ADCL circuit technique handled here is arithmetic logic unit of the 4 bits. The ALU can execute 16 kinds of logical operation by two Boolean variables and 16 kinds of arithmetic operation according to two 4 bit words.

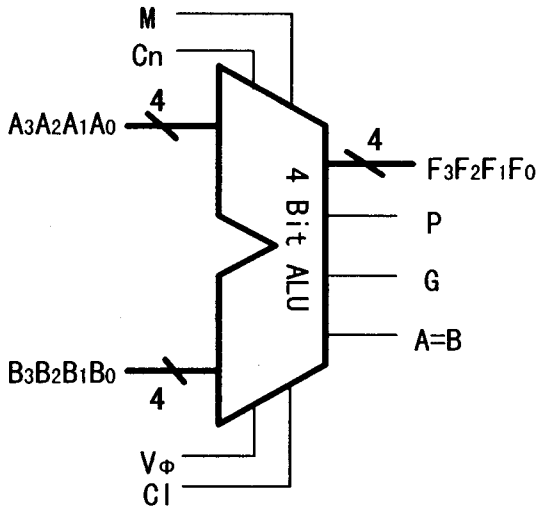


Fig.6 Conceptual illustration of the ADCL expandable 4-bit ALU.

By the voltage level of modal control input M, it is possible to choose which of arithmetic operation or logical operation. The logic function of desire can be chosen in making modal control input M to be high level, if fixed

binary number is input at Select Input $S_3S_2S_1S_0$. On the other hand, the desired arithmetic function can be chosen by inputting the fixed word to Select Input $S_3S_2S_1S_0$ and applying C_n, if modal control input M is low level. In addition, it is possible to manipulate 4 bit word inputs of $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ and arithmetic function output $F_3F_2F_1F_0$, even in which of the 'active high' data and the 'active low' data.

In the method for connecting the adder in the subordination only, the delay time of the carry increases when the bit number increases, because a carry output moves it in order from the lower order digit to the higher during operating. Thus, the high-speed operation can not be done. Then, the speedup was attempted using the Carry-Look-Ahead system for the simultaneous carry generation on the internal 4 bits in the ADCL ALU. Therefore, the output terminals of $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate) have been added to the ALU for the purpose.

The ADCL ALU uses a sine wave supply voltage V_Φ for adiabatic operation. As it has the property that the operation follows the supply voltage, the operation time is dependent on number of steps of ADCL basis circuit connected longitudinally in the inside. This means that the time that 4 bit data $F_3F_2F_1F_0$ is output respectively differs. Thus, it once puts arithmetic function output data $F_3F_2F_1F_0$ in the output resister and then the data are read out simultaneously with data strobing signal C_L.

4. The Adiabatic Expandable 4-bit ALU IC Fabrication

The Adiabatic expandable 4-bit ALU IC was fabricated using a 1.2μ standard CMOS process. The chip size is 2.3mm×2.3mm. For the typical transistor size in the basic inverter circuit, W/L is set as 10μ/1.2μ for both of p channel and n channel transistors. The value of load capacitor for holding the output voltage is 0.25 pF. In the input and output interfaces, the conventional CMOS circuit is used to get the CMOS interface compatibility. The interface circuits are not adiabatic. In Fig.7, the pattern layout of the adiabatic expandable 4-bit ALU IC is shown.

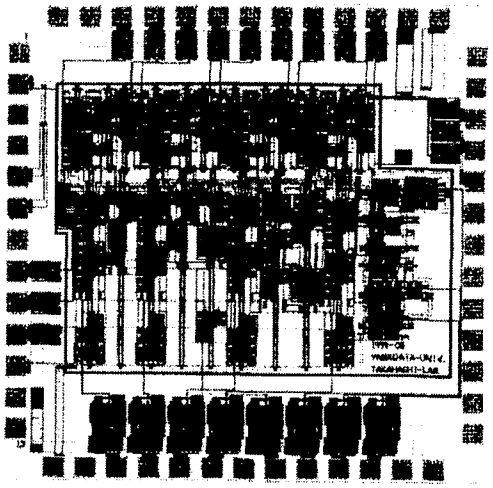


Fig.7 Pattern layout of the adiabatic expandable 4-bit ALU IC.

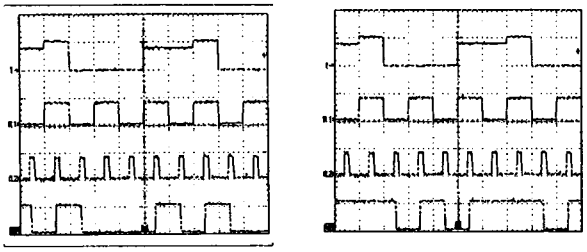
5. Evaluation of the Adiabatic Expandable 4-bit ALU IC

Table 1. Function Table of the 4-bit ALU

Mode Select Input	Active Low Operands & Fn Outputs		Active High Operands & Fn Outputs	
$S_3S_2S_1S_0$	Logic Operation	Arithmetic Operation	Logic Operation	Arithmetic Operation
	(M=H)	(M=L,Cn=L)	(M=H)	(M=L, $\overline{Cn}$ =H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L L H L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L L H H	Logic"1"	minus 1	Logic"0"	minus 1
L H L L	$\overline{A+B}$	A plus ($A+\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	A B plus ($A+\overline{B}$)	$\overline{B}$	(A+B) plus $A\overline{B}$
L H H L	$\overline{A\oplus B}$	A minus B minus 1	$A\oplus B$	A minus B minus 1
L H H H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H L L L	$\overline{AB}$	A plus(A+B)	$\overline{A}+B$	A plusAB
H L L H	$A\oplus B$	A plusB	$\overline{A\oplus B}$	A plusB
H L H L	B	$A\overline{B}$ plus (A+B)	B	($A+\overline{B}$) plus AB
H L H H	A+B	A+B	AB	AB minus 1
H H L L	Logic"0"	A plus A	Logic"1"	A plus A
H H L H	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A+B) plus A

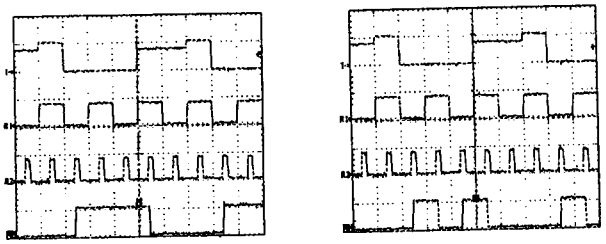
H H H L	AB	$A\bar{B}$ plus A	A+B	A minus 1
H H H H	A	A	A	A minus 1

The function table of the 4-bit ALU is shown in Table 1. Both of the static and dynamic tests were carried out on all of these functions, and the operation is fully confirmed. Several examples out of the dynamic test results are shown in Fig.8 to Fig.11.



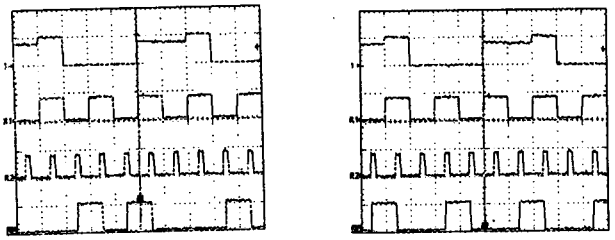
(a) A+B (b) AB

Fig.8 Logic operation in 'Active Low' mode. Waveforms are V_{A0},V_{B0},V_{CL} and V_{F0} from the top to the bottom.



(a) A minus 1 (b) AB minus 1

Fig.9 Arithmetic operation in 'Active Low' mode. Waveforms are V_{A0},V_{B0},V_{CL} and V_{F0} from the top to the bottom.



(a) $\overline{A+B}$ (b) $A \oplus B$

Fig.10 Logic operation in 'Active High' mode. Waveforms are V_{A0},V_{B0},V_{CL} and V_{F0} from the top to the bottom.

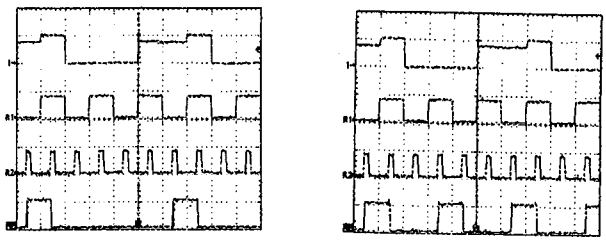
The chip of the ADCL expandable 4-bit ALU IC is confirmed experimentally to operate steadily in all operation modes. On the other hand, the power consumption of the IC is also confirmed to be 1.078 μ W by the simulation. Simulation condition is as follows:

·Operation mode : 'Active Low ' A plus B.

·Frequency of input [F_{B0}]/ power supply[F_{Φ}]: 15kHz / 450kHz.

·Voltage swing and offset: Sinusoidal $5V_{p-p}$ and 2.5 V_{DC}.

For the comparison, HC181 power consumption which is CMOS standard logic IC which connected 47pF capacity to output terminal was measured. The input signal of the equal condition was given, and the power consumption in continuously operating was 62 μ W. It has been proven that the power consumption of the ADCL expandable 4- bit ALU under this condition was much fewer than that of HC181 of CMOS standard logic IC.



(a) A plus AB (b) A plus B

Fig.11 Arithmetic operation in 'Active High mode. Waveforms of V_{A0},V_{B0},V_{CL} and V_{F0} are from the top to the bottom.

References

[1] W.C.Atlas, L.J.Svenson, J.G.Koller,N.Tzartzanis and E.Y.Chou, "Low-power digital systems based on adiabatic-switching principles", IEEE Trans. on VLSI systems, vol.2, no.4, pp.398-407, Dec.1994.

[2] K.Takahashi and M.Mizunuma, "Adiabatic Dynamic CMOS Logic Circuit", Trans. on IEICE, Vol.J81-C II, no.10, pp. 810-817, Oct. 1998.

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