Stress-Bias Effect on Poly-Si TFT's on Glass Substrate

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Abstract: N-channel poly-Si TFT, processed by Solid Phase Crystalline(SPC) on a glass substrate, has been investigated by measuring its electrical properties before and after stressing. It is observed that the threshold voltage shift due to electrical stress varies with various stress conditions. Threshold voltages measured in 1.5um and 3um poly-Si TFT's are 3.3V, 3.7V respectively. With the threshold voltage shift, the degradation of transconductance and subthreshold swing is also observed.

1. Introduction

Polycrystalline Silicon Thin Film Transistors(Poly-Si TFT's) have attracted much attention for high resolution active matrix liquid crystal displays(AMLCD's). Currently, in large size AMLCD's the pixel switching elements are TFT's fabricated in amorphous silicon while the peripheral driving circuitry, for which the very small amorphous silicon TFT mobility is inadequate, is fabricated on single crystal silicon. However, Poly-Si TFT's mobility, while smaller than that of single crystal devices, is fast enough for the peripheral circuit. This fact allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry, onto a single glass substrate. Thus, it substantially reduces manufacturing complexity and cost, and enhances reliability [1]. These poly-Si TFT's must have a high-field effect mobility on the order of 30 $cm^2/V{\cdot}s$ for driver TFT [2] and low leakage current of < 1 pA/μm for pixel TFT [3] for making the realization of large-area and high-resolution display possible. In order to get any further enhancement of the device performance, fabrication should be carried out under a low-temperature process, below 630℃, to prevent the substrates from shrinking. Also, the low process temperatures would reduce display manufacturing costs by allowing the use of inexpensive glass substrate rather than costly quartz substrates. Key requirements of TFT's for AMCLD are a low threshold voltage, a high field effect mobility, a low leakage current that is independent of the gate voltage, and a high ON/OFF state current ratio. In those devices, the characterization, modeling and the performance improvement play an important role.

One issue associated with poly-Si TFT's which has been previously identified is a hot carrier induced instability which occurs at high drain bias and is important in AMLCD applications because driving voltages in the integrated poly-si circuits can be quite large(above 15V). Hot carrier instability is also well known in single crystalline Si metal-oxide-semiconductor-field-effect-transistors (MOSFET's) and occurs when the drain field is high enough to cause significant carrier injection into the gate dielectric.

In this work, the n-channel poly-Si TFT's formed by SPC process on glass using low temperature (below 600℃) process were investigated. Before and after stressing, the electrical properties such as I-V characteristics, threshold voltage, transconductance, and subthreshold swing were characterized. It is done to check the possiblity of large-size and high density TFT-LCD with poly-Si TFT's.

2. Experiment

The process sequence of the top gate Poly-Si TFT's is shown in Fig 1. A silicon dioxide (SiO_2) underlayer was deposited by atmospheric pressure chemical vapor deposition (APCVD) on the glass. Silicon film was deposited in the amorphous phase by thermal decomposition of disilane (Si_2H_6) with a deposition rate of 2.2 nm/min at 470℃ in a conventional low pressure chemical vapor deposition (LPCVD) reactor. The reactant source gas was a mixture of 5% disilane in helium. Those films were crystallized by a low-temperature thermal annealing at 600℃ for 10h in N_2 atmosphere. It had resulted in polysilicon films with the average grain size of 1μm. After annealing, those films were fully crystallized along the film thickness as confirmed by TEM observations. The gate dielectric was a SiO_2 (100nm) grown by LPCVD at 550℃. A gate polysilicon film was deposited by LPCVD immediately after the oxidation. The gate electrodes were patterned with a subsequent photolithographic process

followed by dry etching. Phosphorous (Boron for p-ch. devices) ions were implanted to form source, drain, and gate doped regions with a dose of > 10^{15} cm^{-2} at an energy of 85 KeV (35 KeV for p-ch. devices). An implant activation annealing process was then performed at 600℃ for 6 h in nitrogen atmosphere. No dopant was introduced into the channel polysilicon layer. A100-nm-thick passivation was then deposited by PECVD, followed by opening of contact windows, deposition and patterning of the aluminum electrodes. Aluminum was used as the gate, drain and source electrodes. These devices were processed at process temperatures not exceeding 600℃. The channel lengths of the fabricated devices were 1.5, 2, 6, 10 μm and the width is fixed at 5 μm. Post metallization anneal was done at 400℃ for 30min in a forming gas atmosphere (20% H_2 and 80% N_2). Finally, hydrogen plasma passivation of the polysilicon grain boundaries was performed at 350℃ for 30min.

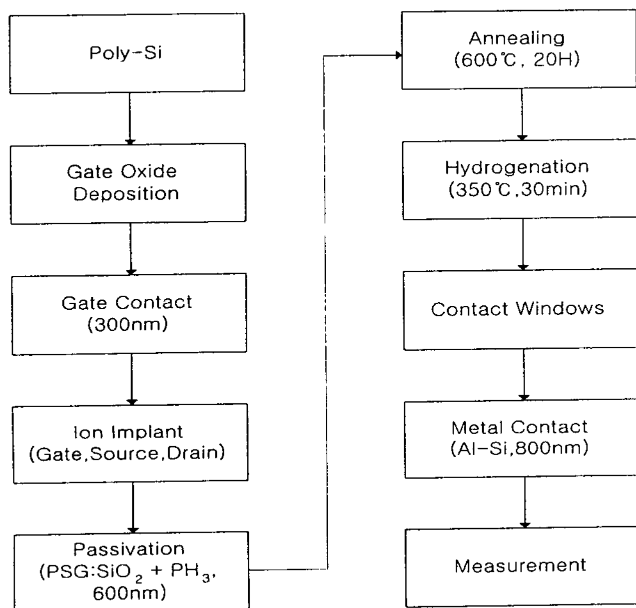
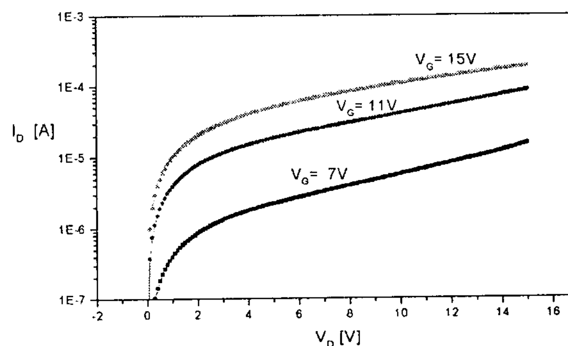


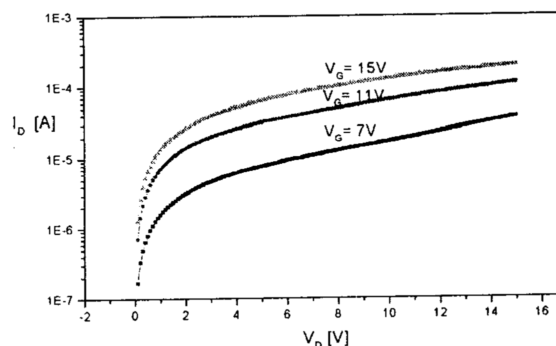
Fig 1. Poly-Si TFT's Process Sequence

2. Measuremints and Discussion

1.5um and 3.0um Poly-Si TFT's show output characteristics in Fig 2. The slope of I_D before saturation is linear. It is indicated that ther source and drain contacts are ohmic due to the low-resistivity n+ poly-si but drain current(I_D) at ON-state increases due to the increasing of the drain field with decreasing channel length. Also, I_D currents are not saturated. The output characteristics exhibit in fact an anomalous current increase in the saturation regime, often called "kink"effect due to an analogy with silicon-on-insulator(SOI) devices. The following results clearly show that the primary cause for the "kink" effect in Poly-Si TFT's is impact ionization. Indeed, when Poly-Si TFT's are biased in the saturation region at large drain voltages, the electric field encroached the drain end is rather large and generation of electron-hole pairs by impact ionization occurs. The increase of current in the $I_{DS}(V_{DS})$ at large V_{DS}(shown e.g., in Figs 2) arises from generated pairs which survive the recombination process occurring in the high field region and are separated by the electric field in the drain depletion region. Electrons are readily collected at the drain electrode while holes move to the opposite direction and are pushed by the gate induced potential toward the back of the channel. As holes flow toward the source, they experience a recombination process via the energetically distributed gap-states. It can be easily anticipated that the higher the recombination rate, the lower the hole concentration at the source. It is also clear that the excess current does depend on generation and also recombination[5].

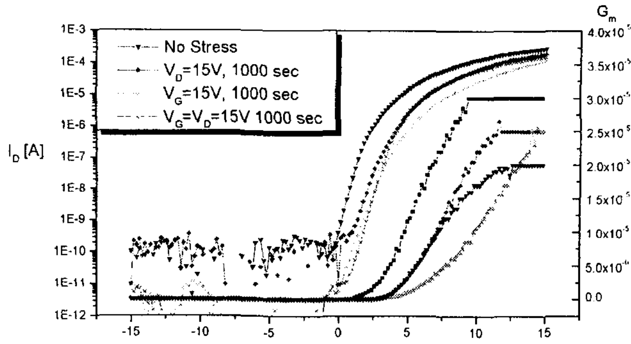


(a) Output characteristic of 1.5um n-channel Poly-Si TFT's with different gate voltages

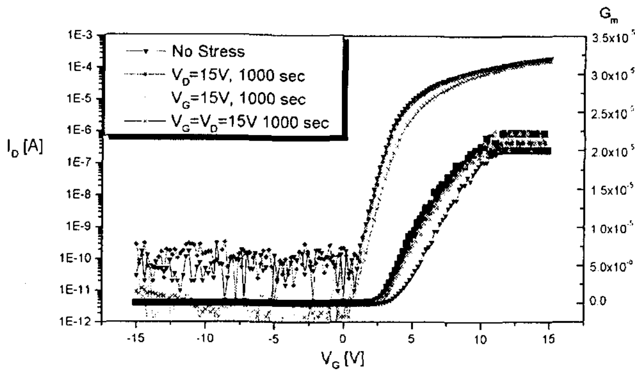


(b) Output characteristics of 3.0um n-channel Poly-Si TFT's with different gate voltages

Fig. 2 Output characteristics of Poly-Si TFT



(a) Transfer characteristics and transconductance of 1.5um n-channel Poly-Si TFT's



(b) Transfer characteristics and transconductance of 3.0um n- channel Poly-Si TFT's

Fig. 3 Transfer characteristics and transconductance of n-channel Poly-Si TFT's

Figure 3 shows the effects of a 1000sec long, high drain and gate bias stress on the transfer characteristics of SPC n-channel Poly-Si TFT's. The n-channel TFT's were stressed at a drain bias value of Vd=15V, a gate bias value of V_g=15V, and both drain and gate bias values of Vd=Vg=15V. The degradation of device characteristics, such as the increase of threshold voltage, the decrease of on current are appeared in both 1.5um and 3.0um n-channel Poly-Si TFT's. It has been reported that the degradation may be occurred either by the creation of metastable states in the drain depletion region probably due to the existence of weak Si-H bonds or by the hot-carrier trapping in the gate insulator near the drain junction in Poly-Si TFT's.

These figures of results show that the leakage current in both 1.5um and 3.0um n-channel Poly-Si TFT's is drastically decreased by the electrical stress. The decrease of leakage current by the electrical stress was more effective to 1.5um than to 3.0um n-channel TFT. Leakage current reductions of TFT's fabricated by SPC process after an electrical stress were reported by other papers. They also reported that on current and Vth are varied by the electrical stress. In order to investigate which stress is more effective, stress conditions were varied. V_g=15V reduced the leakage current without any drain to active stress(V_d=0). The leakage current behavior before and after the electrical stress at V_d=15 and V_g=15 for 1000s is shown Fig 3. These figures suggest that the carriers generated at gate oxide reduce the leakage current and most of carrier trapping occurred at near the gate oxide biased region.[6]

Table1. Summary of threshold voltage and subthreshold swing

Stress [1000s]	Threshold Voltage		Threshold Voltage Shift	
	1.5um	3.0um	1.5um	3.0um
No Stress	3.3V	3.7V	N/A	N/A
V_d=15V	5.2V	3.9V	1.8	0.2
V_g=15V	7.0V	3.9V	3.7	0.2
V_d= V_g=15V	5.1V	3.8V	1.8	0.1
Stress [1000s]	Subthreshold Swing S [mV/decade]		Subthreshold Swing Shift	
	1.5um	3.0um	1.5um	3.0um
No Stress	2.0	1.4	N/A	N/A
V_d=15V	2.0	1.4	0	0
V_g=15V	3.59	1.61	1.59	0.17
V_d= V_g=15V	2.0	1.4	0	0

The threshold voltage, V_{th}, was defined as V_g which gives 1% of the maximum I_d current measured at V_{ds} = +15V for n-channel Poly-Si TFT's. The subthreshold swing, S, was obtained as the reciprocal slope of the linear region in the semi-log transfer characteristics before the transistor is turned on. Table 1. shows the threshold voltage and subthreshold swing of Poly-Si TFT's with electrical stress. The threshold voltage shift of 1.5um n-channel TFT's is much worse than that of 3.0um n-channel TFT's. Especially, 1.5um n-channel TFT's is the worst threshold voltage shift when V_g=15V stressed The sign of $\triangle V_{th}$ may be explained predominantly by the mobile ions effect. Water related species may not be involved here because of the high temperature used during the densification of the oxide. Sodium ions may mobile, however, in present APCVD oxide particularly because it was not phosphorus doped. Phosphorus doped oxide is known to reduce the mobility of sodium ions. Degradation of the subthreshold slope S must then be explained from another effect. An increase of S may be explained by a state creation at the insulator-

channel interface and/or in the channel material. States creation is usually used to explain the degradation of hydrogenated amorphous and hydrogenated polycrystalline silicon TFT's. According to the model currently used, the weak Si-Si bonds, present in amorphous silicon or in strained and disordered regions of Poly-Si, are likely to break under electron or hole accumulation. This breaking induces pairs of dangling bond defects. To prevent reforming of the weak bonds, the model needs to stabilize the dangling bonds by a diffusive motion of hydrogen. This model may be involved to explain the increase of S in hydrogenated TFT's, more important when the stress bias is positive i.e. under electron accumulation. It is due to creation of states in the upper part of the band-gap in the case of n-channel Poly-Si TFT's.[8]

4. Conclusion

In summary, electrical properties of Poly-Si TFT's optimized through solid phase crystalline on glass substrate has been investigated. Kink effect is originated by impact ionization at the drain end of channel, where the electric field is larger. Electrical characteristic degradation of Poly-Si TFT's induced by prolonged bias-stress applied in the Kink regime, has been related to the generation of interface states near the drain.

From the results presented here, it appears clear that driving schemes of analog and digital circuits based on Poly-Si TFT's should avoid operating the devices in the kink regime, because sensitive hot-carrier induced degradation could occur. In order to reduce this problem, drain field engineering is mandatory and several options, including lightly doped drain and drain-offset, should be followed.

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