DESIGN AND IMPLEMENTATION OF THE ALL DIGITAL QPSK TRANSMITTER FOR MPEG-2 PACKETS SUPPORTING THE DAVIC STANDARD

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ABSTRACT:

In this paper, a next generation high speed QPSK transmitter is designed based on 0.8μm design rule. The designed transmitter supports the MPEG2-TS coded packet data for the DAVIC standard. Transmitter is composed of the convolutional coder, the shortened Reed-Solomon coder, and the QPSK modulator. The coded packets are modulated in QPSK with an RC filter. Especially, Galois Field multiplier with a standard basis is designed with the pipelined parallel architecture. Also, in the QPSK modulator, the RC filter and mixer are simplified into the ROM table, which can improve the performance of the transmitter. The total number of gates for the implemented baseband transmitter is 26,875.

1. INTRODUCTION

Nowadays, all digital high speed multi-media digital communication systems are concentrating in the wireless field. They have been digitizing records of every information to offer various multi-media services which are composed of voices, letters, and images. To meet these requirement, development of high speed communication systems and efficient algorithms of the complex signal process are necessary. The rapid and continuous growth of digital VLSI circuit techniques help the production ability of system-on-chip and reduce the production cost. High speed communication systems in a wireless channel require a power limited modulating method and an encoding method in order to correct the several errors occurring in the transmission channel. The QPSK modulation, one of the most popular schemes in the present, is robust for not only phase noises strongly but also distortions and interferences of the multiple pathway. These characteristics are very important regarding the communication system of limited power like a LMDS (Local Multipoint Distribution Service). The QPSK method, for several years, has been successfully accepted to the service of a digital satellite television DTH (Direct-to-home) and DAVIC (Digital Audio-Visual Council).

The main function of the designed chip which has the error correcting coder(i.e. shortened RS coder and Convolutional coder) and QPSK modulator is to guarantee a high quality broadcasting through a wide-band multi-channel. The architecture for the GF multiplier in a shortened RS coder should be essentially considered. Because it determins the entire system processing time. Regarding the implementation of finite field multipliers, since Bartee and Schneider presented the "Computation with Finite Fields" in 1963[1], several approaches have been discussed and developed. The standard basis multiplier, among them, is used in our design, for being have features of regularity, modularity, and simplicity. It does not need the basis conversion used in the dual basis and normal basis multiplier[2]. In the designed QPSK modulating module, the designed filter has a structure for selecting four samples from the modulated signals, thus operates at a high speed. To do this, in this modulating module, the multipliers needed to achieve a filter function are replaced by ROM table stored the information of four samples.

The organization of this paper is as follows. In Section II, we present the structure and function of the implemented transmitter. We then present the designing, implementing procedure and show the simulation result in Section III, and conclude in Section IV.

2. DESIGN FOR HIGH SPEED QPSK TRANSMITTER SYSTEM

2.1. Transmitter Architecture

Fig. 1 shows the functional blocks of implemented transmitter. The transmitter inputs are the MPEG-2 parallel data 8bits and two clocks with a fractional rate. The outputs are the four parallel data 10bits and the control signals to access the external memory. Also there is an output to test the

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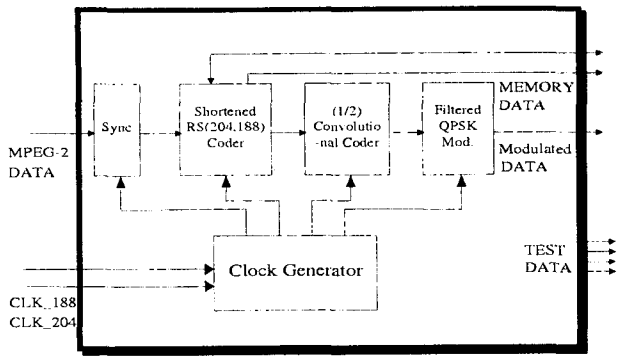

Figure 1: Functional Block Diagram for Transmitter System

correct operation of each modules. The implemented transmitter consists of five modules, i.e., the clock generator, the synchronizer, the shortened RS(204,188) coder, the convolutional coder with an 1/2 code rate, and the QPSK modulator including the square-root raised cosine filter with a roll-off factor, r=0.35. This transmission method is useful, in a band-limited wireless environment, to have strongly robust channel coding as a concatenated code based on a convolutional code and a shortened RS code.

The framing structure is in accordance with MPEG-2 transport stream which is composed of 188 bytes(= 187 data byte + 1 synch. byte($47hex$)) packets. The 187 bytes data stream is randomized except the 1 synch. byte for spectrum shaping purposes. The energy dispersal randomized input data with 188 bytes follows the shortened RS coder. The error protected packets are generated by performing systematic shortened RS(204,188) encoding with t=8. This means that 8 erroneous bytes per packet can be corrected. This coding process adds 16 parity bytes to the input packet, 188 data bytes systematically.

2.2. Synchronizer and Clock generator modules

This module inverts the 1 byte according to the MPEG-2 frame. The non-inverted 187 bytes are transmitted by randomizing. This process starts by initiating the polynomial for the pseudo random binary sequence(PRBS) generator resister to "100101010000000" at the start of every eight transport packets. The generation polynomial is "$1+x^{14}+x^{15}$". To provide an initialization signal for the derandomizer, the MPEG-2 sync byte of the first transport packet in a group of eight packets should be inverted bitwise from $47hex$ to $B8hex$.

The clock generator have two modules, i.e., one is the external fractional rate generator to generate two clocks: a 188/204 clock and a 204 clock and the other is the inner clock generator which has four-type clocks used in modules. The external fractional rate clock generator is easily made a synchronous 6 bits counter and some combinational logic.

2.3. Error Correcting Coder modules

2.3.1. Standard Basis Galois Field Multiplier

In most error correcting coder, the Galois Field operations such as addition and multiplication are necessary. Among them, the GF multiplier is a critical element determining the performance of the designed non-binary shortened RS coder and entire transmitter. For a designed application, we already know the primitive coefficient values of the primitive polynomial and then complexity for the GF(2^m) multiplier can be reduced much more as compared to one of the generalized multiplier by removing some related gates of this known coefficient values.

Let $f(x)$ be the primitive irreducible polynomial of degree m for GF(2^m) and α be a root of $f(x)$. Let multiplicand be $A = \sum_{n=0}^{m-1} a_n\alpha^n$, and multiplier be $B = \sum_{n=0}^{m-1} b_n\alpha^n$. The product of A and B in a finite field GF(2^m) is

$$\begin{aligned} p &= AB = \textstyle\sum_{n=0}^{m-1}(A\alpha^n)b_n \\ &= \textstyle\sum_{n=0}^{m-1} p_n\alpha^n \end{aligned} \quad (1)$$

where $p_n = Ab_n$ is a standard basis coordinate.

In above equation, the operation of multiplication by α, $A\alpha^n$ can be rewritten by a $A\alpha^n = a_0^k\alpha^0 + a_1^k\alpha^1 + ... + a_{m-1}^k\alpha^{m-1} = \sum_{n=0}^{m-1} a_n^k\alpha^n$, where a_n^k is a partial element coefficients of A corresponding to the element of standard basis α^n for a given range, $0 \le k \le m-1$. Then the initial value is $A\alpha^0 = A$, for $n = 0$ and the coefficient is $a_n^0 = a_n$, for $0 \le n \le m-1$, $a_n^0 = 0$ for $n = 0$, and a_n^k can be found as follows[3].

$$\begin{aligned} a_0^k &= a_{m-1}^{k-1} f_0, & 1 \le k \le m-1 \\ a_n^k &= a_{n-1}^{k-1} + a_{m-1}^{k-1} f_n, & 1 \le k \le m-1. \end{aligned} \quad (2)$$

If we apply the known coefficient values, f_i, the basic multiplier cell can be constructed from the Eq.7 and the basic cell blocks $M_{i,j}$ at position (i,j) are shown in Fig. 2. Input variables of the multiplier are the following five parameters: the coefficient a_i^{j-1} of a_i in $A\alpha^{j-1}$, the primitive polynomial coefficient f_i of α^i, partial product ($p_i^{j-1} = a_i^{j-2}b_i$), the coefficient $A_j(= a_0^j)$ of α^{m-1} in $A\alpha^j$, and the coefficient $B_j(= b_j)$ of α^j in a multiplier B. The basic cell block $M_{i,j}$ computes a_i^j and p_i^j in each step. A parallel multiplier obtained is finally composed of the m^2 basic cells as shown in Fig. 3. For a bit-level pipelined parallel architecture with three latches, the critical path delay, i.e., the delay for a calculation of the total multiplication, is the delay through 1 two-input XOR gate and 1 two-input AND gate. It is identical to the delay of each basic cell in calculating the partial multiplication.

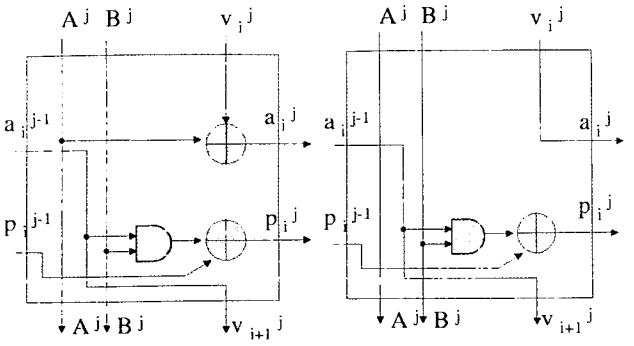

Figure 2: Basic Cell for a Standard Basis GF Multiplier

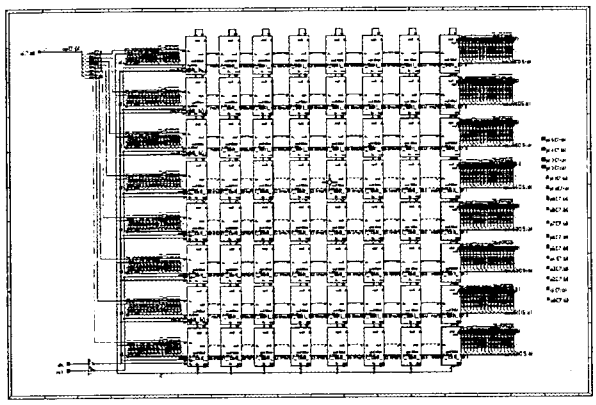

Figure 3: Schematic for a Standard Basis GF(2^8) Multiplier

2.3.2. *Shortened RS coder and Convolutional Coder*

The functional block diagram for the shortened RS coder is showed in Fig.4. This process adds 16 parity bytes to the MPEG-2 transmission packet to give a code word (204, 188). The shortened RS(204,188) encoder is implemented by adding the all zeros with 51 bytes to the data information with 188 bytes before the information bytes at the input of a RS(255,239) encoder and after the coding procedure 51 bytes are discarded from the coded word. This can be applied either inverted(i.e., $B8hex$) or non-inverted(i.e. $47hex$) and erroneous eight bytes per packet can be corrected. In our design, we generate and extend the field from the following generation polynomial or primitive polynomial,

$$f(x) = x^8 + x^4 + x^3 + x^2 + 1. \tag{3}$$

The elements in a generated field is used as code symbols which are satisfied for following code generation polynomial,

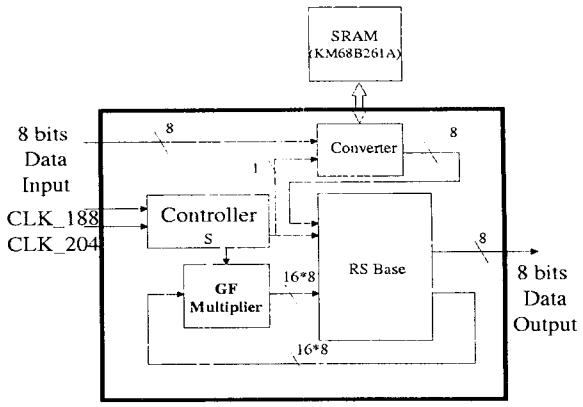

Figure 4: Block Diagram for Shortened RS(204,188)Coder

$$g(x) = \prod_{i=0}^{15}(x + \mu^i) \tag{4}$$

where, $\mu = 02hex$. Fig. 4 shows that the functional block composed of controller, the standard basis GF multiplier, and the RS base blocks implemented by using Eq.4 and 5. The elements over the finite GF(2^8) are obtained from Eq.4 which are easily designed by a sequential shift memory with a feedback loop in the RS base block and the codeword symbols is generated by the GF multipliers in Eq.5. The operation of RS coder is achieved by the controller signal S. The stages of the memory are first initialized by being filled with zeros. During the transmission of input packet 188 bytes, the parity code is stored in this sequential shift memory. After transmission of the 188th message byte, the stored the 16 bytes of the encoding memory is cleared by moving the parity bytes to the output memory. To support the real-time operation, it is designed that the input data, 188 bytes per packet, is read or written alternatively at two external SRAM. The external SRAM used is a high speed BiCMOS Static RAM($KM68B261A$). Fig. 5 shows the (133,171) 1/2 convolutional code block with constraint length K=7 and it is designed 8 bits parallel structure.

2.4. Modulating module

The transmitted signals have serious distortions, in a wireless communication, thus rise the inter symbol interference(ISI) problems. we need a raised cosine filter to limit the bandwidth of the transmitted signals and to minimize the ISI. The filter tab coefficient of the pulse raised cosine filter has symmetric at center and the linear property in phase. The implementation for the FIR filter is generally convoutional sum of $x(n)$ and filter coefficient, h_k. The filter coefficient, h_k is stored in ROM and the entire tab number, N in the FIR digital filter is identical to the number of

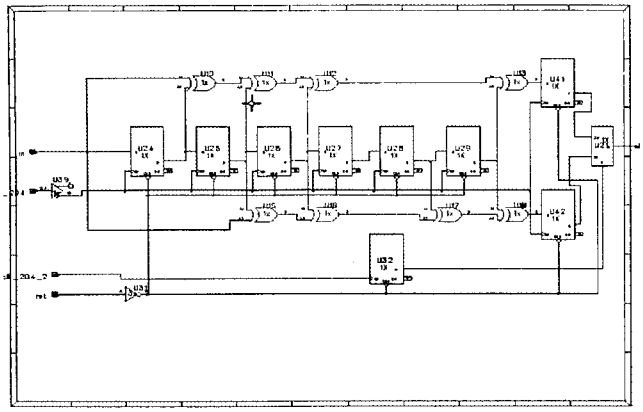

Figure 5: Schematic for the (133,171) 1/2 Convolutional Coder

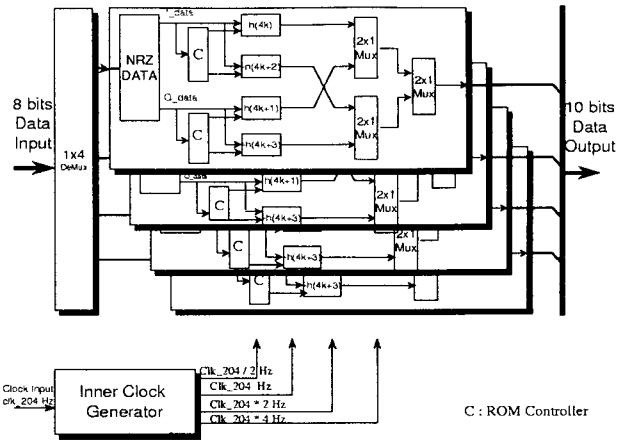

Figure 6: Block Diagram for a QPSK Modulation Module without Multipliers

multiplier. The filter output is presented by

$$y_n = \sum_{i=0}^{N-1} h_i x_{n-1} \tag{5}$$

The multiplication implemented in Eq.6 is limited in the high speed processing time over the entire transmitter system. In our design, we reduce the delay time and size by a practical use of the several properties of QPSK modulation. If we set the IF carrier frequency as four times of symbol rate, the modulated signal is presented by

$$S(n) = I(n)cos(\frac{\pi}{2}n) + Q(n)sin(\frac{\pi}{2}n) \tag{6}$$

where, $S(n)$ is the modulated IF signal, $I(n)$ and $Q(n)$ are the I/Q channel signals through the raised cosine filter. The coefficients(h_0 h_3) in each ROM block are stored as

$$\begin{aligned}
h_0(I_{N/2} : I_{(N-1)/2}) &= \sum_{i=-N/2}^{(N-1)/2} [I_i \cdot h\{iT\}] \\
h_1(Q_{N/2} : Q_{(N-1)/2}) &= \sum_{i=-N/2}^{(N-1)/2} [Q_i \cdot h\left\{\left(i+\frac{1}{4}\right)T\right\}] \\
h_2(I_{N/2} : I_{(N-1)/2}) &= \sum_{i=-N/2}^{(N-1)/2} [I_i \cdot h\left\{\left(i+\frac{1}{2}\right)T\right\}] \\
h_3(I_{N/2} : I_{(N-1)/2}) &= \sum_{i=-N/2}^{(N-1)/2} [Q_i \cdot h\left\{\left(i+\frac{3}{4}\right)T\right\}]
\end{aligned} \tag{7}$$

where, I_i and Q_i have 1 or -1 as a I channel and Q channel, T is a symbol period, and $h(t)$ is the impulse response of the FIR raised cosine filter with roll-off factor, $r = 0.35$. The cosine and sine signals are I/Q channel, i.e., I channel signals have 1, 0, -1, 0,... and Q channel signals have 0, 1, 0, -1,.... Therefore the modulated signals obtained by selecting the +(I channel signal), +(Q channel signal), -(I channel signal), -(Q channel signal),.... The designed QPSK modulator is shown in Fig. 6.

3. CHIP IMPLEMENTATION AND DESIGN PROCEDURE

The implemented chip is designed by top-down procedure. First, the circuit netlist is obtained from the front-end design and then the capacitance values in the circuit netlist are extracted. Second, the layout of the circuit netlist is designed by using the extracted capacitance information as a back-end design procedure, i.e., place and route(P&R). Before the synthesis, the statistical property of the spectrum distortion in band region and the spectrum suppression out of band region are considered by using the Matlab and Alta Group SPW BDE tools for the system level simulations. Then we complete netlists of the gate level by using the mixed design method, i.e. both VHDL code and Schematic. At the Avant's Compass tool, the generated netlist information are placed and routed. The results verified as the timing simulation including the capacitance information of the chip layout are compared with the simulation results at the system level. The last comparison and verification in the several chip environment is also achieved by using the Compass tool. The characteristic for the implemented chip is shown in Table 1. The result of P&R for the designed chip is shown in Fig. 7. For a chip test, we implement the IBM PC 8255 I/O board circuits and the two clock generator in designing the FPGA(i.e. target device type is $4028xhq240$). As shown in Fig. 8, the function operation of the implemented chip is displayed and verified by controlling the in-

Table 1: Chip Specification

Design Consideration	DATA
Technology	0.8 um CMOS /cmn8a
Base array	vgc400186
Max. clock freq.	40 MHz
Num. of gate	26,785 gates
Num. of I/O pins	136 pins
Input/ Out / Bi	11/81/16
VDD/ VSS	12/16
Power consumption	900 mW
Input word length	8 bits
Output word length	10 bits
Chip size	6.7 mm x 6.7 mm

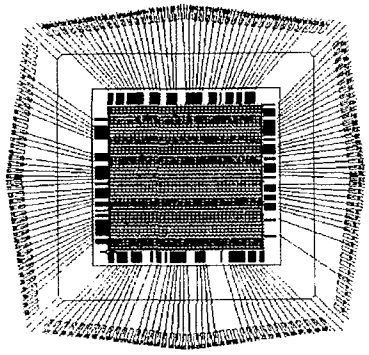

Figure 7: The Bonding Diagram for the Designed Chip

put and output signals at PC. The simulation result of the error protected modulation-data is shown in Fig. 9.

4. CONCLUSION

In this paper, an all digital high speed QPSK transmitter for MPEG-2 packets supporting the DAVIC designed and implemented in detail. To get a high speed process, entire functional modules had a parallelized and pipelined structure. Especially, the GF multiplier in the shortened RS(204,188) code was designed as a parallel input and parallel output GF(2^8) multiplier based on the standard basis, which was reduced complexity and critical path in a basic cells by using the known coefficient values of the primitive polynomial over the GF(2^8). For the QPSK modulator, we removed the multipliers used in a conventional modem to get a high operating speed and to reduce the number of gates. The efficiency of the H/W is improved by replacing the simplified root raised cosine filter considered a low pass filter(LPF) to a ROM table.

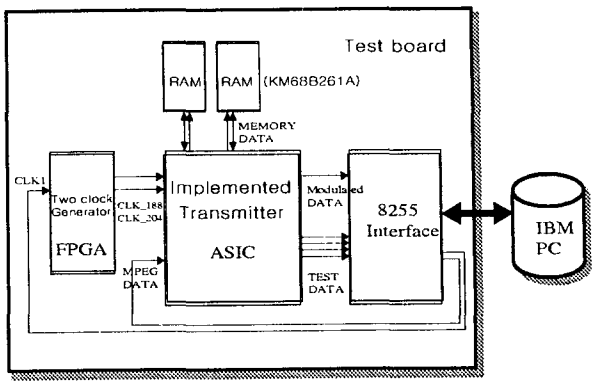

Figure 8: Test Board for Implemented Chip

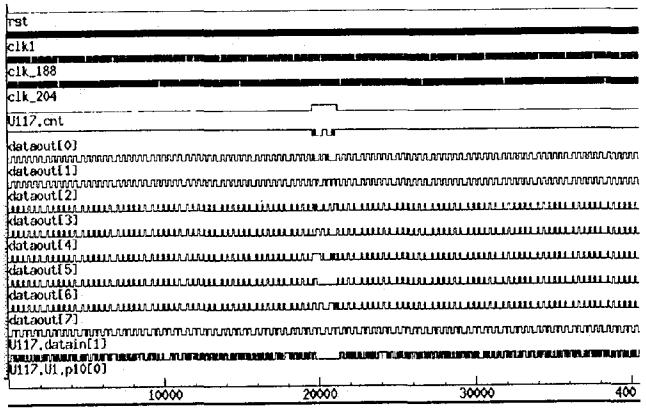

Figure 9: Simulation Result for the transmitter system

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