A New Curvature-Compensated CMOS Bandgap Reference with Low Power Consumption

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Abstract: We propose a new curvature-compensated CMOS bandgap reference circuit that is achieved by varying a current ratio. The proposed circuit is shown to have small temperature coefficient that the output voltage variation is 0.4mV.

1. Introduction

The bandgap reference(BGR) is widely used in almost all VLSI ICs because of its good temperature stability. Specially, the DTCXO(Digital Temperature Compensated Crystal Oscillator) system, as shown in Figure 1, requires highly precise reference voltage for the accurate output frequency[1]. In the DTCXO system(Figure 1), it is necessary that both the temperature sensor and ADC require highly accurate reference voltage over temperature variation for sub-ppm frequency accuracy. Hence, an essential component of the DTCXO is a bandgap reference circuit.

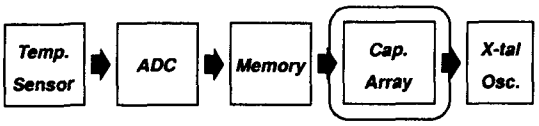

Figure 1. Block diagram of the DTCXO(Digital Temperature Compensated Crystal Oscillator) system.

Figure 2 shows an example of a classic CMOS BGR implementation[2]. Two diodes, D1 and D2, have the same area to reduce mismatch between two diodes and the current of D2 is larger by factor α than that of D1[2] because the diode matching property is worse than MOSFET's in the standard CMOS process. The output voltage is given by

$$V_{out} = V_{D2} + \frac{C_1}{C_2}\Delta V_D = V_{D1} + \left(1 + \frac{C_1}{C_2}\right) V_t \ln(\alpha) \quad (1)$$

, where V_D is forward diode voltage, ΔV_D is the difference between the diode voltages of D1 and D2, V_t is thermal voltage, and a constant value of α is the current ratio between two diodes. It is well known that the output voltage as a function of temperature in a classic BGR circuit displays a curvature[3] due to the nonlinear behavior of the diode voltage with respect to temperature. Several curvature-compensated BGR circuits were proposed[3][4] by using BJTs which are not easy to implement in a standard CMOS process.

In this paper, we propose a new curvature-compensated BGR circuit with low temperature coefficient which is achieved by varying a current ratio(α) controlled by a diode voltage of V_{D1}.

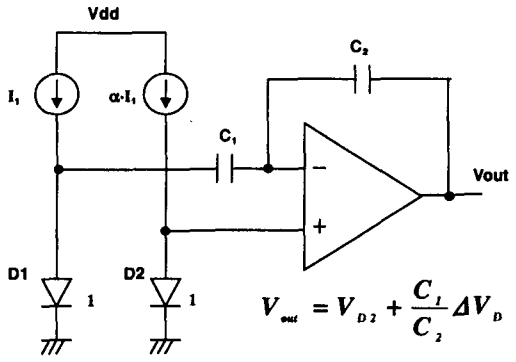

Figure 2. An example of classic CMOS BGR circuit.

2. A New Curvature Compensated Method and Its Implementation

Figure 3 compared the concepts of conventional and the proposed BGR. The output voltage of the classic BGR(Figure 2) is the sum of a diode voltage and a PTAT(Proportional To Absolute Temperature) voltage (see Eq. (1)), as shown in Figure 3(a). Because the diode voltage has inherent curvature, the output voltage has curvature also. Figure 3(b) shows the proposed BGR concept. The output voltage is sum of a diode voltage and the modified PTAT voltage with the symmetrical curvature of a diode voltage, which make it possible to produce almost temperature-independent output voltage.

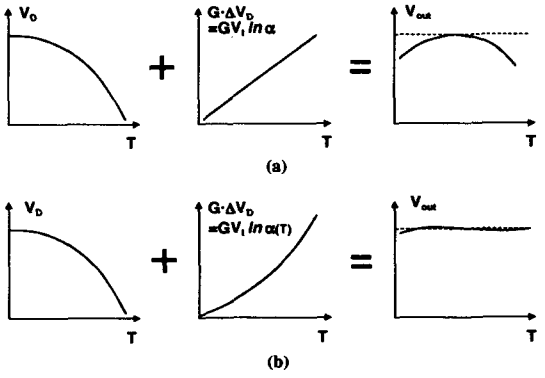

Figure 3. The concept of (a)the classic BGR and (b)the proposed BGR. $G=C_1/C_2$.

The new proposed curvature-compensated BGR to implement the concept in Figure 2(b) is shown in Figure 4. M3 generates adaptive current controlled by V_{D1} for curvature compensation. As the temperature increases, the diode voltage of D1 decreases and the current of M3 increases, which makes curvature compensation by increasing the current ratio of D1 and D2. The current ratio, α is expressed as follows:

$$\alpha = \frac{(W/L)_4}{(W/L)_2} + \frac{(W/L)_3}{(W/L)_2} \cdot \frac{(V_{DD} - V_{D1} + V_{Tp})^2}{(V_{SG2} + V_{Tp})^2} \qquad (2)$$

, where V_{Tp} is the threshold voltage of the pMOSFET. The sizes of M3 and M4 for a given capacitance ratio of C_1/C_2 should be determined to diminish the temperature dependence of the output voltage.

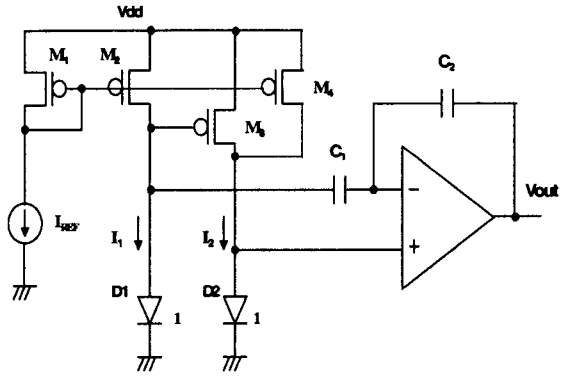

Figure 4. The proposed curvature-compensated BGR circuit.

3. Design Results

For low voltage design, folded cascode opamp[5], as shown in Figure 5, was used in the proposed BGR circuit. Common-mode input range of opamp should be covered range from 0.8V to 0.3V of diode voltage variation as a function of temperature, so input transistors consisting of M5 and M6 are pMOSFETs. The opamp performance is summarized in Table I.

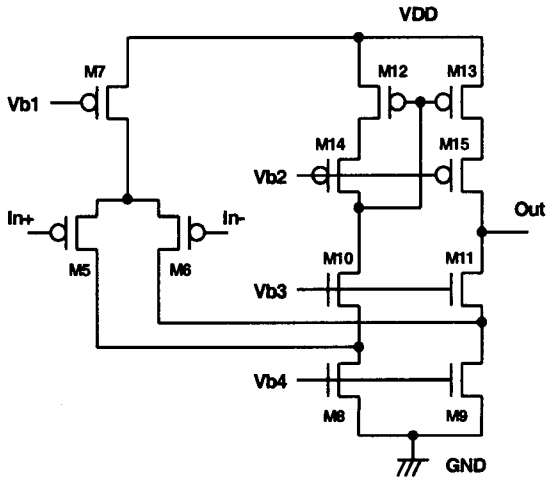

Figure 5. Folded-cascode opamp schematic.

Table I. Performance summary of opamp.

Power supply voltage	2.5 V
Power consumption	61 μW
Open loop gain	59 dB
Phase margin (at 1pF load)	70°
Common mode input range	0.1 – 1.7 V

Figure 6 shows the simulated curves of the modified PTAT voltage, as illustrated in Figure 3(b), compared with the PTAT voltage. This result is well suited for the proposed concept. The difference between the modified PTAT and PTAT is compensated with the nonlinear diode voltage and hence the temperature-independent output voltage can be produced.

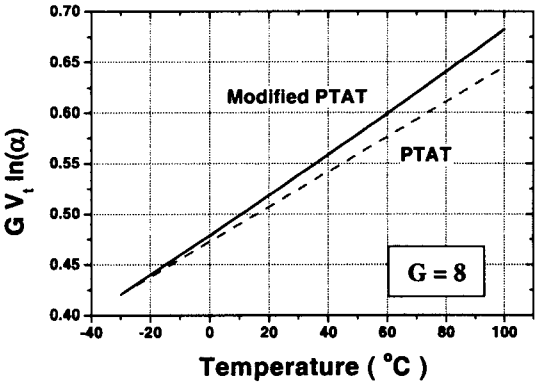

Figure 6. The simulated curve of the modified PTAT. The difference between the modified PTAT and PTAT is compensated with the nonlinear diode voltage and hence the temperature-independent output voltage can be produced.

The maximum output voltage variation over the temperature range from –30°C to 100°C is illustrated in Figure 7 where the x-axis is the size of M3 and the y-axis is the size of M4. The capacitance ratio of C_1/C_2 is 8. As shown in Figure 7, the optimum sizes of M3 and M4 are 10.5/10 μm and 15.3/10 μm, respectively.

Table II gives the optimized design parameters in the proposed circuit(Figure 4). The reference current(I_{ref}) is 3.3μA at 300K and diode area is 400μm^2.

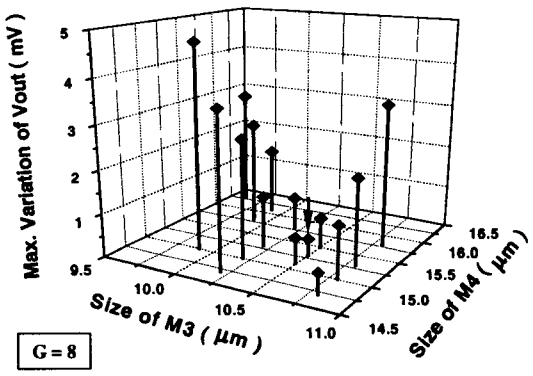

Figure 7. The maximum variation over the temperature vs. the sizes of M3 and M4. The marker represents the optimum design point.

Table II. Device sizes of the proposed BGR circuit.

M1, M2	2.1/10	C_1/C_2	8
M3	10.5/10	I_{REF}	3.3 μA at 300K
M4	15.3/10	D1, D2	20×20μm²

Figure 8 shows the simulated output voltage versus temperature. Insert figure shows output voltage characteristics of a classic BGR. Maximum output voltage variation of the proposed BGR is within 0.4mV while that of classic BGR is 2.5mV.

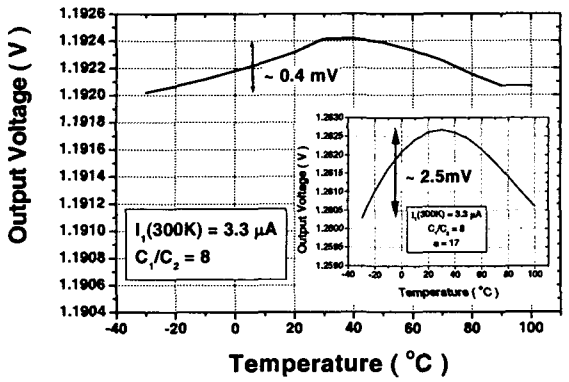

Figure 8. The temperature dependency of the simulated output voltage. Insert figure shows the output of the classic BGR.

The proposed BGR circuit with G=8 was laid out using a 0.5-μm double-poly triple-metal CMOS technology. Because it is important the capacitance ratio of C_1/C_2, the common-centroid layout method should be used. The layout view of the proposed BGR, which occupied the layout area of 225×150μm², is shown in Figure 9. In this design, there is another advantage of small layout area because two diodes have the same area.

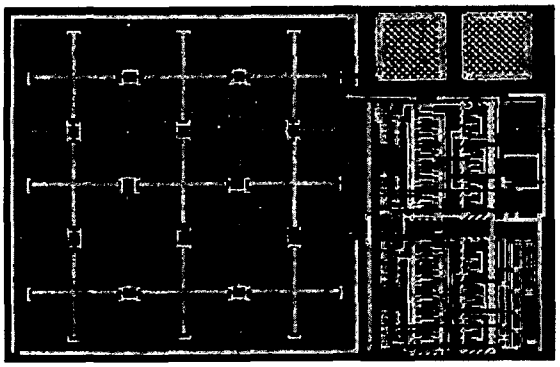

Figure 9. The layout of the proposed BGR with G=8 using 0.5μm double-poly triple-metal CMOS technology. The layout area is 225×150μm². The output pads are not shown.

Table III summarizes the performance of the proposed circuit. The output voltage has small variation over the temperature and the power consumption of the proposed BGR circuit is 216μW at the power supply voltage of 2.5V. Also the layout area is small.

Table III. Summary of the proposed BGR circuit.

Technology	0.5 μm CMOS
Power supply voltage	2.5 V
Power consumption	216 μW
Max. output voltage variation	0.4 mV
Layout area	225×150μm²

4. Conclusion

We proposed a new scheme of curvature-compensated BGR circuit by adaptively adjusting a current ratio as a function of temperature. The proposed BGR has the maximum output voltage variation of only 0.4mV over the temperature range from –30°C to 100°C.

Acknowledgement

This work was supported in part by the Korea Science and Engineering Foundation through the MICROS center at KAIST, Korea. Also this research is a part of University Research Program supported by the Ministry of Information and Communication in Korea. And the authors wish to thank Seungho Han at Shin-Sung Electronics, Pusan, Korea for his technical assistance.

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