고성능 패키징 설계를 위한 시뮬레이션

이 춘 홍 박사
(Amkor Technology Korea)

Packaging Simulation for High Performance

for IMAPS

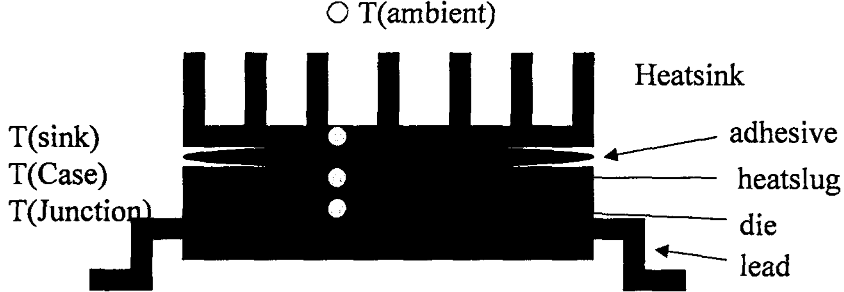
C. H. Lee
R & D Center
Amkor Technology Korea

Thermal Management

- ➯ Threshold power above which thermal enhancement is required : 1.5W
- ➯ Power variation of Microprocessor(MPU) of PC
  - ➢ 5W in 1989
  - ➢ 10 W in 1995
  - ➢ 13 - 16 W in 1996
  - ➢ 34 W in 1997
  - ➢ 20 W (low end Celeron) - 40 W (high end Xeon) today
  - ➢ 30 - 35 W for Pentium III at 500 MHz
  - ➢ 50 - 70 W expected for upcoming Merced and McKinley
- ➯ Power variation of Memory
  - ➢ 0.3 - 1.0 W for a typical SRAM in 1998
  - ➢ 2 W for high end memories for workstation today
- ➯ High power generation in power supply module
  - ➢ 1200 W for power supply and fuel injection module by Outboard Marine Corporation

Heat transfer mechanism

- Thermal resistance Θja = (T(junction) - T(ambient)) / power
- Θja is a combination of Θjc and Θca.



- Major heat transfer mechanism
  - conduction (from solid to solid) : from the pkg to the circuit boards or to the external heatsink

    R_{cond} = L / (K x A) : L (distance the heat travels)
    K (thermal conductivity W / mC)
    A (cross-sectional area)

  - convection (from solid to fluid) : from the pkg heat sink or the circuit boards to the surrounding medium (mostly air)

    R_{cond} = I / (h x A) : I (distance the heat travels)
    h (convective heat transfer coefficient)
    A (surface area for convective heat transfer)

Thermal Solutions

- without external heat dissipating components : over 70 % of the generated heat flows to the air through the board
- with embedded metal planes in the circuit board : over 90 %
- Leadframe packages
  - factors affecting thermal performance
    - pad/inner lead gap
    - pad size
    - leadframe material
    - thermal molding compound

⇨ Thermal solutions by assembly level

Packaging level	Thermal solution	Applicati
Die Level	Die Attach :	die attach to substrates
	–Silver or diamond particles filled in epoxy	
	Thermally enhanced molding compound :	power and discrete Ics
	–Silicon-coated AlN	
	Heatspreader and heat slug	power modules and
	–Copper, Aluminum, Cu/W, Diamond film, AlSiC	thermally enhanced pkgs
Board / Module level	Thermal substrate :	IGBT
	–Ceramics (Al_2O_3), AlN, Direct bond copper	Automotive engine control unit, DC/DC converter, Motor controls
	–Insulated metal substrate (IMS)	
	–Flex-on-metal (FOM)	
	Heatsin	power discretes, MPU, ASICs
	–Cu, Al alloys	
	Heatpipe :	Notebook, power modules, SCR, IGBT
	–Evacuated vessels back-filled with a small quantitiy of a working fluid such as ammonia, water,acetone and methanol	

Thermal management technology

⇨ Thermal interface material : to fill the physical gap

➢ basic elements :

- filler : various oxide, nitride, precious metal powders
- binder : polymeric resin to provide a supporting matrix and compliance
  silicone, epoxies, acrylics
- reinforcement : optional to provide additional rigidity and strength
  woven glass, polyimide films, metal foils

➢ materials :

- grease/paste : silicone oil loaded with fillers
- adhesive : acrylic or epoxy adhesive with fillers
- pads : silicone with fillers. Reinforced by woven glass, polyimide film,
  or metal sheets. 20 - 100 mil thick. Applicable to board assembly
- films/tapes : similar to pad, but 2-20 mil thick. Tapes have adhesive
  coating on both sides.
- phase change : fillers filled paraffin-based or thermoplastic polymers
  solid at room temp and liquid above 40-60 C(T(change)

⇨ Thermal dissipation component

➢ heatspreaders and heatslugs : Cu, Al, Cu-W, Cu-Mo, Cu-C, AlSiC,
brand name composite: Dymalloy, Silvar

➢ heatsinks : Cu, Al
- fabrication methods : stamping, extrusion, casting, folding, swaging
- folded fin heatsink : folded fin aluminum sheet-stock bonded directly to an aluminum base plate-like the radiator in a car

➢ heatpipe : employing a small quantity of working fluid in evacuated vessels heat transfer by the evaporation and condensation of the fluid.
- principle : The internal walls of the evacuated cylindrical vessels are lined with a capillary structure or wick that is saturated with a working fluid. As the heat is applied at the evaporator, the fluid id vaporized, and a pressure gradient is created in the pipe. This pressure gradient forces the vapor to flow along the pipe to the cooler section where it condenses, giving up its latent heat of vaporization. The working fluid is then returned to the evaporator by capillary forces developed in the wick structure.
- carrying a few watts or several kilowatts

- for the applications of a 6 to 8 watt heat load, 4 - 6 C/W
- high end chips dissipating in the 75 to 100 watt range, the thermal resistance is only 0.2 - 0.4 C/W
- Cu/water is used where the junction tmep needs to be maintained below 125-150 C.
- Cu/methanol is used in the case of an operating temp below 0 C.

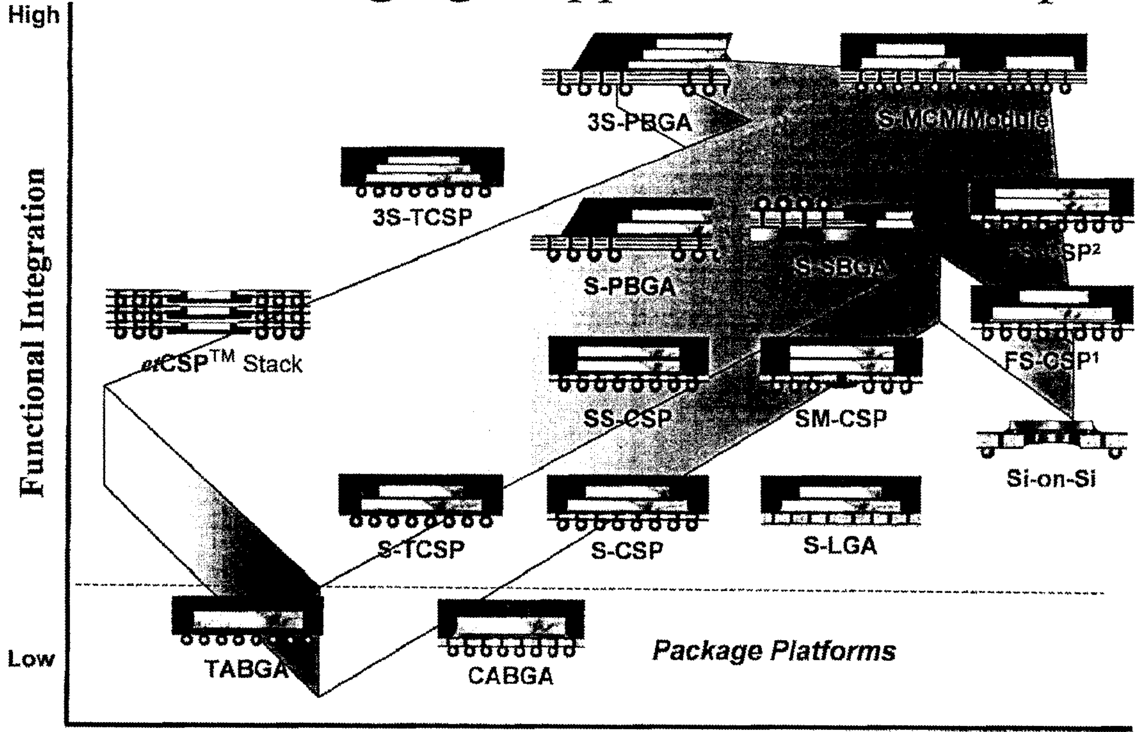
⇨ Thermal substrate

➢ direct bond copper

➢ flex-on-metal

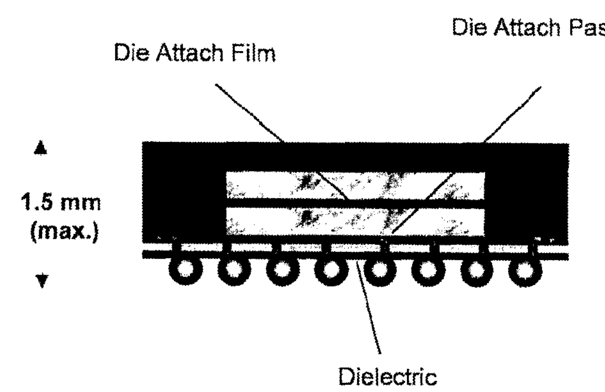
➢ insulated metal substrate(IMS) : cheapest solution
- Structure : 3 layers : The base layer 1.5 mm thick Al or Cu
a dielectric layer : a blend of heat resistant epoxy resin w ceramic fillers
35 um thick Cu foil
- Application : DC/DC converter by Lucent, which ranges in power dissipation from 50 to 600 W.

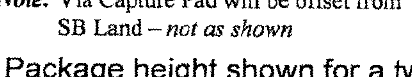
3D Packaging – *Application Roadmap*



Same Size Die Stacking: BGA format, Laminate Substrate

Peripheral bond pads: face-up configuration with W/B interconnection: no chip redistribution or Interposer required



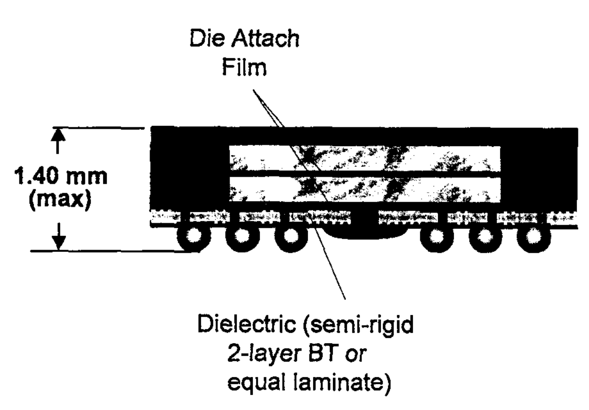

Note: Via Capture Pad will be offset from SB Land – *not as shown*

Package height shown for a two metal thin-core (0.10 mm) substrate.

- Dual Flash, Dual SRAM or Combination of Flash/SRAM
- Cellphone, Mass Storage Market - Doubling of Capacity/Same Footprint!
- Cost Effective
  - Ease of design for S/S
  - CABGA/TABGA/SCSP Platform
  - Known Materials/Equipment Set
  - Extendable across numerous product lines.
- Key Customer Interest
  - ST Micro, Atmel (have active designs, huge interest)
  - Erricson ready to test units.

Same Size Die Stacking– *Memory S-CSP* Structure

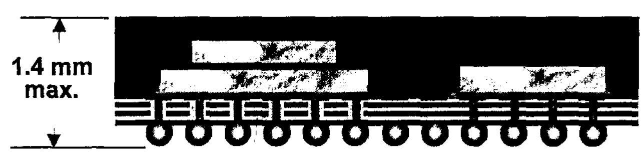
One die with center bond pads: back to back die configuration:
W/B interconnection



Package height shown for a two metal thin-core (0.10 mm) substrate.

- Flash/DRAM or SRAM/DRAM
- Cellphone, PDA's, Storage
- Utilizes Micro BGA/*Memory*CSP Toolsets along with Stacking technology developed with Film and/or Paste.
- Key Customer Interest
  - Nokia, Motorola Cellular and Ericcson have expressed interest.
  - Further market study required.
  - Need to penetrate Flash customers, most likely to take lead as per Flash/SRAM (Intel, Atmel, ST Micro).
  - Flash Product Mgr. to OWN (Bruce Schupp).

S-Module – S-MCM Proposed Structure

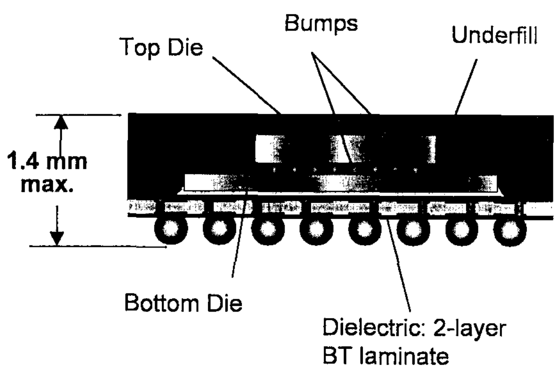


Dielectric

Note: Via Capture Pad will be offset from SB Land – *not as shown*

Package height shown for a two metal thin-core (0.15 mm) substrate.

*Stacked*CSP: Flip Chip and W/B Interconnection

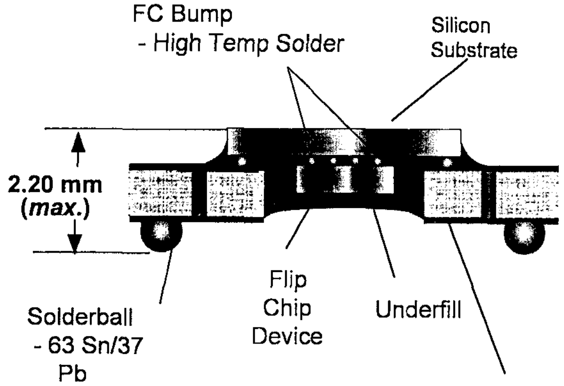


- SiGe (FC Die) on Asic (MSM)
- Cellphone, Set-Top Boxes, Etc.
- Key Customer Interest
  - IBM, Atmel (ES2 in Europe)

Note: Via Capture Pad will be offset from SB Land – *not as shown*

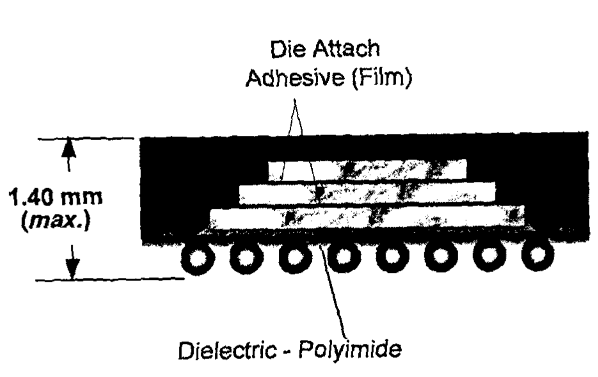
Package height shown for a two metal substrate.

*Stacked*CSP – Si-on-Si Structure



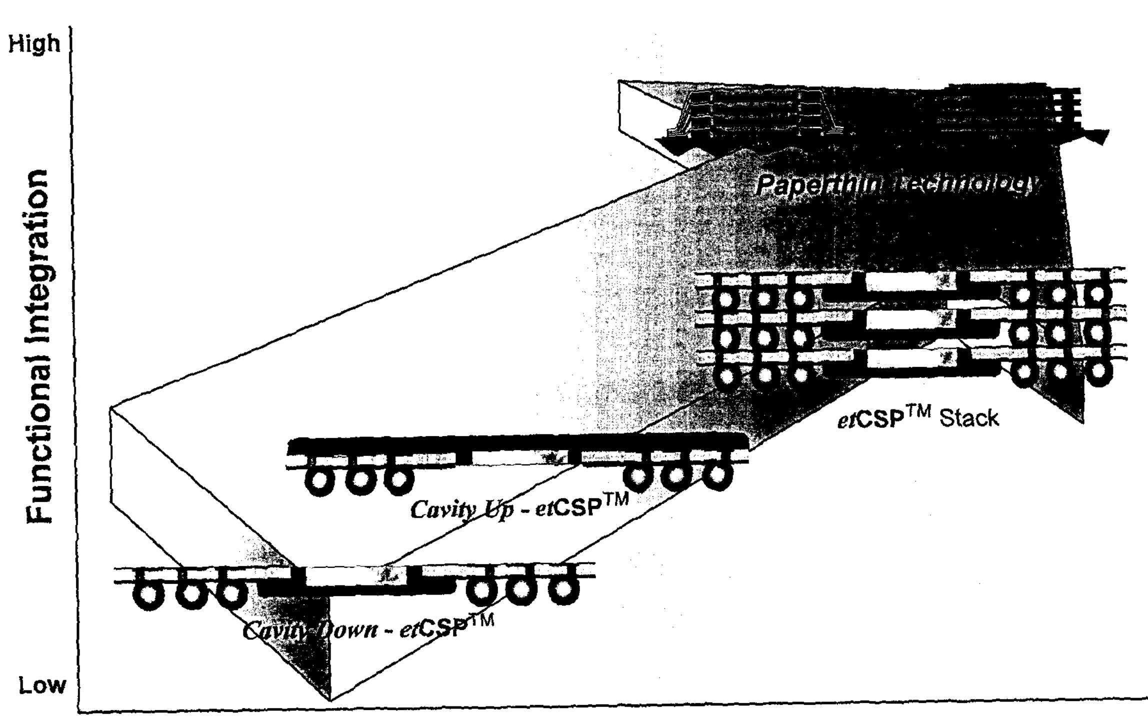
BGA SubstrateSemi-rigid 2-layer laminate (shown)

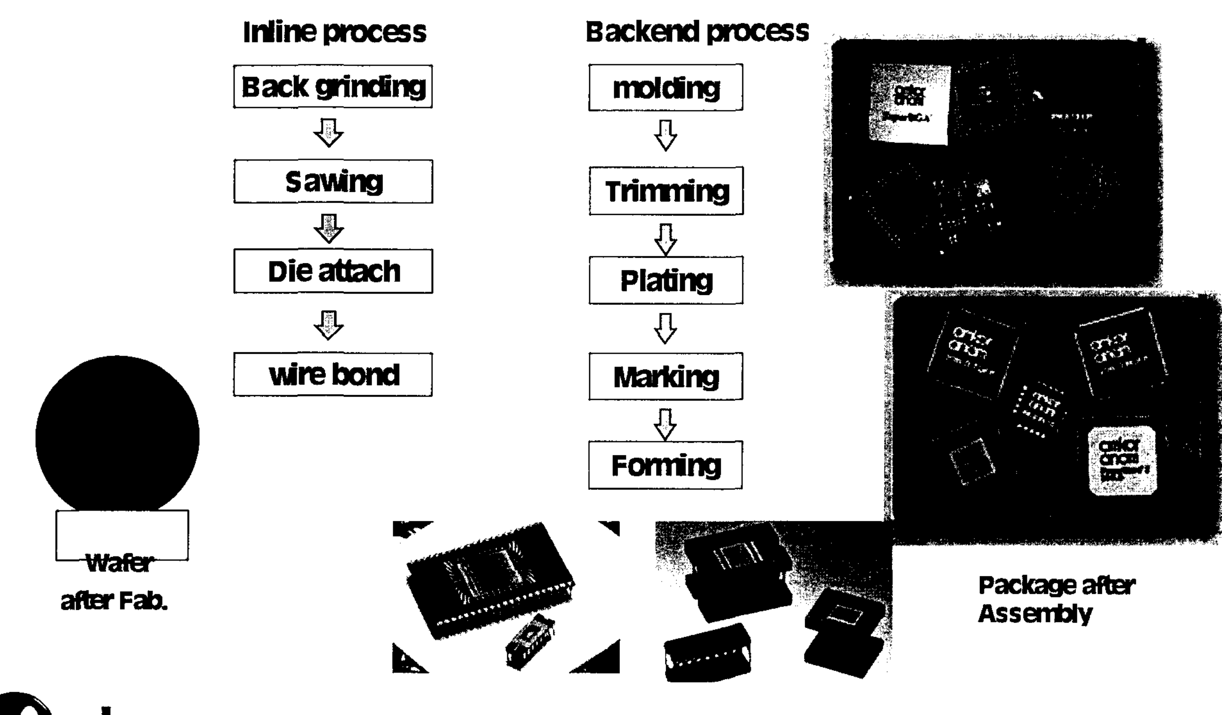
*Stacked*CSP – 3 Die Stacked Structure



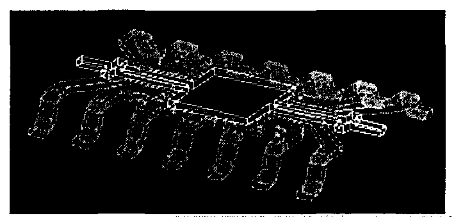
- Flash/Flash/SRAM or Flash/SRAM/SRAM or Asic/Flash/SRAM
- Cellphone, Set-Top Boxes, Etc.
- Extension of our Tape SCSP Development
- Key Customer Interest
  - Intel (NCG) - Network and Set Top Grp. (ASIC/Flash/SRAM combo in PBGA Footprint).
  - 3 Die in 1.4mm footprint will be difficult due to die design, die availability.

Extremely Thin Packaging – *Dev. Roadmap*



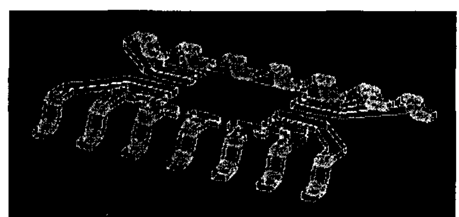


Electrical Molding Examples

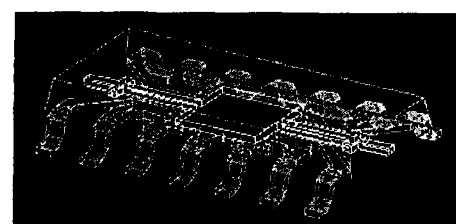


Inductance(H)

	lead01:Int1	lead02:Int2	lead03:Int03	lead04:Int04
lead01:Int1	2.20e-09	6.75e-10	1.84e-10	1.25e-10
lead02:Int2	6.75e-10	1.27e-09	2.56e-10	1.46e-10
lead03:Int03	1.84e-10	2.56e-10	7.74e-10	2.33e-10
lead04:Int04	1.25e-10	1.46e-10	2.33e-10	8.06e-10



	lead01:Int1	lead02:Int2	lead03:Int03	lead04:Int04
lead01:Int1	2.21e-09	6.71e-10	1.84e-10	1.26e-10
lead02:Int2	6.71e-10	1.26e-09	2.57e-10	1.46e-10
lead03:Int03	1.84e-10	2.57e-10	8.01e-10	2.36e-10
lead04:Int04	1.26e-10	1.46e-10	2.36e-10	8.34e-10



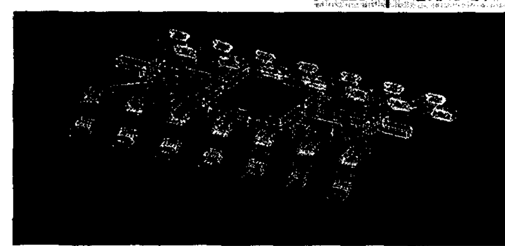
Capacitance(F)

	lead01	lead02	lead03	lead04
lead01	5.23e-13	-2.13e-13	-2.44e-14	-1.98e-14
lead02	-2.13e-13	3.93e-13	-9.61e-14	-8.66e-15
lead03	-2.44e-14	-9.61e-14	2.52e-13	-5.03e-14
lead04	-1.98e-14	-8.66e-15	-5.03e-14	2.37e-13

	lead01	lead02	lead03	lead04
lead01	4.39e-13	-2.20e-13	-2.28e-14	-9.47e-15
lead02	-2.20e-13	3.88e-13	-1.04e-13	-9.86e-15
lead03	-2.28e-14	-1.04e-13	2.31e-13	-5.91e-14
lead04	-9.47e-15	-9.86e-15	-5.91e-14	1.97e-13

Package mounted on the board with ground plane

	lead01	lead02	lead03	lead04
lead01	5.82e-13	-1.96e-13	-1.78e-14	-1.54e-14
lead02	-1.96e-13	4.30e-13	-8.71e-14	-5.40e-15
lead03	-1.78e-14	-8.71e-14	2.83e-13	-4.22e-14
lead04	-1.54e-14	-5.40e-15	-4.22e-14	2.69e-13



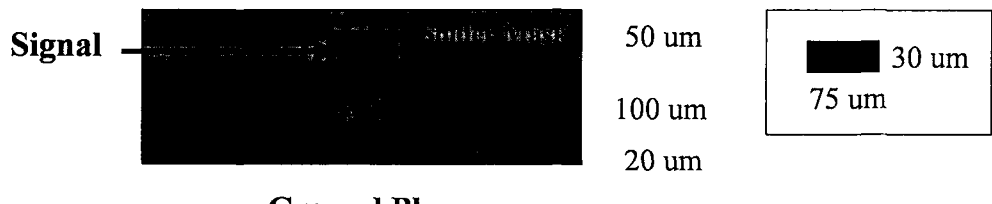
	lead01:int1	lead02:int2	lead03:int03	lead04:int04
lead01:int1	2.15e-09	6.49e-10	1.83e-10	1.29e-10
lead02:int2	6.49e-10	1.24e-09	2.42e-10	1.39e-10
lead03:int03	1.83e-10	2.42e-10	7.60e-10	2.14e-10
lead04:int04	1.29e-10	1.39e-10	2.14e-10	7.49e-10

Formula for Wire Parasitics

	1.3 mil	1.1347x - 0.6149
L(nH)	1.2 mil	1.1876x - 0.6859
	1.0 mil	1.1982x - 0.6016
	1.3 mil	0.0965x - 0.0476
C(pF)	1.2 mil	0.0864x - 0.0358
	1.0 mil	0.071x - 0.0141
	1.3 mil	33.494x - 5.3771
R(mOhm)	1.2 mil	34.41x - 3.5126
	1.0 mil	39.734x - 0.7367

X is in mm.

Model Description: operating frequency = 3.2 GHz



Results : For the signal length of 10000 um,

Capacitance : 0.926 pF
Inductance : 4.3 nH
Characteristic Impedance : 68.15 Ω

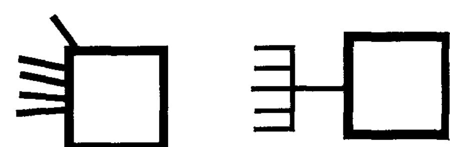
Cross Talk Analysis : 5 V, 100 MHz

Model	2 wires with diameter of 1 mil and spacing of 1 mil	2 wires with a ground plane below EMC	2 wires with diameter of 1 mil and spacing of 2 mil	2 wires and 1 ground wire inserted between them
Cross Talk	- 7.03 dB	- 14.36 dB	- 8.21 dB	- 21.92 dB
Induced Voltage	0.73 V	0.4 V	0.61 V	0.17 V

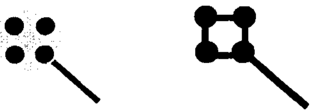
Design Guideline

- Power/Ground Rings
  - ➩ Use as many vias as possible to connect the ring to inner power /ground planes. Minimize the distance between the vias and bond wires.

  - ➩ Increase the number and width of the traces coming out of the ring.



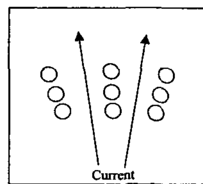
☞ If possible connect adjacent solder balls.

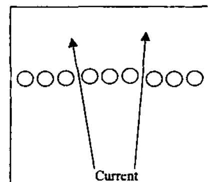


☞ Try to assign solder balls close to power/ground ring.
☞ maximize the thickness of the ring and traces.
☞ If there is room to adjust the ring size, adjust it such that the total the total inductance is minimized. Bondwires contribute more to inductance than traces in the microstrip structure while traces contribute more to inductance than bondwires in the coplanar structure

• Power/Ground Planes

☞ Minimize the number of via holes in the power/ground planes
☞ Arrange via holes in proper locations to avoid blocking current flow from plane center to plane peripherals.





☞ The thicker the plane the smaller(better) inductance for the planes.