Wafer-Level CSP(Omega CSP)

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Contents

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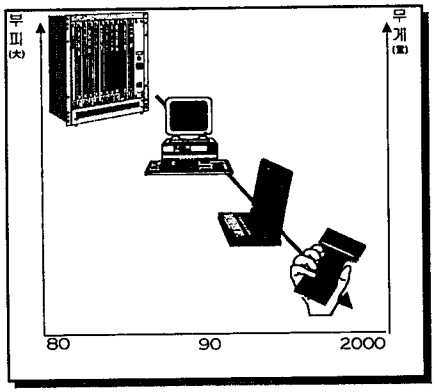
System Trend



WLCSP
CSP
MCM
MCP

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Why, WLCSP?

Characteristics of WLCSP

1. Low Cost
2. High Electrical Properties
3. Smallest PKG Size(Real Chip Size PKG)
4. Good Thermal Properties(w. H/S)

But, Current WLCSP shows
Low S/J reliability
Foot Print Standard Problems

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Application

Current Market

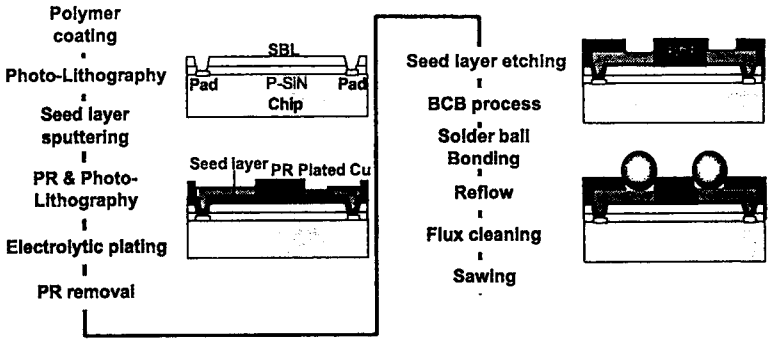
- Low I/O & Small Chip
- Flash
- Large Die with underfill

• *Improving S*
• *Foot Print*
Standardizat

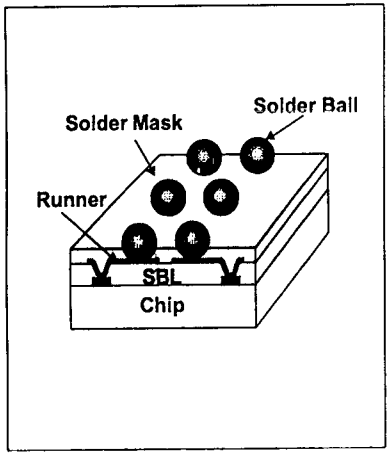
Future Market

- DRAM
- SRAM
- Large Size Devices

Process

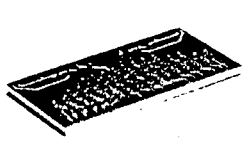


Omega CSP

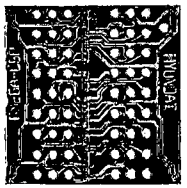


- 1st Polymer layer
  - SBL Layer
  - PKG CTE be close to PCB CTE
    => Reduce Stress acting on S/J
- Runner(Conductive Trace)
  - Ti\Ni\Cu
  - Ti\Cu
- 2nd polymer layer
  - Solder Mask
- Eutectic Solder Ball

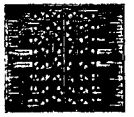
Omega-CSP



72 M DRD



128 M DRD package



4 M SRAM

Solder Joint Reliability

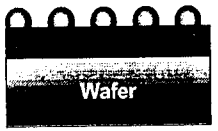
❑ Strain on Solder Joint(ε_{total})

$$\varepsilon_{total} = \varepsilon_{macro} + \varepsilon_{micro}$$

$$\varepsilon_{macro} = \Delta\alpha \ \Delta T \ L$$

❑ Thermal Fatigue Life(N_f)

$$N_f \propto \varepsilon_p^{c} \quad (c < 0)$$



❑ Inelastic Strain at Solder joint

- ☛ CTE mismatch between PKG & Board
- ☛ Solder Stand-off height

❑ PKG CTE

- ☛ Depends on Polymer properties, thickness
  Wafer Thickness

Solder Joint Reliability Improvement

❑ **SBL Material**

❑ **Solder ball Size**

✓ 0.35, 0.45 mm

❑ **Runner metal thickness No**

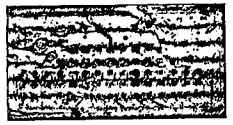
✓ **1, 2, 3, 4, 5**

❑ **Distance from Neutral Point**

❑ **Condition B, - 55 ~ 125 ℃**

❑ **Daisy chained PKG & Board**

PKG CTE measurement by Moire Fringe



(i) U-Field

(ii) V-Field

Omega CSP

❑ **Chip Thickness**

✓Omega CSP : 0.5mm

✓CSP1 : 0.35mm

❑ **PKG CTE_{Global} Test Condition**

✓ ΔT = -80℃(100℃ => 20℃)

❑ **PKG CTE Test Results**

✓ Omega CSP : 5.5ppm/℃

✓ CSP1 : 3.9ppm/℃

cf) 2.7ppm/℃ for Bare Chip

☛ **S/J Life Cycle increment by PKG CTE Increasing**

✓Omega CSP : 1st Fail at 300 Cycles

✓CSP1 : 1st Fail at 500 Cycles

Solder ball size - Moiré Fringe Analysis

U-Field

❑ **Shear Strain measurement**

✓ Condition : 100 to 24℃ cooling

✓ 0.35 ball : 0.54 %

✓ 0.45 ball : 0.43 %

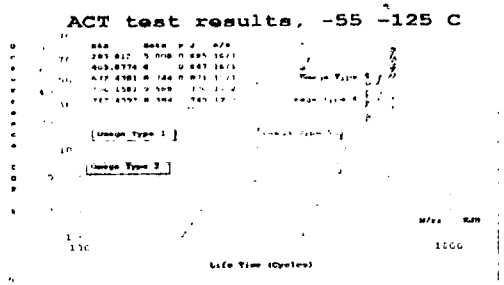
V-Field

❑ **Life Cycles increasing by Strain decreasing with Ball Size**

✓ 1st Fail at 300 cycles for 0.35 Ball

✓ 1st Fail at 500 Cycle for 0.45 Ball

Runner Thickness Effects - S/J ATC results



PKG type	Runner Thick. No	1st Failure (cycles)	Characteristic Life(cycles)	β	Fail Mode
Omega 72	1	200	294	5.0	Runner
	2	400	405	6.0	
	3	500	672	8.7	Mixed
	4	500	706	9.6	Solder
	5	500	712	8.4	

Package Reliability

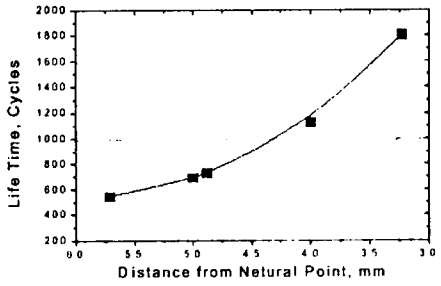
- ❑ **Electrical Performance**
  - ✓ D-RDRAM
  - ✓ SRAM
- ❑ **Temperature cycling**
  - ✓ Electrical Test
  - ✓ Ball shear strength
- ❑ **Pressure Cooker Test**
  - ✓ Delamination check

Chip size effect

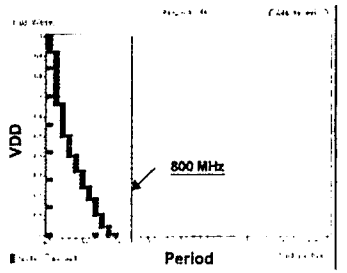
Experimental Results

PKG type	DNP (mm)	1st Failure (cycles)	Characteristic Life(cycles)	Solder	Moiré Analysis	
					Shear strain %	PCB Bending μm
Omega 48	3.23	1700	N.A	Sn-Pb	0.29	1.46
Omega 72	5.71	500	706	Sn-Pb	0.43	5.5

Simulation



Electrical Performance

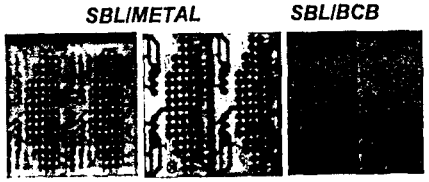


- ❑ **Electrical performance test**
  - ✓ **72 M D-RDRAM**
- ❑ **Test condition**
  - ✓ Temp : Room Temp
  - ✓ Vdd : 2.37/2.50/2.63
  - ✓ Frequency : 800 MHz
- ❑ **Result**
  - ✓ Similar performance to μ-BGA, higher data transfer rate than 800MHz

Pressure Cooker Test

❑ **Pressure Cooker Test**

- ✓ 100% Humidity, 121℃
- ✓ Passed 100 hours
- ✓ No delamination



Summary

Current Status

Good Electrical performance for high speed device

Solder joint reliability

- Passed 1600 cycles for 4M SRAM (3.27 mm DNP)
- Passed 400 cycles for large die (5.71 mm DNP)

Future Plan

Improving Board-Level Reliability for large die size

Lead free solder evaluation