High Density Processing for Flip Chip Package

Sho-ichi Koyama,
SHOICHI_KOYAMA@mail.shinko.co.jp,
Shin-ich Wakabayashi
SHINICHI_WAKABAYASHI@mail.shinko.co.jp
Shinko electric industries CO.LTD. Material & process research Dept

1, Introduction

These days, owing to the development of high performance electronic products, huge volume of information can be simultaneously and speedily exchanged on internet or telecommunication systems. Multimedia using cellular phones and handy cameras becomes much popular in our daily life. In these systems, technology for high density and fine patterning in semiconductor chips and packages have been contributed to the development.

Clock frequency in advanced chip already reached to the range of GHz with introducing a new architecture and a new process called damashin for finer line formation with copper in less than 0.13μm. Packaging and assembly technology are changing from ordinal surface mount type such as OFP and SOP to area array type to deal with high pin count interconnects. In package, a build up package with high density and fine patterns has been much required to mount a high pin count chip as replacing a multi laminated package with CCL boards. In chip assembly, flip chip interconnect has introduced as alternative of wire bond connect. Further more, these technologies have been developed to increase the performance and to decrease the cost.

In this paper, current statuses of organic build up package for MPU and ASIC applications, package structure, used materials and design are descried to suggest the assignments on next generation package.

2, Build up package structure

Road map on logic type chips and packages used for it are shown in table 1[1] In the chip, clock frequency goes up and

Table1 Road map of chip and package (Source : SIA, ITRS)

	Years of first product shipment	*1997*	*1999*	*2002*	*2005*	*2008*	*2011*
	technology node	*250nm*	*180nm*	*130nm*	*100nm*	*70nm*	*50nm*
Semiconductor	Performance: on chip/MHz						
	Cost-performance	350	526	928	1108	1468	1827
	High-performance	600	958	1768	2075	2574	3083
	Power(W)						
	Cost-performance	28	48	68	96		169
	High-performance	70	88	120	170		174
Package	Package pin count						
	Cost-performance	256-568	300-700	378-957	476-1309	600-1791	755-2449
	High-performance	1136	1400	1915	2619	3581	4898
	Flip chip pad pitch/μm	250	200	150	100	70	50
	Line width/μm	40	30	21	16	11	8

I/O pin count increases due to advances of high density circuit formation, therefore interconnect technology between chips and packages changes from wire bound to flip chip type to decrease inductance, at the same time, configuration on interconnect shifts from peripheral to full grid array with fine pitch. On package structure, a conventional package made from CCL boards can not allow to integrate density traces because through hole connection with mechanical drilling needs wide area, so a build up package consisting of fine IVH(Inner Via Hole) appropriates to flexible design as showing a build up package in figure 1.

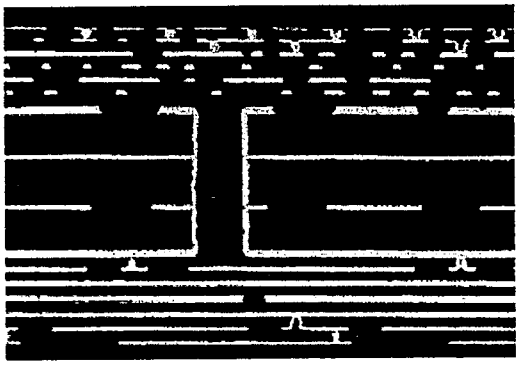


Fig. 1 Build up package with 6/4/6 layers

However, in a build up package, it is difficult to integrate density traces in the core as well as the package laminated with CCL. These days, T.H. of 0.1 or 0.15mm diameter is available in limited applications, but there are still reaming some issues on productivity.

As an alternative of glass cloth core, there is a package replaced with metal core that is easy to make fine through. Figure 2 shows one of metal core package using a thin metal plan.

In comparison with usual package, traces can be fanned out from the chip not only on topside of the core but also on backside of the core because fine pitch through holes can be formed, so layer count in package can be decreased. But in chip assembly process, as the rigidity is lost, stiffener attachment is needed to maintain flatness without occurring warpage, and also during the process to make the package, deformation easily happens. There are still some problems with productivity.

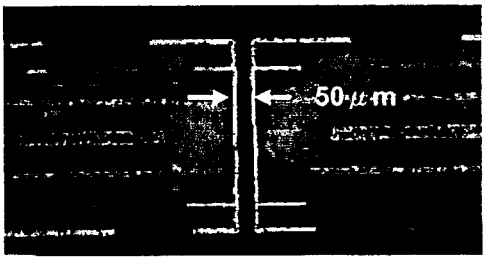


Fig.2 Metal core Package

As the others, there is a co-lamination package that is similar to a ceramic package production process, it is considered that each green layer in a ceramic package are replaced with resin sheets with trace pattern. Figure 3 shows a schematic view of the package. The process is different from sequential lamination process, pattern formation is processed to each layer in parallel so that process time is shortened, even if failures happen in a layer until co-lamination process, it is easy to be replaced with new one, so high yield is easily kept. But there are problems with via filling and via connection, how to fill small the vias with

conductive materials and how to confirm electrical connection. It seems difficult be used for a flip chip package

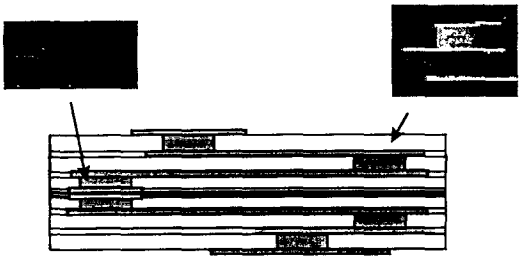


Fig.3 Co-lamination package (MFS)

Anyway it is expected to appear a new package which performs high density at low cost based on new ideas as inclusively considering advantages of each plastic and ceramic packages.

3, Build up dielectric material

On account of increasing heat generation due to high power consumption in chip, and increasing re-flow temperature due to introduction of lead free alloy for environmental protection, build up dielectric materials need higher Tg. In mechanical property, adhesion strength between resin and conductor is especially required for outer terminal pads such as pin and C/C attachment pad because the attachment method is changing from insert type to surface mount with dense terminals. In electric property, clock frequency reaches 1 GHz range so that transmission loss should be considered. The resin properties meeting these demands are shown in table 2[(2)].

In reliability, CTE (Coefficient of Thermal Expansion) value of resin should be concerned with electric open failures and resin cracks. A simulation on stress analysis arising around through hole was conducted with changing resin CTE value. Figure 4 shows a result of the analysis. Large CTE causes large stress. This simulation result well agreed with actual test.

Table 2 Dielectric material property

	Current	Next generation
Tg	170℃～	200℃～
CTE (PPM)	50～100	10～50
Dielectric constant(1GHz)	3～4	2.5～3.5
Dispassion factor (1GHz)	～0.05	～0.005
Elastic constant (Gpa)	～5	～3
Water absorption (%)	～2	～0.5

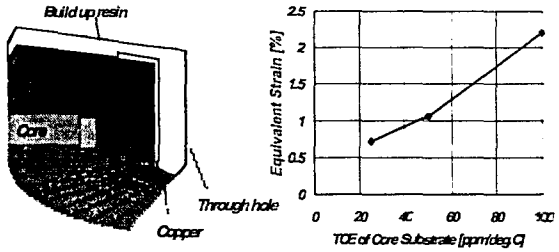


Fig.4 Stress analysis around TH

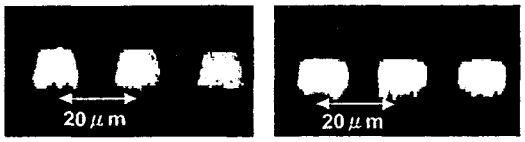
CTE of chip is around 3 ppm, board is 17 ppm, so 10 to 12 CTE is desired for resin of package. It is impossible to reduce CTE by modifying the chemical structure, some additives such as inorganic fillers are effective, but they have higher dielectric constant compared to organic, and they deteriorate resin flow property in lamination process. Small particle sizes of

the fillers are used to enable fine via formation, but it is difficult to homogeneously distribute the fillers into the resin matrix because their reactivity is high to agglomerate during processing. Careful treatment is needed for filler dispersion.

Regarding to material selection, there are environmental issues how to eliminate antimonide and bromide as the flame retardant, and how to replace with the materials excluding them with keeping quality and cost[3].

4, Trace lines, vias formation and position accuracy

As line formation method, there are subtractive and semi-additive methods. Figure 5 shows cross sectional views using each method.



Subtractive Semi-additive

Fig.5 Cross view of line

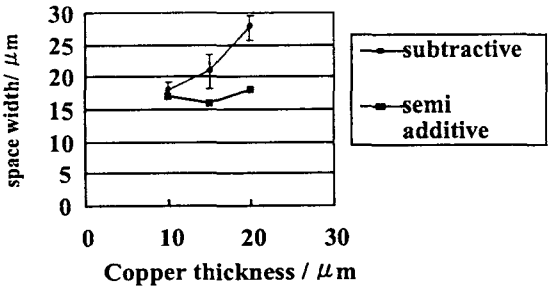
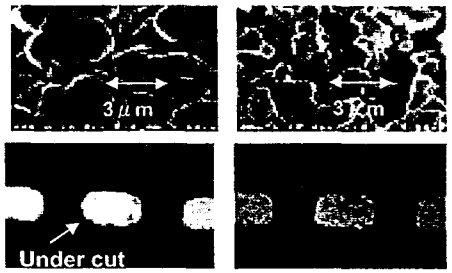


Fig.6 Feasibility of minimum space formation relating to copper thickness

A relationship between copper thickness and minimum line space is shown in figure 6. Semi-additive method is effective for finer line formation without relating to copper thickness, however, as shown in figure 7, at seed layer etching process, etching is forced to proceed to the seed layer and lose original line shape. These phenomenon especially much occur at the bottom corner of lines, This tendency depends on grain size of seed layer and roughness of base resin before plated.



Fig,7 Line shape related to grain size of seed layer

When line width reaches to around 20μm and clock frequency goes up to GHz the roughness becomes key issue on electronic performance. Figure 8 shows a simulation results of transmission loss under changed Ra and frequency, smooth roughness is needed to transmit high frequency signals.

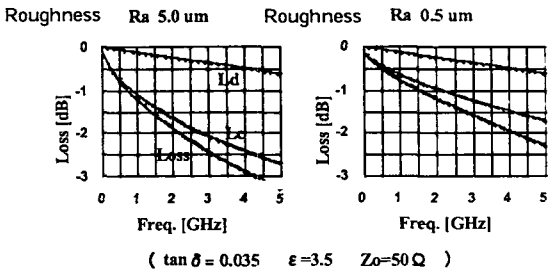


Fig.8 Surface roughness vs transmission loss

Peel strength between resin and copper trace is mainly maintained with mechanical anchor effects. When resin surface gets smooth, it becomes a key issue how to keep the peel strength. Figure 9 shows a result of obtained tight peel strength on the smooth plane shown in figure 10. This effect was achieved by introducing additional physical and chemical treatments as alternative of desmears process.

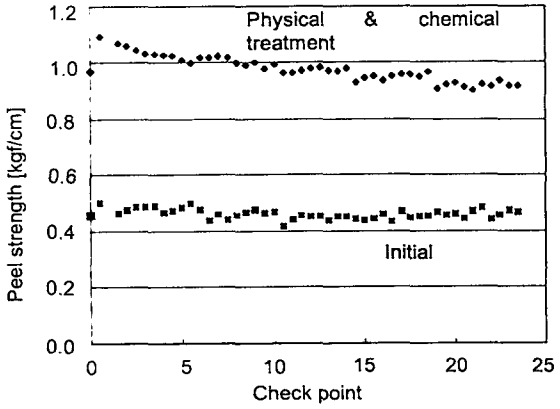
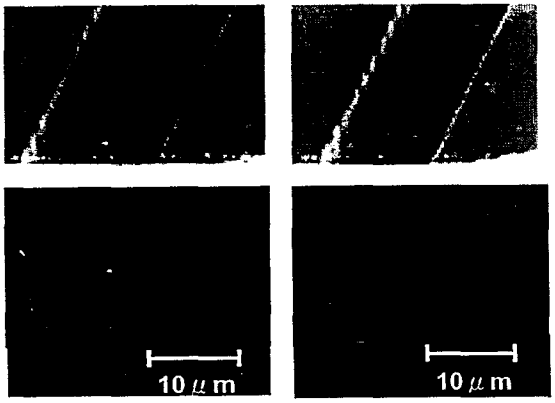


Fig.9 Peel strength on smooth resin surface



Smooth plane Ra<0.05μm

Rough plane Ra=2 to 3 μm

Fig. 10 Fine line formed on smooth surface

In via formation method, there are two methods using photo imaginable resist and thermoplastic resin with laser drilling, currently minimum via size is 70 to 80μm in production. Via size changes during desmear process as shown in figure 11, therefore desmear process has to be investigated not to enlarge via size.

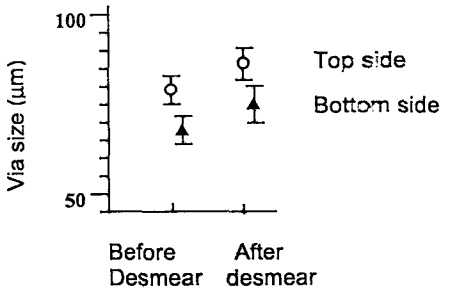


Fig.11 Change of via size before and after desmear process

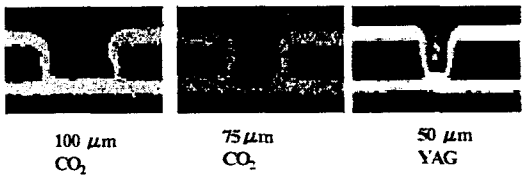


Fig.12 Via shape with CO2 and YAG laser

Figure 12 shows via shape using UV-YAG laser with short wave length than CO2 laser. In comparison with CO2, YAG laser ablates resin as decomposing chemical bounds without remaining any smears at via bottom and wall, the shape is kept good after the process, and small size via is available. These days via formation capability with YAG laser gets higher, around 200 vias per second is available under well controlled conditions including room temperature of machine

set, and laser head scan and table moving programs. Later the machine is expected to apply to mass production.

In pattern position accuracy including solder resist registration, it is important to control the changes of dimension on base core material and to keep the stability during each processing. Figure 13 shows change of dimension on work panels. To increase productivity, handling size can not be decreased, installation of a step exposure machine instead of conventional contact type might be needed to deal with the deformed panel in shape during processing.

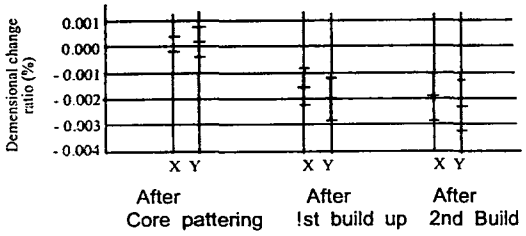


Fig 13, Change of dimension on base core materials

For characteristic impedance matching, thickness controls of copper and build up dielectric resin are needed. Following equation shows a relationship of Zo between conductor and dielectric thickness[4].

$$Zo = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon_{eff}}}\ln\frac{4h}{0.536W+0.67t}$$

W= Conductor Thickness W= Line width H= Dielectric Thickness

Micro strip structure

Under constant of Zo, as conductor width gets smaller, dielectric thickness gets thinner as well as tolerance, further process control and management are needed when line width becomes narrow in the future.

To get a proper resin thickness based on a design, well-controlled lamination process considering resin flow is needed. To control copper thickness, optimized copper plating conditions including plating solutions and facilities are essential. However there is a limitation for accurate control of thickness, as options, mechanical grinding process effects to uniform the thickness, and also soft chemical etching is useful to get desirable copper thickness. In either case, additional processes are added, it reflects to cost.

5, New technology

(1), Via fill

In general build up package, via connect between layers is stagger shape as shown figure 14, therefor some area to connect via land to via land are needed, that avoids to fine dense patterns. Figure 15 shows demonstrated stacked vias filled by copper plating with different modes in via shift position.

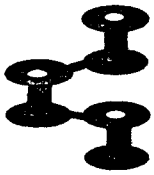


Fig.14 Via connection design

Fig. 15 Cross view of stacked vias filled by copper plating with different design

Propagation of via filling is shown in figure 16. Copper deposition is conducted from inside of bottom corner. Figure 17 shows the build up package with stacked vias and narrow trough holes in high aspect ratio using the via filling technology.

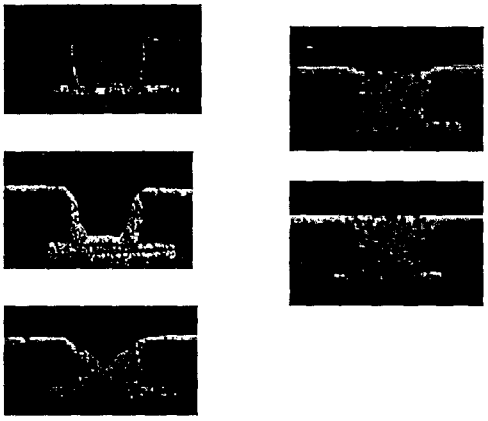


Fig.16 Propagation of via filling process

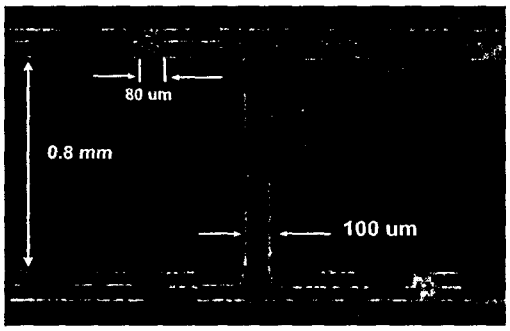


Fig.17 Exemption of a build up package with stacked vias and small trough holes in high aspect ratio

On reliability, failures such as cracks around stacked vias were caused by mismatch of CTE between resin and copper. But, so far, any failures have not been observed in test samples or actual products with stacked vias. Changes of conductive resistance in via chain samples during T/C testing are shown in figure 18.

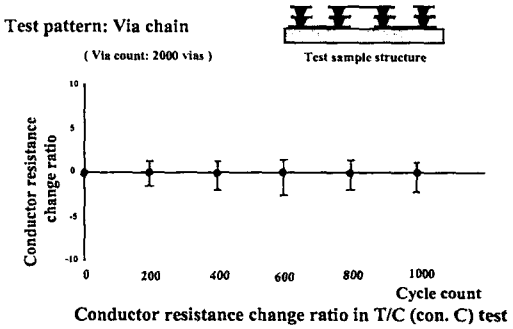
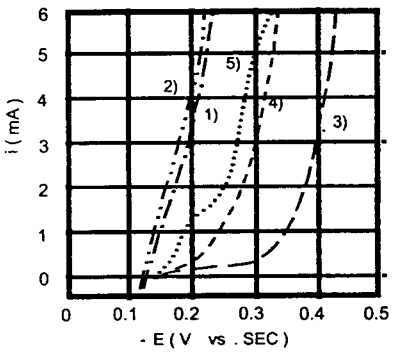


Fig.18 Changes of conductive resistance during T/C testing

To perform via filling, there are two methods using DC (direct current) and PPR (periodic plus reverse) current, in both cases, successful plating were achieved. In plating solution, some additives are added to control copper deposition ratio in via. The additives are mainly enhancer and suppresser which preferentially work for selective deposition under well-optimized condition. Figure 19 shows current potential curves under different agitation speeds. In general, as agitation speed gets higher, the curve shifts positive side, but in the solution mixed with enhancer and suppresser, it oppositely behaves.

In PPR plating, electrolytic charges with plus and minus are alternately replaced to the work panel, this will influence deposition and dissolution behaviors of the additives. The dissolution occurs selectively at the outside of vias because of the geometrical difference between inside and outside of vias based on current concentration effects[5]. These

processes can be applied to board with small vias and small through holes under semi-additive process. This means the fine patterns can be formed at the same time with via filling.



1) Additive free, 1000 rpm
2) Enhancer (A) , 1000 rpm
3) Suppresser (B), 1000 rpm
4) Enhancer (A) + Suppresser (B), 1000 rpm
5) Enhancer (A) + Suppresser (B) , 0 rpm

Fig.19 Current potential curves with different additives and agitated

(2), Embedded passive elements

As clock frequency in chip gets higher, the power tends to easily drifts and it can not be constantly supplied to the chip, introduction of decoupling capacitor to support power system should be needed. Currently, chip capacitors are mounted on top or back surface of package to keep stable power supply. It is effective to reduce inductance that the capacitors are placed the nearest position to the chip as passable as they can. Figure 20 shows a schematic view on embedded passive elements that will be required to improve electric properties in the near future[6].

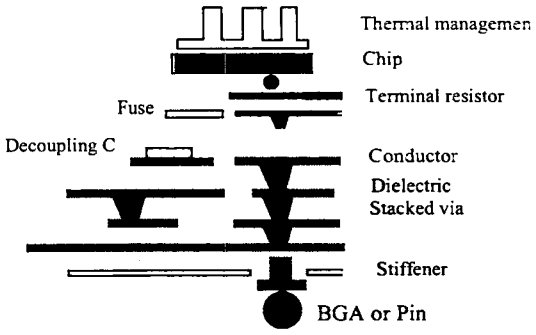


Fig. 20 Schematic structure of package with embedded passive elements

There are mainly two methods to embed them into package. One method is direct formation on inner layers of package using printing process or sputtering process at low temperature with gentle chemical treatments. The other is that once they are formed on a different material that is tough and stable against tough process, and also matches with package material, they are transferred to package.

In former method, some powder consisting of high dielectric constant mixed with resin are used and coated on the layers with printer and they are dried at middle temperature. But this process can not be expected to provide high value because the capacitor itself is not dense bulk. In later method, high value can easily be obtained, but the cost is higher because of complex process that is to transfer the capacitor and to connect an electrode to package in accurate position. Generally when a different material is intruded into package, the reliability must

be concurred because of CTE mismatch or another mismatch. As far as latest experiment on capacitor formation, TaO formed with dry and wet chemical treatment process led to good effects to satisfy a required value and reliability test.

These technologies get much more to be focused how to realize reasonable performance with high reliability at low coat. Not only package and also substrate for cellular phone need these technologies to transmit high frequency signal in GHz range.

6, Conclusions

Performance of semiconductor chip is dramatically increased, and wafer size is getting larger to reduce cost. According to these trends, package should be required to go up performance with redacting cost as well as chip.

In package structure, to achieve further fine patterns, standard build up package with glass cloth core should be improved to integrate fine patterns on the core layers. There is coreless package or co-lamination package as an option, but still some issues are remaining in productivity and reliability.

For fine pattern formation, semi-additive process is effective, but there are some problems with line shape that relates to grain size of electroplating. For high signal transmission, smooth surface is needed, but how to maintain tight peel strength is key issue. This time in just laboratory, introduction of a physical and a chemical treatment could achieve it.

To perform via filling for stacked vias, proper plating additives and optimized condition are essential. This technology can be applied to board with fine vias and small T.H. For fine via formation, YAG laser is effective because desmear process is not needed to remove residual so that original shape is kept.

For embedded passive element formation, TaO is one of suitable materials that can be treated under gentle process.

7, Reference

(1), "atest road map of SIA" Electric Journal, June/1999, June/1998 pp 42-43

(2), Tanaka Z., Sato H., Tezuka N. "Trend of package materials" Electronic packaging technology February/2000 V0l.16 No2 pp18-28

(3), Halogen free flame retardant Polyfile March/2000 pp 43-

(4), Nakazawa K., others Fundamental of circuiting and mounting, VSL system design

(5), Shin-ichi Wakabayashi "Electronic packaging technology and plating technology" The journal of the surface finishing society of Japan, 50th ,years anniversary of foundation lecture proceedings, March/2000

(6), Rao R. Tummala "System on a package" 2000 IEMT/IMC proceeding pp218-224

2nd Korea-Japan Advance
Semiconductor Packaging
Technology Seminar
26th/Oct. 2000

High Density Processing for a Flip Chip Package

Shinko Electric Industries CO.LTD
Core Technology Research & Laboratory
Sho-ichi Koyama, Shin-ichi Wakabayashi

SHINKO

1, Background of Packaging Technology

2, Package Structure

3, Dielectric Materials

4, Trace Pattern and Via Formation

5, New Technology

6, Conclusions

SHINKO

Road Map on Semiconductor Chip and Package

Years of first product shipment / *technology node*	*1997* / *250nm*	*2000* / *180nm*	*2002* / *130nm*	*2005* / *100nm*	*2008* / *70nm*	*2011* / *50nm*
Performance: on chip/MHz						
Cost-performance	350	526	928	1108	1468	1827
High-performance	600	958	1768	2075	2574	3081
Chip pad count						
Cost-performance	256-768	300-934	378-1277	476-1747	600-2386	755-3268
High-performance	1515	1867	2553	3492	4776	6532
Package pin count						
Cost-performance	256-568	300-700	378-957	476-1309	600-1791	755-2449
High-performance	1136	1400	1915	2619	3581	4898
Flip chip pad pitch/μm	250	180	130	100	70	50
Line width /μm	40	30	21	16	11	8

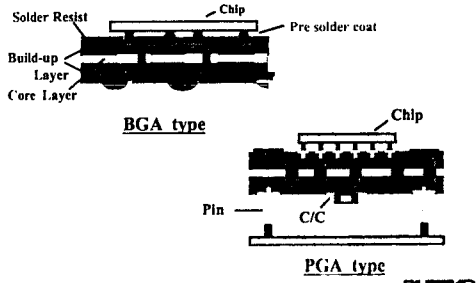
www.semichips.org

SHINKO

Package Structure

SHINKO

Build Up Package Types



SHINKO

Package Feature of Standard Build Up

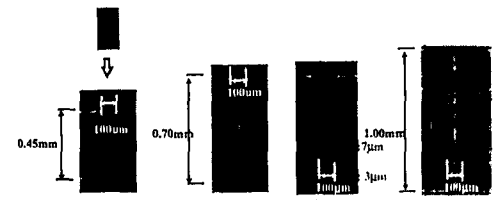
Standard build up package

Trace integration on Core layer

Structure = 6 / 4 / 6

SHINKO

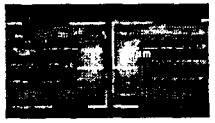
Fine Through Hole with Mechanical Drill



Process condition
Material : STD material
Entry sheet using
Drill spin speed : 120.000

Package Feature with built up onto Metal Core

Metal core package

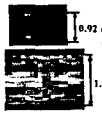


Metal core ⇨ Handling
Warpage

Stiffener

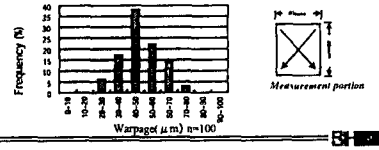
Warpage on PKG

» Relationship with PKG thickness



PKG Thickness	Total layers	Build-up layers	PKG size	Warpage (μm) Av.	Max.	Min.
0.92	6	4	40mmsq.	42	74	23
1.8 mm	16	12	45msq.	21	35	10

» Variation on warpage value in 0.92 thickness package



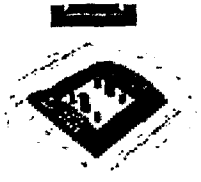
PKG Structure

Warpage on PKG After Chip Mount

» Warapage mode without and with stiffener

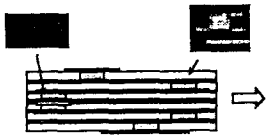
without Stiffener

with Stiffener



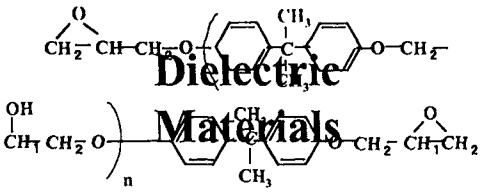
Package Feature of Co-Lamination PKG

Co-lamination package



⇨ Reliability
Via filling with conductive paste into fine via hole

Dielectric Materials



Dielectric Material Properties for Build Layer

	Current used materials	Materials used for next generation
Glass Transition Temp.(Tg)	120～180℃	180℃～
C T E (PPM)	60～100	10～50
Dielectric Constant (1GHz)	3～4	2.5～3.5
Dielectric Loss (1GHz)	～0.05	～0.005
Elastic Constant (Gpa)	～6	～3
Water Absorption rate (%)	～2	～0.5

Environmental issues: Non-halogen, -bromine, -antimony

SHINKO

Resin Properties for Next Generation PKG

Property	Cause	Solution
High Tg	High electric power consumption in chip Exchange to Lead free solder	high bridge density
Low water absorption	For improvement of migration of hydrolysis	Alternation to Non-polar group
Low CTE	CTE Matching between Si and Package	high bridge density Additive of Filler

Productability

Copper peel strength

SHINKO

Resin Cracks

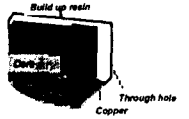
C.T.E : 80ppm/℃
after T/S (-50℃⇔125℃) 500cycles

SHINKO

Simulation with Finite Element Method

Parameters for simulation

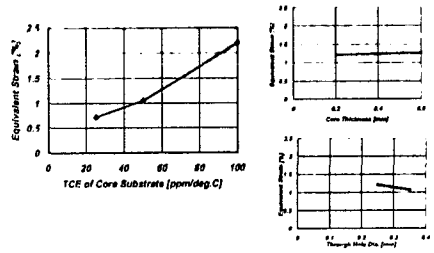
	C.T.E. α of Resin [ppm/deg. C]		Core Thickness [mm]	Through Hole Dia [mm]
Pattern 1	80		0.6	0.35
Pattern 2	80		0.6	0.35
Pattern 3	80		0.6	0.35
Pattern 4	80		0.6	0.39
Pattern 5	80		0.6	0.25
Pattern 6	80		0.2	0.25



Simulation model (1/4 th portion of through hole)

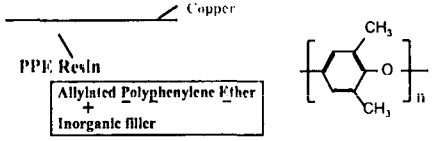
SHINKO

Simulation Results of Equivalent Strain at each parameter (CTE, Thickness, Hole size)



SHINKO

PPE Chemical Structure & Properties

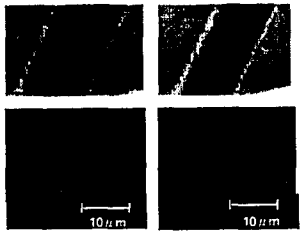


Item	Property
Tg(TMA)	185℃
Dielectric Constant	3.4(1MHz)
Dissipation Factor	0.002(1MHz)
Water Absorption	0.2% *1
C.T.E.	α 1: 45ppm/℃
Solder Resistance	>120sec @260℃

*1) E-24/50+D-24/23

SHINKO

Fine Trace Formation on Smooth Surface



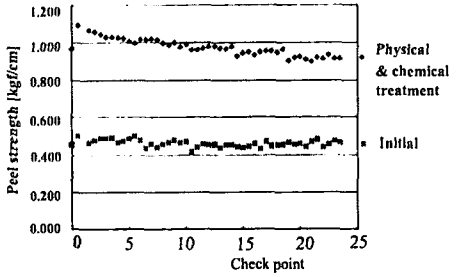
Modified PPE resin Ra<0.5 μm

Current used resin Ra=2~3 μm

Process:
Semi-additive

Base resin
⇩
Physical & chemical treatment
⇩
Cu electroless plating
⇩
Cu electrolytic plating

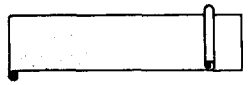
Peel Strength of PPE Resin with Smooth Surface



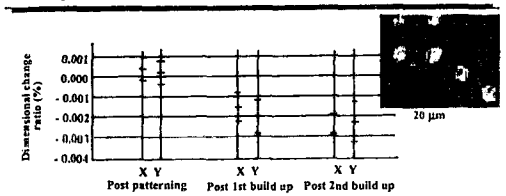
Organization How to Keep Peel Strength

In current used resin
"Anchor effects"

In smooth flat resin



Registration

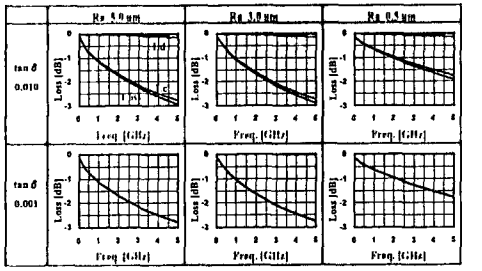


Dimensional change ratio (510mm x340 mm)

Exposure mask: Film ⇨ Glass mask
Machine: Contact type ⇨ Stepper

Simulation Result of Transmission Loss

surface roughness (Ra) and dielectric loss tangent (tan δ) vs Frequency



Here Lc = conductive loss , Ld = dielectric loss , Loss = all transmission loss,

Via Formation Status by Lasers

Laser	UV-YAG	CO_2
Principle	Photolysis	Thermal decomposition
Via Size	20~50 μm)	60~150 μm)
Process Speed	200 (via/sec.)over	400 (via/sec.)over
Residual	None	Denaturation Carbon
Others	Taper shape	

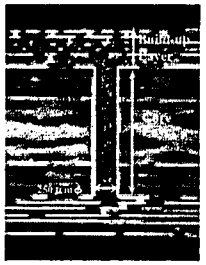
Trace Pattern and Via Formation

Package Design Guide

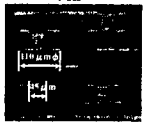
Build-up Layer	Via (Top/Bottom)	φ50_80μm
	Land	φ110_160μm
	Max. Layers	6
	Line/Space	30_50μm
	Insulation layer thickness	30～70μm
	Conductive layer thickness	15～20μm
Core Layer	Drill	φ250μm
	Land	φ400μm
	Line/Space	80/80μm
Solder Resist Clearance		±20μm

Panel size :510×340mm

High Pin Count STD Package (Layer ⌐ 6 / 4 / 6)



Via



Build-up Layer

Future Designs

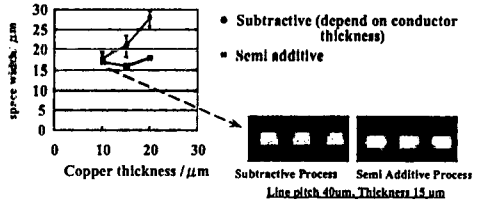
» FC pad pitch
250 μm ⇨ 150 μm

» Via size
50～80 μm ⇨ 30～40μm

» Line/space
40 μm ⇨ 20 μm

Feasibility of Fine Pattern Formation

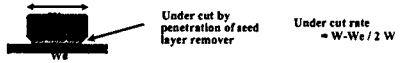
» Fine space formation ability with Subtractive vs Semi-additive process



Actual view on line/space

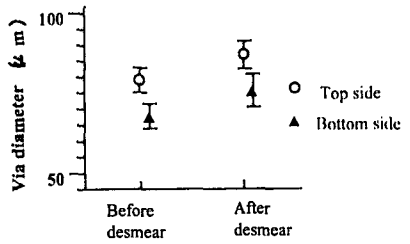
Line Shape with Elecrtoless Plating in Semi-Additive Process

» Line shape relays on crystal size of electroless plating



Under cut rate	0.20	0.1
Actual cross section view		
Crystal size		

Via Dimension Change by De-Smear Process



Via Shape with Laser Processing

New Technology

Stacked Vias

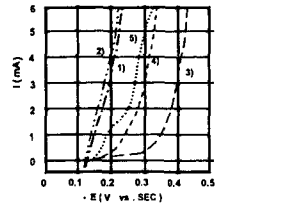
STD vias

Via Filling Process

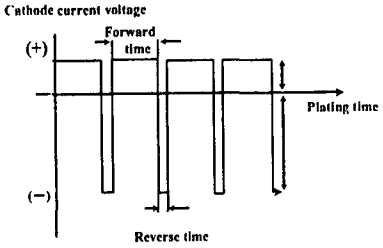
Propagation on via filling

Current Potential Curves

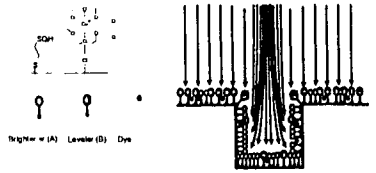
on copper solution with each additive



Current Voltage in PPR Plating



Adsorption Structure of the Additives and Current Distribution at via (Schematic)

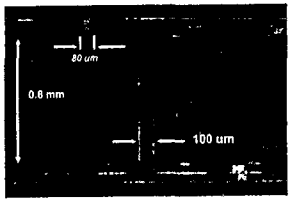


Via filling Capability

Via size (μ m)	50	40	30
Aspect	1.5 / 2.0	1.5 / 2.0	1.5 / ✕

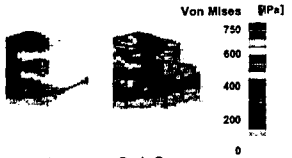
Package with Filled Vias and Fine T.H.

» Optimized via filling process achieved package production utilizing filled vias and fine narrow TH



Stress Distribution on Stacked Via with liner static analysis

» Large CTE material induces large stress around stacked via



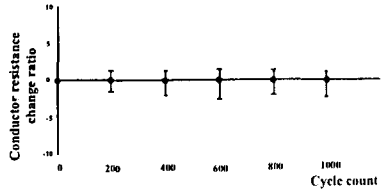
Resin A
CTE=50 ppm
Stress: 380MPa

Resin B
CTE=100 ppm
Stress: 933MPa

Stress distribution analysis

Reliability Test Result of Stacked Vias

Test pattern: Via chain
(Via count: 2000 vias)



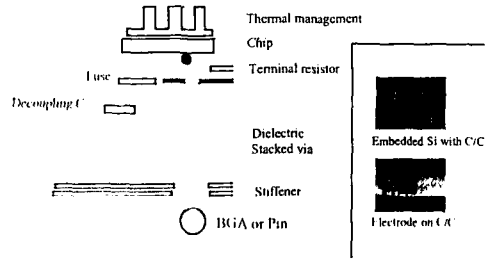
Conductor resistance change ratio in T/C (con. C) test

Reliabilities Test Results of Package

Description	Check stage	Result
Pre-con. Level 2:		Pass
TC (condition B) : -55C to 125C	1000 cycles	Pass
TC (condition C) : -65C to 150C	1000 cycles	Pass
TS (condition B) : -55C to 125C	1000 cycles	Pass
PCT : 121C /2.1 atom /100%	336 Hrs	Pass
HAST : 130C / 85% / 5.5V	336 Hrs	Pass
THB : 85C / 85% /5.5V	1000 Hrs	Pass

Pre-con. Level 2: 125C/24Hrs 85C/65%/168Hrs IR225C/3 times
Test sample : Structure- 2/2/2, Via - all filled via
Pass: Non-failure in visual and electrical change (within ±10 %)

Schematic View of Package with Embedded Passive Elements



Issues on Package with Embedded Passive Elements

» Effective materials to meet requirement values on C, R,,
» Package structure and specification
» Formation and fabrication processes into Package including facilities
» Reliability
» Cost

Conclusions

- For further fine pattern integration, glass cloth core in a STD build up package is needed to alternate with another equivalents which are easy to make fine T.H.
- For fine pattern formation, Semi-additive process is effective, but there are issues on the line shape, which relates to grain size of electroless plating.
- For high signal transmission, smooth surface is needed, but for maintaining tight peel strength, a different organization from anchor effects should be investigated excepting thin film process. This time in laboratory, it could be achieved.
- For stacked via formation, some additives and optimized plating condition are essential.