Adhesives Flip Chip Technology

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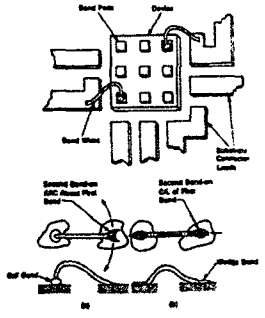
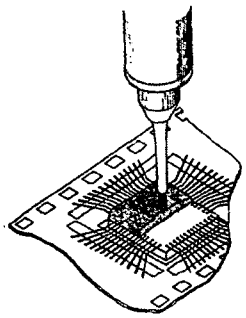
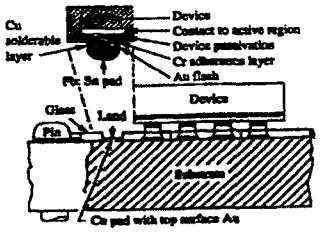
3 Chip Interconnection Technologies



Wire Bonding



Tape Automated Bonding (TAB)



Flip Chip

Wire Bonding Interconnection

Wire bonding is a method used to connect a fine wire between an on-chip pad and a substrate pad. This substrate may simply be the ceramic base of a package or another chip. The structure of a wire bond assembly is shown in Figure . Common wire materials include gold and aluminium.

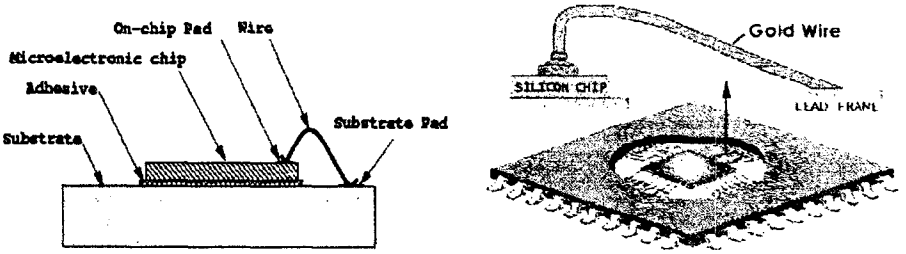


Figure: The wire bonding assembly shows how a bare chip is interconnected to a substrate or another chip using a wire conductor. Hence, the 'substrate pad' may either be a package pad or a pad on another chip.

The main advantage of wire bonding technology is that it is low-cost. The disadvantages include (a) low I/O counts due to technology limitations, (b) large bonding pads in the order of 100 100 m , (c) large bonding pitch in the order of 200 m, (d) the requirement for relatively large quantities of gold, (e) production rate, (f) relatively poor electrical performance, (g) variations in bond geometry and (h) robustness and reliability problems brought about by environmental conditions.

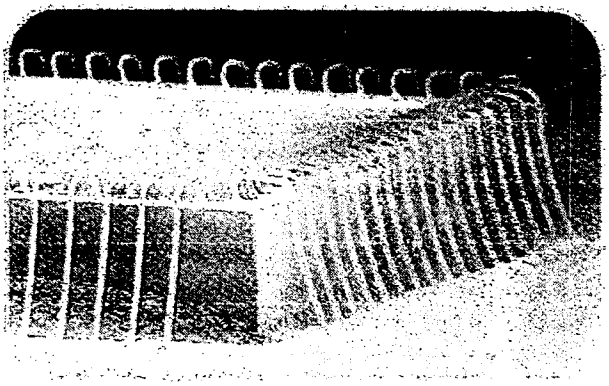
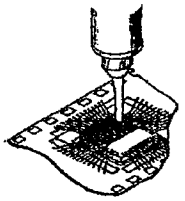
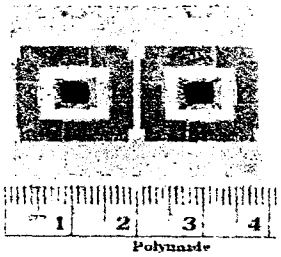


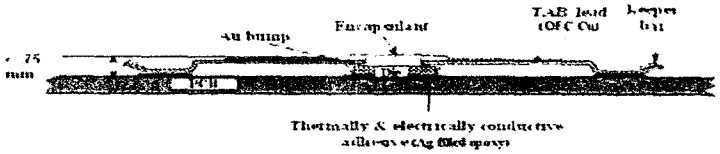
Figure 2. CSP loops created by a ball bonder. Special bends are formed that provide this shape with the second bonds close to the die edge.

Tape Automated Bonding (TAB)

To increase performance of wire bonding, engineers have replaced the wire with **etched copper leads plated with gold**. The leads are supported with **polyimide plastic film**. The resulting assembly has better electrical performance, and can achieve a higher density of interconnections. It also has a lower overall height than other methods of assembly. For these reasons, it is the dominant method of **packaging chips for driving liquid crystal displays**. It is also used for some very cost-sensitive high volume consumer electronics products like **digital watches and calculators**. It was once predicted that TAB would replace wire bonding, but it has not, due to higher costs and inflexibility in design associated with the production and inventory of the tape. As a result, TABs are only rarely **used for digital logic chips** like this one.







Tape-Automated Bonding

Tape-automated bonding (TAB) is an approach to fine the pitch interconnection of a chip to a leadframe. The interconnections are patterned on a multilayer polymer tape. The tape is positioned above the 'bare die' so that the metal tracks (on the polymer tape) correspond to the bonding sites on the die, as shown in Figure . A new version of TAB, referred to as '**area TAB**', borrows a good idea from a bonding technique called 'bump bonding' (which will be discussed in section). *In this version,* metal bumps are distributed over the entire surface of the chip (ie. I/O and power/ground terminals are not constrained to the chip periphery) - thus a large I/O count becomes viable.

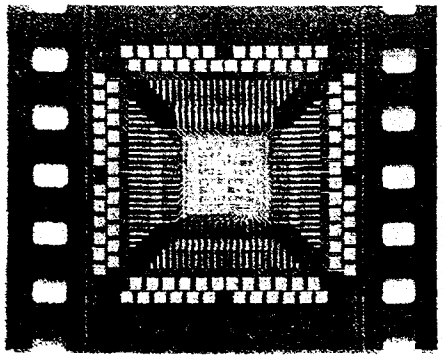


Figure: Tape-automated bonded die with a bare chip placed on the tape and connected to an interconnection pattern (Courtesy of Westinghouse ESG).

The tape-automated bonding technology provides several advantages over the wire bonding technology. These advantages include

(a) a smaller bonding pad compared to wire bonding technology,

(b) smaller on-chip bonding pitch in the range of 100 m,

(c) a decrease in the quantity of gold used for bonding,

(d) the reduction of variations in bond geometry,

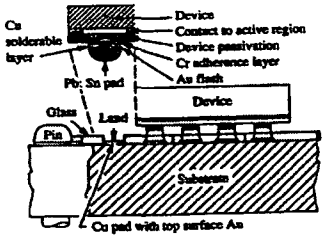
(e) an increase in production rate because of area or 'gang' bonding, and

(f) a stronger and more uniform inner lead bonding strength.

In addition to better electrical performance (noise and frequency), lower labour costs, higher I/O counts (up to 850 pins) and lighter weight, greater densities are achievable and the chip can be attached in a face-up or face-down configuration. On the other hand, the disadvantages of TAB technology include the time and cost of designing and fabricating the tape and the capital expense of the TAB bonding equipment. In addition, each die must have its own tape patterned for its bonding configuration. For these reasons, TAB has typically been limited to high-volume production applications.

Advantages of Flip Chip Interconnection

1. *Low Inductance, Capacitance*
2. *High I/O Density*
3. *Small Package Size*
4. *Self Alignment*



Flip Chip

Controlled Collapse of Bumps

As Placed During Reflow

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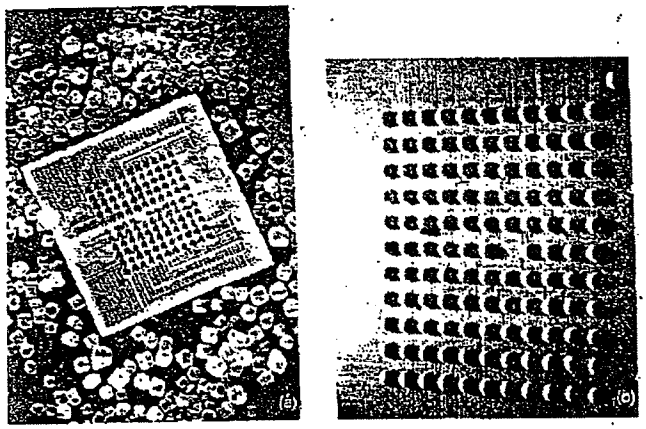

Figure 6-8. Area Array C4 Configuration. (a) An 11 x 11 full area array of solder bumps on a 730-circuit logic chip for use with multilayered ceramic. (b) SEM view of solder bumps. After Goldmann, Ref. [5], 1983, reprinted with permission of Solid State Technology.

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Comparison of Wirebond, TAB, and Flip Chip

* **Number of interconnections**
* **Interconnect area**
* **Electrical properties**
* **Cost**
* **Assembly**

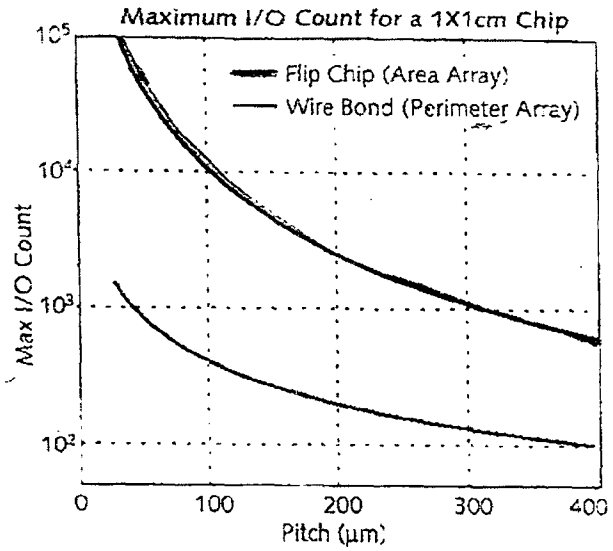

Figure 1. Flip chip technology enables a higher I/O count per pitch than that of perimeter arrays.

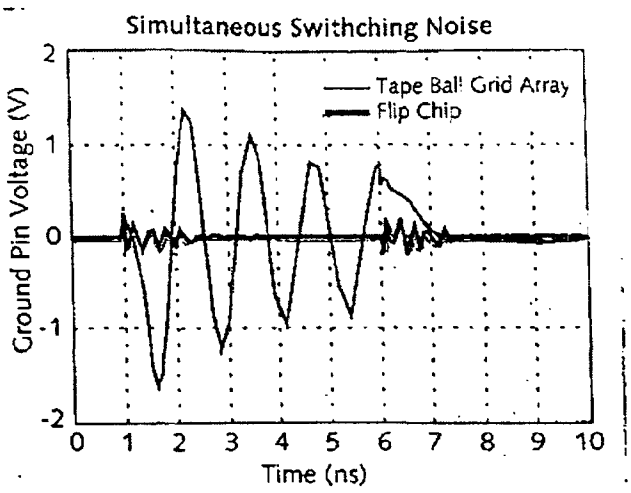

Figure 7. A circuit designed to simulate the effects of solder bumps on IC behavior (a) demonstrates the performance improvements attainable with flip chip (b).

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Comparison of Interconnect Technologies

	Size (um)	Length (mm)	Pitch (um)	Typical I/O	Inductance Lead (nH)
Wire bond	25 dia.	1	100	320	1 - 2
C 4	100 dia.	0.1	400	625	0.05 - 0.1
T A B	50 x 50	1	100	400	1

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