2nd Korea-Japan Advanced Semiconductor Packaging Technology Seminar

Recent Trend in Japanese Packaging Technology

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IMAPS–Japan

2nd Korea-Japan Advanced Semiconductor Packaging Technology Seminar

Recent Trend of Japanese Packaging Technology

IMAPS Japan
Nagano Institute of Technology
Dr.S.Denda

October 26, 2000 in Seoul

Technological Topics under Development and in Pre-Production

- Various Wafer Level Packaging
- Chip Stacked High Density Devices
- Thin Package with Paper Thin Chips
- Extension of Flip Chip Interconnection
- Pb Free Soldering Adoption Roadmap
- Higher Density Built-up Substrate
- Finer Wiring Pattern for Redistribution
- Cu Plating Via Filling Mechanisms
- Substrate Materials Development

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Next Generation Technology Development in Institutions

- 3D Chip Stacking with Chip Through Hole
- Optoelectronic Packaging
- Active Research Groups at Universities, Tokyo-U, Waseda-U, Shinshu-U, Okayama-U, Osaka-U
- Japan Institute of Electronics Packaging (JIEP-IMAPS Japan)
- Pb Free Soldering Development (NEDO-EIAJ-JEIDA)
- Super Connent Program (10μ range technology)

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Wafer Level Packaging- WLP

- WLP is aiming at lower device cost than CSP
- *Redistribution is essential for peri-pheral pad chips*
- Reliability is assured by resin coating
- Redistributed flip chip is WLP group
- MOST is growing
- New WLP company started
- Bumping business started

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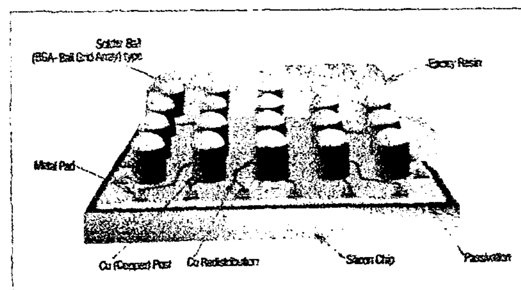
WLP CSP Post Structure (IEP)



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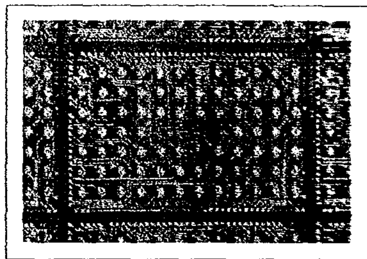

Redistributed Wafer Lebel CSP showing Copper Posts

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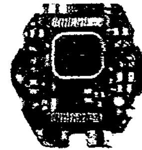
Application of WLP to Wrist Watch (Casio



Conventional Wire Bond COB

WLP CSP Chip

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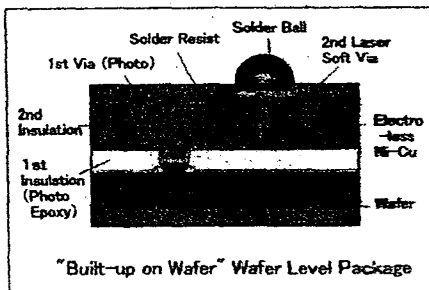

"Built-up on Wafer" Wafer Level Package

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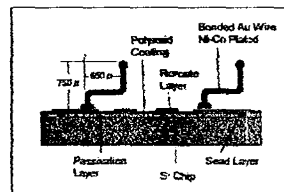
MOST(Microspring on Silicon Technology) by FormFactor and Shinko



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Chip Level Stacking Device

- Mainly for Cellular phone
- Needed more memories
- 2-3 chip CSP by wire bonding or flip chip
- Low loop wire bonding
- Thickness is limited, 1.4mm
- Chips are ground to 50μ
- Sharp, Toshiba, Fujitsu, Rohm, Epson
- ASET approach is chip through hole

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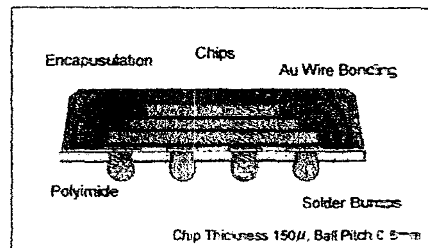

3 Chip Stacking CSP Package by Sharp

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Chip Through Hole Stacking 3D Package, ASET

Wafer through hole etching
Side wall CVD
Cu plating Cu filling

Dual Damascene CMP
Backside grinding
Bump formation

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Package Level Stacking Device

- 40-50 μ thick chips are packaged
- Device can be tested before stacking
- Dicing Before Grinding technology
- Grinding after packaging
- Au or solder bumps
- Total heights less than 150 μ
- Toshiba, NEC, Misuzu, Atomnics, Shinko, Ibiden

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Printed Resin Encapsulation
Low Loop Au Wire Bonding
Maximum Heights 1.4mm
LSI Chips
70 μ Thin PCB Interposer
Printed Solder Bumps

Package Level Stacking Device, Toshiba-Misuzu

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Cu Via Filling

- Vias are filled with Cu during plating
- Largely depends on additives and pulse current
- Important for cost reduction and surface flatness
- Several mechanisms proposed

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Cu Via Filling on Built-up Substrate (Shinko)

Plating Time:10min.

Plating Time:30min.

Plating Time:50min.

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Built-up Substrate (6+4+6) by Shinko

Poly Phenylene Ether Layer for 250 μ Pitch Chips
L/S=45 μ, Via Diameter=50 μ, Land=110 μ Dielectric=30 μ
Vias are filled by Cu

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Flip Chip Interconnection

- Bump pitch close to 150μ (area), 60μ (SBB)
- Microprocessor with C4 bumps and built-up substrate
- ACF and NCP connection and underfill
- SSB becoming more popular

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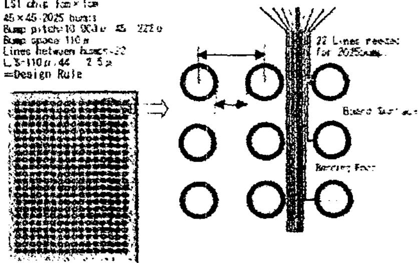

Fine Line Requirement on Board (one layer)

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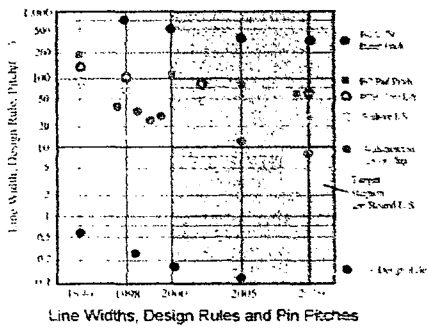

Line Widths, Design Rules and Pin Pitches

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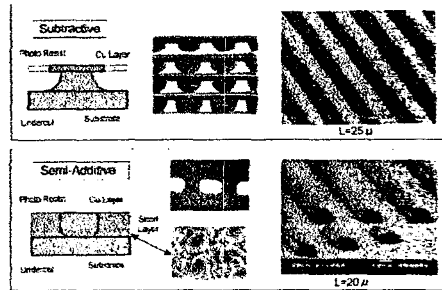

Fine Wiring Pattern Formation

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High Performance BGA

- Enhanced BGA with high speed signal and better thermal characteristics
- Double Layer tape interposer
- Metal heat spreader
- 800-1000 pins

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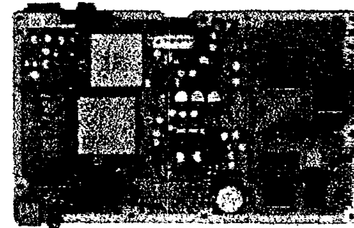

Playstation 2 (SCE-Toshiba)

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